

DESIGN NOTES

1.25Msps, 12-Bit ADC Conserves Power and Signal Integrity on a Single 5V Supply – Design Note 146

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INTRODUCTION

The new LTC[®]1415 expands LTC's family of high speed, low power 12-bit ADCs. Operating on a single 5V supply, it is optimized for applications such as ADSL, HDSL, modems, direct down-conversion, CCD imaging, DSP-based vibration analysis, waveform digitizers and multiplexed systems. The LTC1415's block diagram is shown in Figure 1.

Single 5V Supply, High Speed, Lowest Power

The new LTC1415 has lower power dissipation and better performance and features than other 12-bit ADCs currently on the market. It samples at 1.25Msps and dissipates just 55mW. NAP and SLEEP modes reduce dissipation even further. Its 28-pin SO and SSOP packages offer the industry's smallest footprint.

A separate output-driver supply pin, OV_{DD}, allows the ADC to interface to either 3V or 5V digital systems.

Tiny Package

The LTC1415 is the smallest 1.25Msps 12-bit ADC available. Its 28-pin SSOP occupies just 0.123in², 43% of a 28-pin SO. It operates with equally tiny 0.1μF 0805-sized surface mount supply bypass capacitors and a small 10μF 1206-sized ceramic reference bypass capacitor.

Complete ADC with Reference and Wideband S/H

The LTC1415 includes a 10ppm/°C 2.5V reference that is suitable for use as a system reference. This internal reference sets the LTC1415's full-scale input range from 0V to 4.096V. The circuit in Figure 2 trims the full-scale (gain) error without placing additional circuitry in the signal path.

The LTC1415's fully differential S/H has a typical 20MHz input bandwidth and very good CMRR of 60dB or better over a DC to 10MHz bandwidth. AC specifications are measured with single-ended ($-A_{IN}$ grounded) signal drive. Offsetting $-A_{IN}$ above ground eases the drive requirements of rail-to-rail op amps that drive the LTC1415's input.

BENEFITS

Reduce Power with Single Supply Operation and Two Power Saving Shutdown Modes

The LTC1415 has NAP and SLEEP modes that further reduce the converter's low 55mW power dissipation. NAP mode shuts down all converter circuitry except the 2.5V reference, reducing dissipation by 95%. The converter

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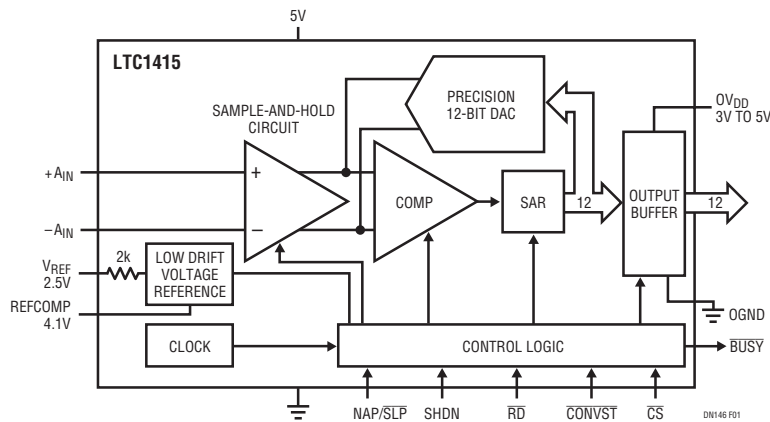


Figure 1. This Complete 5V, 12-Bit, 1.25Msps ADC Comes in a 28-Pin SSOP

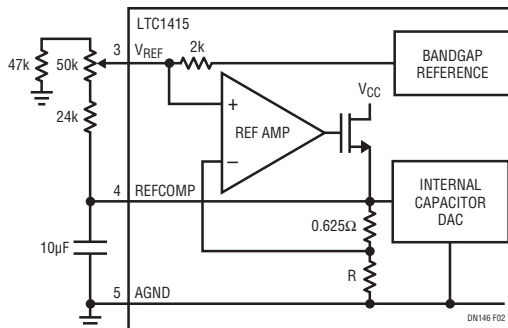


Figure 2. Adding Nothing to the Signal Path, This Simple Circuitry facilitates Full-Scale Adjustment

returns from NAP mode very quickly because the active reference keeps its bypass capacitor charged.

SLEEP mode reduces dissipation to 30µW by shutting down all of the LTC1415's internal circuitry. The converter returns from SLEEP more slowly than from NAP mode because the reference must recharge its bypass capacitor. The converter is ready after a typical settling time of 10ms when using a 10µF bypass capacitor as shown in Figure 2.

Wide Bandwidth CMRR

The ADC S/H's excellent CMRR eliminates the effects of common mode ground noise. The CMRR is constant over the entire Nyquist bandwidth ($f_s/2$), dropping 3dB at 5MHz. This ability to reject high frequency common mode signals is very helpful in sampling systems where switching transients often cause high frequency noise.

No Latency and Low Bit Error Rate (BER)

The LTC1415's successive approximation architecture is optimum for high speed data conversion and achieves two important benefits. This first benefit is absence of latency (a time delay of more than one sampling period between sampling an input signal and generating an output code). SAR converters generate data from the current sample before taking the next sample. Thus, unlike high speed converters using pipeline conversion techniques, the LTC1415 is always free of data latency. Absence of latency is advantageous for signal multiplexing, closed-loop control systems, single shot event driven measurements and DSP feedback systems

The second benefit is reduced BER. The LTC1415 is inherently immune to bit errors or "sparkle codes" (infrequent conversion errors as large as full scale in magnitude), unlike subranging or pipelined converters. The LTC1415's BER is immeasurably low, less than 10^{-15} .

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DSP Interface

The LTC1415's high speed parallel digital interface can be connected directly to a DSP, or by using the CS and RD pins, data can be retrieved when desired. The edge-triggered CONVST signal precisely controls the sampling instant, essential for processing signals and maintaining signal integrity.

Exemplary AC and DC Performance

The LTC1415 handles input signals with great care. Its differential S/H has a wide, 20MHz bandwidth and achieves -75dB THD for a 625kHz, 4.096V_{P-P} input signal. This AC performance is complemented by DC specifications that include ±1LSB maximum differential linearity error (0.25LSB, typ) and integral linearity error (0.2LSB, typ) guaranteed over temperature.

The FFT in Figure 3 reveals the LTC1415's 1.25MSPS conversion rate performance with a full-scale 100kHz sinewave input signal. The curve shows -88dB THD and 72.8db SINAD (11.8 ENOBs).

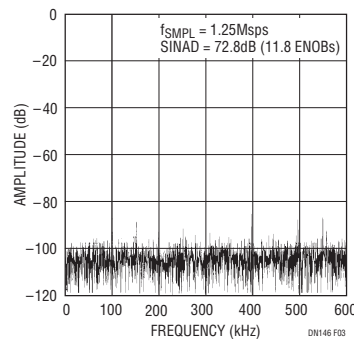


Figure 3. FFT of the LTC1415's Conversion of a Full-Scale 100kHz Sinewave Shows Excellent Response with a Low Noise Floor While Sampling at 1.25MSPS.

Figure 4 shows that the 11.8 effective number of bits (ENOBs) remains flat out to an input frequency of 200kHz and maintains 11-bit AC performance at 1MHz.

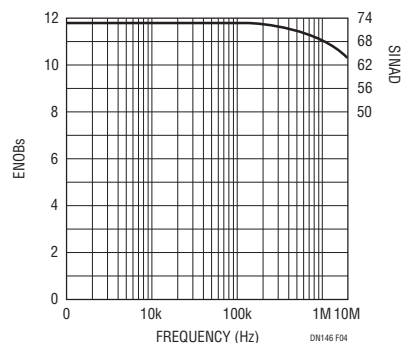


Figure 4. This Curve Shows That the Dynamic Performance of the LTC1415 Remains Robust Out to an Input Frequency of 1MHz, Where it Maintains 11-Bit Performance