

ADSP-CM403 Sinc—Isolated Measurement in Solar Applications

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INTRODUCTION

Voltage and current measurement in solar applications requires isolated measurement techniques. DSP sinc inputs along with Analog Devices AD7401A isolated ADC make just one example of an Analog Devices signal chain that offers such isolation measurements.

This document describes the typical signal chain of a measurement application designed by Analog Devices using the ADSP-CM403xy and the AD7401A devices.

SOLAR PV INVERTER SYSTEM

A solar PV inverter converts power from a solar panel and deploys this power to the utility grid efficiently. Power from the solar panel, which is essentially a dc current source, is converted to ac current and fed onto the utility grid in phase with the frequency of the grid and to a very high efficiency

level. The conversion can take one or more stages (see Figure 1). Stage 1 is typically a dc-to-dc conversion where the low voltage and high current of the solar panel output is converted to high voltage and low current. The reason for this is to raise the voltage to a level compatible to the peak voltage of the grid. Stage 2 is typically the conversion of dc voltage and current to ac voltage and current, typically using an H-Bridge topology.

ADC THEORY—AD7401A

The AD7401A is a second-order, sigma-delta (Σ - Δ) modulator that converts an analog input signal into a high speed, 1-bit data stream with on-chip digital isolation based on Analog Devices *iCoupler*® technology. The AD7401A operates from a 5 V power supply and accepts a differential input signal of ± 250 mV (± 320 mV full scale). The analog modulator, eliminating the need for external sample-and-hold circuitry, continuously samples the analog input. The input information is contained in the output stream as a density of ones with a data rate up to 20 MHz. The original information is reconstructed with an appropriate digital filter, namely a sinc filter. The processor side (non-isolated) can use a 5 V or a 3 V supply (V_{DD2}).

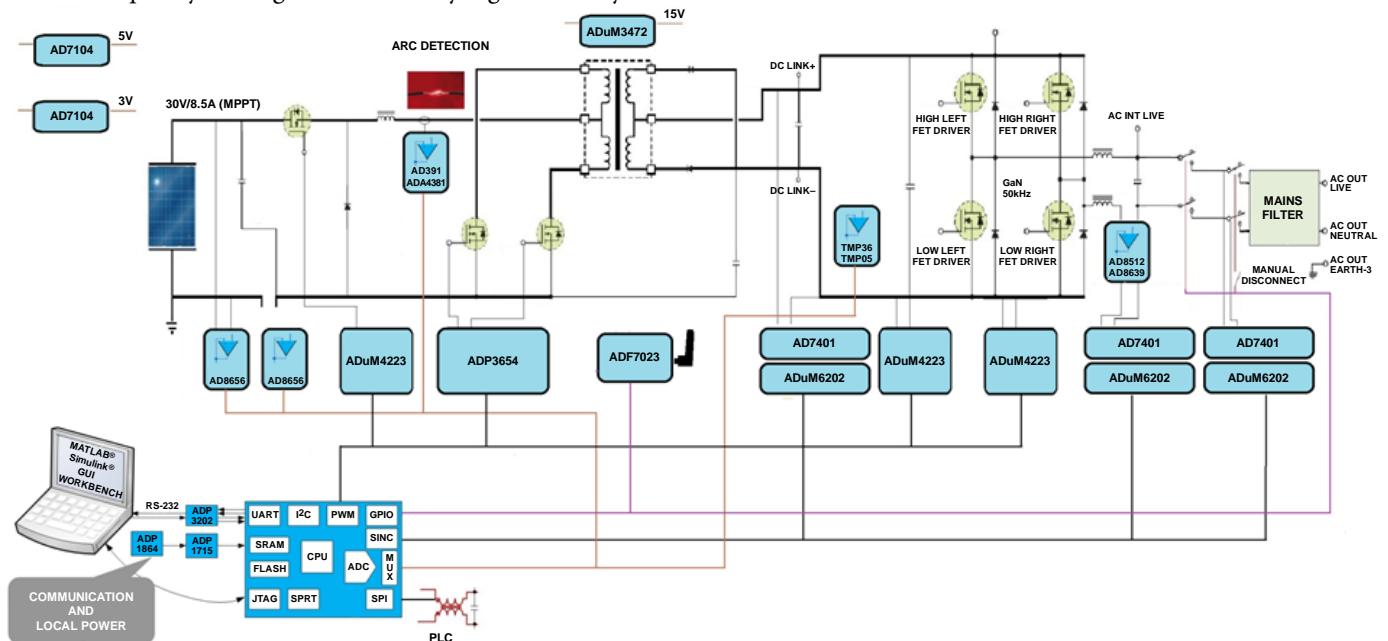


Figure 1. Solar PV Inverter Signal Chain, Analog Devices

EXAMPLE CIRCUIT – DESCRIPTION

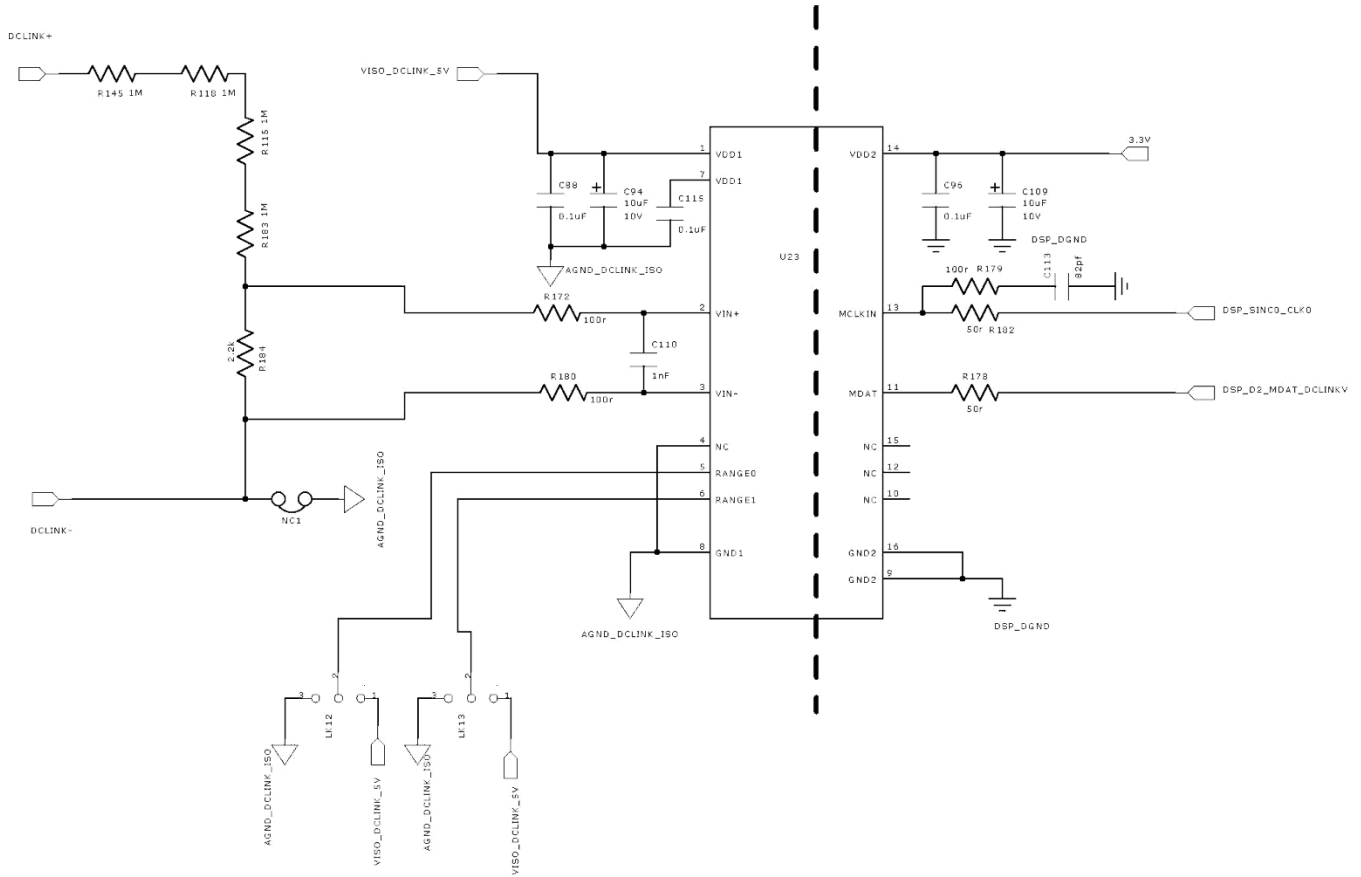


Figure 2. Isolated Voltage Circuit

The ac input to the Σ - Δ modulator is an ac sine wave representing 220 V rms from a single phase grid. There is a resistor divider to reduce the input range to that of the specified input range of the ADC. An input filter reduces noise at the inputs.

The output of the Σ - Δ modulator contains two signals: a high speed clock input from the ADSP-CM403xy DSP processor and a data signal that holds the modulated data. This data can be input directly to a sinc3 filter where the data can be directly converted to an ADC result. An example of this data is shown below.

At the lower range of the ADC the input signal has a narrow pulse width, while at the higher end of the scale the pulse width is near its maximum. When put through a sinc filter, the output data is that shown in the diagonal line. The AD7401A can operate to voltages up to 891 V unipolar range or 565 V bipolar range, across its isolation barrier: a 20 μ m polyimide. Further information on this and the various approvals can be found in the relevant data sheets.

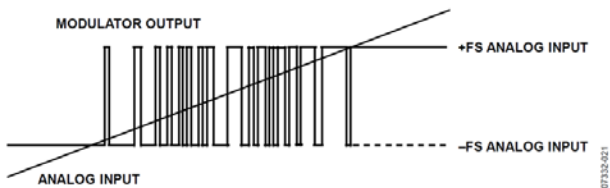


Figure 3. Modulator Example Data

ADSP-CM403XY SINC3 PERIPHERAL BLOCK

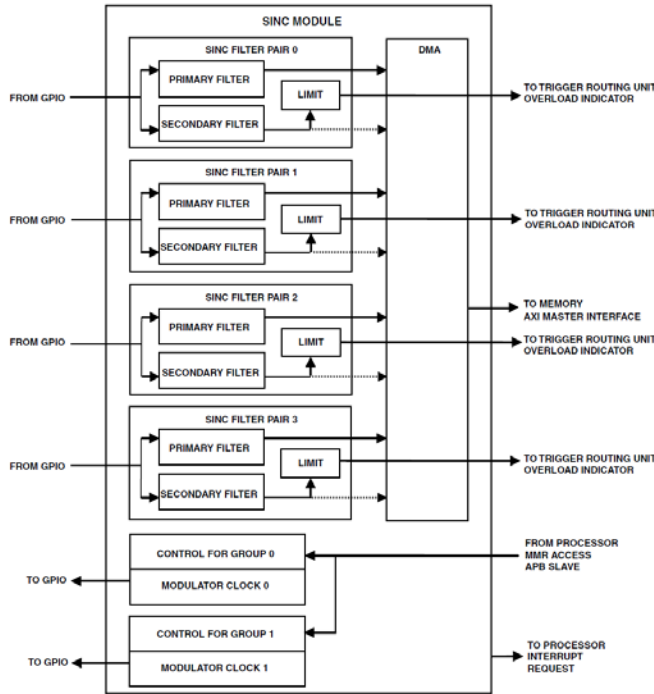


Figure 4. ADSP-CM403 Sinc Peripheral Block Diagram

The block diagram shows four sinc filter pairs (sinc0–sinc3), two modulator clock sources, and two banks of control registers (units). The module accepts four Σ - Δ bit streams from the GPIO input pins and directs two modulator clock sources to the GPIO output pins. A pulse-width modulation (PWM) signal synchronizes the modulator clocks to optimize system performance. Each sinc filter pair includes the primary filter, secondary filter, DMA interface, and overload limit detection functions. The primary sinc filter transmits its data to memory using DMA. The secondary sinc filter generates overload signals, which can be routed via the trigger routing unit (TRU) to trip a PWM modulator and generate an interrupt.

When using the AD7401A, the device is specified to a decimation rate (DR) of 256. However, it is possible to use this device at other decimation rates.

For a DR=256, the response of a sinc3 filter is shown in Figures 5a and 5b below.

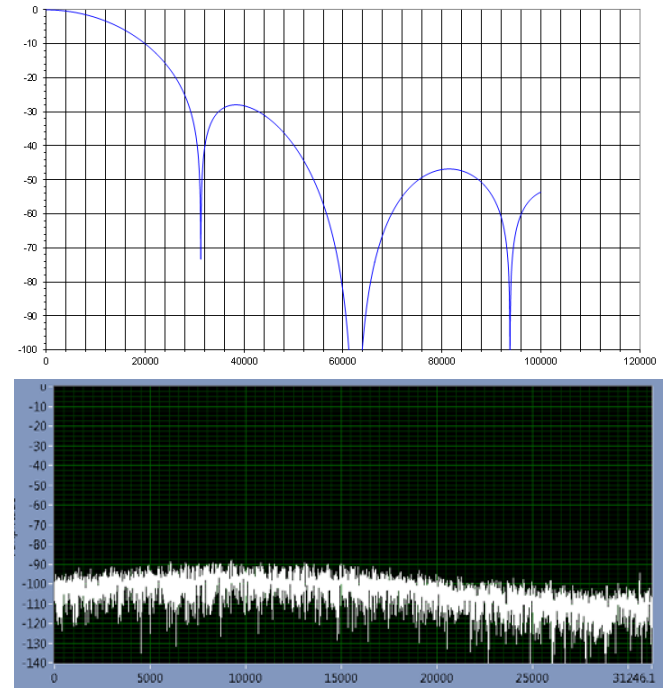


Figure 5. (a) Sinc3 Decimation Rate=256 and (b) Module Noise Floor

DIGITAL FILTER

The sinc filter has a transfer function that lends itself to an implementation in digital logic, using a series of summation and decimation functions. The filter purpose is to remove the modulator sample clock and recover a digital value of the sampled signal. The filter design matches a bipolar Σ - Δ modulator, producing a 50% pulse density for a 0 V input, over 50% for positive inputs and less than 50% for negative inputs as show in Figure 6.

The digital filter is a set of accumulators driven by the modulator clock (M_CLK), followed by a set of differentiators driven by the decimation clock (D_CLK). The input accumulators convert the input bit stream into a multibyte word, while the output differentiators derive the average one's density of the bit stream.

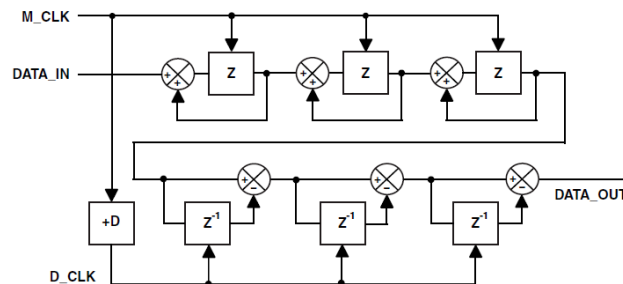


Figure 6. ADSP-CM403 Sinc Filter Block Diagram

The number of accumulator and differentiator stages can be three or four, depending on the order of the filter. The DC gain and bandwidth of the filter are functions of the filter order (O) and the decimation rate (D), which is the ratio of the modulator to the decimation clock. The transfer function of the sinc filter is generated by the product of the transfer functions for the accumulators and differentiators, and in the z domain is given by

$$H(z) = \left[\frac{1}{D} \times \frac{1 - z^{-D}}{1 - z^{-1}} \right]^O$$

ALIGNING PWM AND SINC DATA

The sinc peripheral block and the PWM are inherently running on the same system clock in the ADSP-CM403, typically 100 MHz. The PWM and the sinc can be synchronized so that the data can be available, at an appropriate time and rate that coincide with the control algorithm. This is typically aligned with the PWM level waveform. The diagram below shows an example of the timing required to use a sinc input for synchronization to

the grid. With the PWM running at 20 kHz (50 μ s), the PWM_SYNC signal (required to synchronize the PWM blocks or external PWMs from different DSPs) occurs at the center of the PWM waveform, where little switching occurs. To align the sinc data, the clock rate for the AD7401A should be set to 10.24 MHz with a decimation rate of 256 (specified in the AD7401A data sheet). This gives a resulting 16-bit word rate is of 40 KHz (50 μ s); twice that of the PWM frequency. As the sinc can also be set to align with the PWM_SYNC output, as shown in the diagram below, the sinc will now produce two data outputs every PWM period. The output words will be available, in SRAM, at the next PWM_SYNC signal. This clearly demonstrates that the sinc data can be used in grid synchronization algorithm control.

RESOURCES

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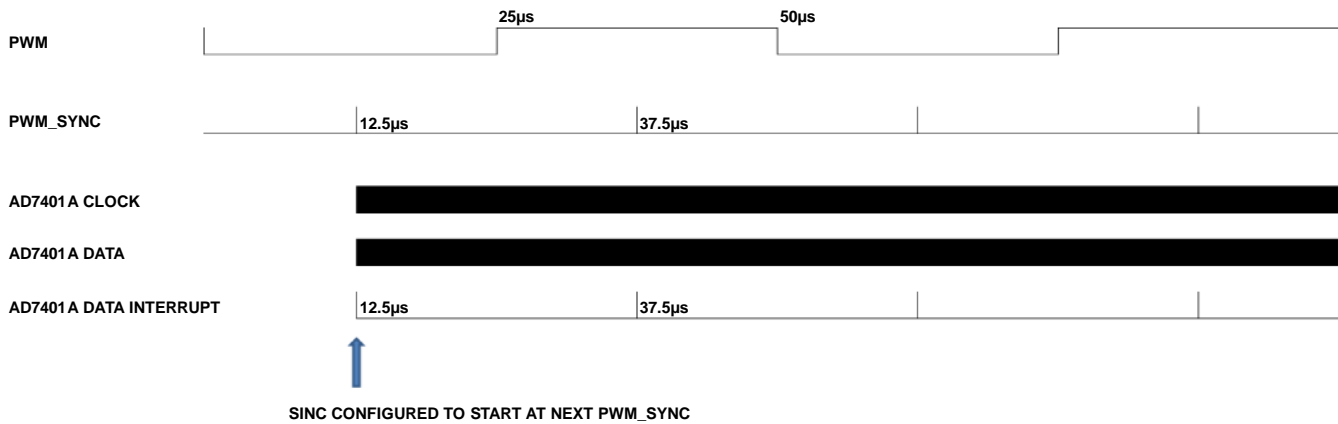


Figure 7. Alignment of PWM and Sinc Peripherals in the ADSP-CM403

PROGRAMMING EXAMPLE

```

/* SPECIFY DECIMATION RATE OPTIONS */

/* 256 */
// RESULT = ADI_SINC_SETRATECONTROL (DEV, ADI_SINC_GROUP_0, ADI_SINC_FILTER_PRIMARY, DECRATE_256, 0);
// RESULT = ADI_SINC_SETLEVELCONTROL (DEV, ADI_SINC_GROUP_0, 0, 0, SAMPLECOUNT_INTRATE, PSCALE_256); // PCINT INT RATE

/* 128 */
RESULT = ADI_SINC_SETLEVELCONTROL (DEV, ADI_SINC_GROUP_0, 0, 0, SAMPLECOUNT_INTRATE, PSCALE_128); // PCINT INT RATE
RESULT = ADI_SINC_SETRATECONTROL (DEV, ADI_SINC_GROUP_0, ADI_SINC_FILTER_PRIMARY, DECRATE_128, 0);

/* 64 */
RESULT = ADI_SINC_SETLEVELCONTROL (DEV, ADI_SINC_GROUP_0, 0, 0, SAMPLECOUNT_INTRATE, PSCALE_64); // PCINT INT RATE
RESULT = ADI_SINC_SETRATECONTROL (DEV, ADI_SINC_GROUP_0, ADI_SINC_FILTER_PRIMARY, DECRATE_64, 0);

/* SET SECONDARY RATE CONTROL */
RESULT = ADI_SINC_SETRATECONTROL (DEV, ADI_SINC_GROUP_0, ADI_SINC_FILTER_SECONDARY, 8, 0);
RESULT = ADI_SINC_SETFILTERORDER (DEV, ADI_SINC_GROUP_0, ADI_SINC_FILTER_THIRD_ORDER, ADI_SINC_FILTER_THIRD_ORDER); RESULT = ADI_SINC_SETCIRCBUFFER (DEV, ADI_SINC_GROUP_0, SINC_CIRCBUFFER, CIRC_BUF_SIZE);

/* SET OVERLOAD AMPLITUDE DETECTION LIMITS TO 0 - FULLSCALE */
RESULT = ADI_SINC_SETAMPLITUDELIMIT (DEV, ADI_SINC_PAIR_0, 0X0000, 0XFFFF);
RESULT = ADI_SINC_SETAMPLITUDELIMIT (DEV, ADI_SINC_PAIR_1, 0X0000, 0XFFFF);
RESULT = ADI_SINC_SETAMPLITUDELIMIT (DEV, ADI_SINC_PAIR_2, 0X0000, 0XFFFF);
RESULT = ADI_SINC_SETAMPLITUDELIMIT (DEV, ADI_SINC_PAIR_3, 0X0000, 0XFFFF);

/* SPECIFY MODULATOR CLOCK FREQUENCY, PHASE & STARTUP SYNCHRONIZATION */
RESULT = ADI_SINC_CONFIGMODCLOCK (DEV, ADI_SINC_GROUP_0, FSYSCLK, MODCLK, 0, FALSE); // UP TO 20MHZ

/* IT'S THE SAME CLOCK AS THE PWM - SO PWM AND SINC ARE SYNCHRONOUS */
RESULT = ADI_SINC_ENABLEMODCLOCK (DEV, ADI_SINC_GROUP_0, ADI_SINC_MOD_CLK_IMMEDIATE);

/* ASSIGN BUFFERS TO RECEIVE SINC DATA - AUTOMATICALLY DMA'D INTO SRAM IN THE ADSP-CM403*/
RESULT = ADI_SINC_SUBMITBUFFER (DEV, ADI_SINC_GROUP_0, SINC_DATA0, NUM_SAMPLES);

/* ROUTE THE TRU INTERRUPT */
RESULT = ADI_SINC_ENABLEDATAINTERRUPT (DEV, ADI_SINC_GROUP_0, ADI_SINC_DATA_INT_0, TRUE);

/* ENABLE & ASSIGN USED SINC FILTER PAIR, AND SPECIFY INTERRUPT MASKS */
RESULT = ADI_SINC_SETCONTROLINTMASK (DEV, ADI_SINC_INT_EPCNT0|ADI_SINC_INT_EFOVF0|ADI_SINC_INT_EPCNT1|ADI_SINC_INT_EFOVF1);
RESULT = ADI_SINC_ENABLEPAIR (DEV, ADI_SINC_PAIR_0, ADI_SINC_GROUP_0, TRUE); // ACV_EXTERNAL
RESULT = ADI_SINC_ENABLEPAIR (DEV, ADI_SINC_PAIR_1, ADI_SINC_GROUP_0, TRUE); // ACV_INTERNAL
RESULT = ADI_SINC_ENABLEPAIR (DEV, ADI_SINC_PAIR_2, ADI_SINC_GROUP_0, TRUE); // DC LINK
RESULT = ADI_SINC_ENABLEPAIR (DEV, ADI_SINC_PAIR_3, ADI_SINC_GROUP_0, TRUE); // AC_CURRENT

/* WAIT AND READ FULL SINE WAVE INTO SRAM - START NEAR AC CROSSOVER. */
DO
{
    PWM_SINC_LOOP=0;
    GET_ADC_DATA_PWM();
}
WHILE ((SINC_VEXT_DATA[0] > 50) || (SINC_VEXT_DATA[0] < -50)); // START SINC AT 0 V MEASUREMENT - ALIGNS WITH SINEWAVE.

```