Sequencer-Supervisor Simplifies Design of Multi-Supply Systems

by Bob Jurgilewicz

Introduction

Proper supply sequencing and supervision are key aspects of a stable multi-power-supply system, but supply specifications are often finalized near the end of the project. This puts pressure on the supervisor and sequencing components to remain versatile, even as they are built into the design.

The LTC2928 offers a solution to the problem of moving target designs by using a simple approach to sequencing and supervision—no complicated firmware or software needed. You can configure sequence and supervisor thresholds, supply sequence order and timing with just a few components. The number of sequenced and supervised supplies is unlimited—just cascade multiple LTC2928s through a single pin. System faults can shutdown all controlled supplies immediately, and application faults are detected and reported by the LTC2928, making quick work of fault diagnosis.

A Simple But Powerful Design Idea

One of the best ways to avoid expensive design rework at the back end of a project is to use the LTC2928 in generic reusable circuit blocks that are added early in the system design with little regard to the final specific power requirements. Leave blocks unfinished—simply waiting for passive component values to be determined.

Loaded with Features

Designing with the LTC2928 requires little more than specifying a few resistors, capacitors and the biasing of some three-state pins. Design flexibility however, is virtually unlimited. Table 1 outlines a few design features and configuration options available in the LTC2928.
How to Set Up the LTC2928

This section describes how to calculate the component values required to set particular supervisor and sequence parameters. The calculations are not difficult, but we recommend using the LTC2928 Configurator, a free calculation tool that does much of the work for you (see “The LTC2928 Configurator Tool Designs It for You” above). Either way, be sure to call about the available demo board, which you can use to quickly evaluate any configuration.

Figures 1 and 2 show a generic LTC2928 application and waveforms for the discussion and calculations here.

To set the supervisor undervoltage threshold at the V1 input (UV \( TH_1 \)), calculate the ratio for the resistive divider (\( R_{1B} \), \( R_{1A} \)) between supply voltage \( S_1 \) and ground:

\[
\frac{R_{1B}}{R_{1A}} = \frac{\text{UV}_{TH}(V) - 1}{0.5V}
\]

The resistive dividers for the other positive supervisor inputs are calculated in the same way.

Let the LTC2928 Configurator Tool Design It for You

Configuring an LTC2928 application is simple (see “How to Set Up the LTC2928” in this article), but why should you have to do any calculation at all? To make life truly simple, Linear Technology offers free configuration software that calculates all resistor values, capacitor values and required logic connections. The tool also generates schematics and a passive element bill-of-materials. All you need to know are your supply parameters and sequence. The LTC2928 Configurator can be obtained from LTC applications staff members.

Table 1. LTC2928 feature summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Voltage Operation: 7.2V to 16.5V</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Low Voltage Operation: 2.9V to 6V</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Power-Up and Power-Down Sequencing</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>(Positive and Negative Supplies)</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Sequenced Shutdown upon Loss of ( V_{CC} )</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>±1.5% Accurate Under Voltage Comparators</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Over Voltage Comparators</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Sequence Threshold Comparators</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Negative Supply Comparator</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
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<tr>
<td>Fault Channel and Fault Type Reporting</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
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<tr>
<td>Controller Fault</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
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<tr>
<td>Under Voltage Fault</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Over Voltage Fault</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Sequencing Fault</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
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<tr>
<td>External Fault</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Auto Restart</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>N-Channel MOSFET Gate Drive</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Power Supply Capacitance Discharge*</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>RESET Disable for Margining</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Single Pin Cascading for More Supplies and Time Positions</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Fast Shutdown at Power-Down*</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Individual Comparator Outputs</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
<tr>
<td>Adjustable Sequence, Power-Good and Reset Timers</td>
<td><img src="https://example.com/feature.png" alt="" /></td>
</tr>
</tbody>
</table>

*see data sheet

If a negative supply is monitored on the V1 input, tie the VSEL pin to \( V_{CC} \). Connect the ground side of \( R_{1A} \) to the REF pin. The reference voltage provides level shifting of the negative supply to the ground sensing comparator on the V1 input. Calculate the resistive divider ratio using:

\[
\frac{R_{1B}}{R_{1A}} = \frac{-\text{UV}_{TH}(V)}{V_{REF}}
\]

where \( V_{REF} \) is nominally 1.189 volts.

In the power supply world, undervoltage thresholds are commonly discussed as a percentage below the nominal supply voltage. The same is true for the LTC2928, but all other thresholds in the LTC2928 (sequence-up, sequence-down and overvoltage) are keyed to the configured undervoltage thresholds on each respective input, and are expressed as a percentage of the undervoltage threshold. A bias on the OVA pin globally configures the overvoltage threshold for all positive supplies. Use a resistor to ground to configure overvoltage thresholds in the range of 12% to 32% above the undervoltage threshold. Use a resistor to \( V_{CC} \) for overvoltage thresholds greater than 32% above the undervoltage threshold. Use Figures 3 and 4 to select the OVA biasing resistor.

Typically, a single resistor (\( RT_n \)) sets the power supply’s sequencing time position. The normal sequence-down order is the reverse of the sequence-up order, and order is preserved regardless of the number of cascaded LTC2928 devices. The sequence up/down time positions can also be actively changed—see “Active Sequence
Positioning below. In this generic application, supply S1 is shown to start in time position 5 (TP5). Time position resistor RT1 is connected between $V_{CC}$ and the RT1 input pin. Time position resistors and the corresponding ideal time position voltages are given in Table 2. To configure time position 5 for supply S1, a 9.53kΩ resistor is selected. Time positions 6, 7 and 8 are similarly selected with RT resistors for supplies S2, S3 and S4.

Any sequencer/supervisor channel that must be shut off or is otherwise unused may be disabled by pulling the corresponding RT pin low (ground). Prior to sequencing-up, with the ON pin low, any or all enable pins may be forced high by pulling the respective RT pin to $V_{CC}$. In this manner, supplies may be tested individually or together in any combination.

Transition the ON pin to begin sequencing-up or down. The shortest time delay between two time positions (TP2~TP1 for this example) or the time delay between an ON pin transition and the next time position is defined to be equal to $t_{STMR}$ (sequence timer delay). The time between two adjacent time positions is potentially stretched by a power supply’s rise time to its configured sequence-up threshold. In Figure 2, supply S1 has a finite rise time $t_{RISE}(S1)$ to the sequence-up threshold $S_QT1$. Using three-state pins $S_QT1$ and $S_QT2$ (not shown), sequence-up thresholds can be set to equal to 100%, 67% or 33% of the configured undervoltage threshold.

The PTMR pin configures the power-good timer which is used as a watchdog for stalled power supplies. When sequencing-up, a sequence fault is generated if any sequenced supply fails to reach its undervoltage threshold during the power-good time-out period. When sequencing-down, a sequence fault is generated if any sequenced supply fails to reach its sequence-down threshold during the power-good time-out period. The power-good timer starts with the first enabled (disabled) supply and is terminated when the last supply reaches its undervoltage threshold (sequence-down threshold). The power-good timeout period is set with capacitor $C_{PTMR}$ and is calculated from

$$C_{PTMR}(F) = \frac{t_{PTMR}(s)}{4.0\text{M}\Omega}$$

$$C_{STMR}(F) = \frac{t_{STMR}(s)}{8.67\text{M}\Omega}$$

To disable the power-good timer, simply tie the PTMR pin to ground. To avoid generating sequence faults due to insufficient power-good timer period, be careful to add some time...
margin to the minimum recommended power-good timeout period. The minimum recommended time consists of the time difference between the first and last enabled (disabled) supplies added to the sum of supply rise (fall) times. The minimum recommended power-good timeout is given by

\[ t_{PTMR}^{\text{min}} = \left[ TP^{\text{max}} - TP^{\text{min}} \right] \times t_{\text{STM}} + \sum_{n=1}^{4} \max\left( t_{\text{rise}}(Sn), t_{\text{fall}}(Sn) \right) \]

In this example, with the simplifying assumption of equal rise and fall times for all four supplies, the minimum recommended power-good timeout period reduces to

\[ t_{PTMR}^{\text{min}} = \left[ 8 - 4 \right] \times t_{\text{STM}} + 4 \times t_{\text{rise}} \]

\[ = 4 \times t_{\text{STM}} + 4 \times t_{\text{rise}} \]

Again, adding some additional time margin to this minimum time is helpful to avoid bogus sequence faults. Details regarding the biasing (high, low or open) of the three-state configuration pins (MS1, MS2, SQT1, SQT2, RDIS) are discussed in the LTC2928 data sheet.

**Active Sequence Positioning**

In most sequencing applications, the sequence-down order is the reverse of the sequence-up order. While the LTC2928 easily handles such applications, it is not limited to same up, same down sequencing. Two methods are available to obtain flexible sequencing order. The first technique uses a simple analog multiplexer to switch the resistance seen at the RT pin(s). The second technique uses a rail-to-rail voltage output DAC, preferably with

\[ \text{I}^{2}\text{C} \]

interface, such as the LTC2629, to directly drive a programmed voltage to the RT pin(s). Both methods require changing the voltage (\( V_{\text{RT}} \)) seen at the RT pin(s), subject to the error bound specified in Table 2. The RT pin input resistance is nominally 12k.

Figure 5 shows how a simple analog multiplexer is connected to allow a different sequence position on the basis of the DONE signal. During sequencing-up, the DONE pin is high, so RT1\text{UP} is selected. When sequencing-up is complete, DONE pulls low and RT1\text{DN} is selected. Sequencing-down commences once the ON pin is pulled low.

Table 2. Sequence time position resistors

<table>
<thead>
<tr>
<th>Position Number</th>
<th>( R_{T} ) (kΩ)</th>
<th>Ideal ( R_{T} ) Pin Set Point (( V_{\text{RT}} / V_{\text{CC}} ) ±0.005)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>95.3</td>
<td>1/9 = 0.111</td>
</tr>
<tr>
<td>2</td>
<td>42.2</td>
<td>2/9 = 0.222</td>
</tr>
<tr>
<td>3</td>
<td>24.3</td>
<td>3/9 = 0.333</td>
</tr>
<tr>
<td>4</td>
<td>15.0</td>
<td>4/9 = 0.444</td>
</tr>
<tr>
<td>5</td>
<td>9.53</td>
<td>5/9 = 0.556</td>
</tr>
<tr>
<td>6</td>
<td>6.04</td>
<td>6/9 = 0.667</td>
</tr>
<tr>
<td>7</td>
<td>3.40</td>
<td>7/9 = 0.778</td>
</tr>
<tr>
<td>8</td>
<td>1.50</td>
<td>8/9 = 0.889</td>
</tr>
</tbody>
</table>

Figure 6 demonstrates how the low-power LTC2629 ratiometric voltage output DAC can be used in place of resistors to actively program sequence positions. The LTC2629 uses a 2-wire \( \text{I}^{2}\text{C} \) compatible serial interface and is available in a tiny 16-lead SSOP package. Supply range and output drive capability are compatible with the LTC2928. Most importantly, the LTC2629 incorporates a power-on reset circuit that forces the outputs to zero scale until a valid write and update take place. This feature prevents

*continued on page 12*
is shown in Figure 5. The most flexible
turn-on behavior is afforded by the ON
register. For this the ON pin should
be set low. Now when BD_SEL# goes
low the switches remain off. The ON
register has four bits to control the
state of each supply switch. Writing
a one to any of these bits turns on
that particular switch. In this way
a host controller can turn on the
supplies in any desired sequence or
combination.

Extensive Fault Information
Aids Diagnosis
If a board fault occurs, diagnosing the
problem is simplified by checking the
LTC4245’s onboard fault information.
One status and two fault registers
contain a record of faults that are
present or have occurred.

The STATUS register reports if
any supply is in an undervoltage or
power bad state and if any switch is
potentially shorted. It also indicates
the state of the SS, PCI_RST#, LO-
CAL_PCI_RST#, BD_SEL# pins and
the ADC. The fault registers log any
faults that have occurred but may no
longer be present. Individual bits re-
cord input undervoltage, output power
bad and overcurrent faults on each
supply. Each of these faults has an
auto-retry bit in the CONTROL register.
If a fault occurs and its auto-retry bit
is set, then once the fault is removed
the LTC4245 turns on the external
switches automatically. Otherwise the
switches are latched off until the fault
bit is cleared.

Another 8-bit register called the
ALERT register controls whether
the occurrence of a particular kind
of fault triggers the LTC4245 to pull
the ALERT# pin low. This can be
used to interrupt a host controller in
real-time so it can query the LTC4245
register information and take appro-
priate remedial action. When multiple
LTC4245s are present in a system, the
SMBus Alert Response Protocol can
be used to find the faulting LTC4245.
The default behavior is to not pull
ALERT# low for any fault.

Flexible Supply Configuration
The CFG pin on the LTC4245 can be
used to deal with applications that
do not utilize a −12V supply, or use
another 3.3V supply instead of 5V. In
a normal CPCI application the CFG
pin is tied low. When the −12V supply
is absent, the CFG pin is left uncon-
ected. In this case, the LTC4245
disables the undervoltage lockout
and power bad comparators on −12V, thus
allowing 12V, 5V and 3.3V to power-
up. By tying the CFG pin to INTV, CC,
not only is the −12V undervoltage and
power bad ignored but 5V thresholds
change to 3.3V levels.

Figure 6 shows the LTC4245 on a
PCI Express backplane controlling one
12V and two 3.3V supplies. The VEE
pins are all tied to ground. PRST#1
and PRST#2 signals sense when the
plug-in card is seated. These signals
are used by the PCI Express Hot-Plug
Controller to command the LTC4245 to
turn the switches on and off. Figures
7 and 8 show the LTC4245 controlling
just two supplies, one of them 12V, the
other being either 3.3V or 5V.

Conclusion
The LTC4245 packs a 4-supply Hot
Swap controller, ADC, PCI interface
and numerous other features into a
5mm × 7mm QFN package, simplify-
ing the task of inrush control, fault
isolation and power monitoring on
a plug-in board. The simple default
behavior can be customized through
onboard registers. It provides a
space-saving Hot Swap solution for
any high-availability system utilizing
multiple supplies such as CompactPCI
or PCI Express.