

# MONOLITHIC DIGITALLY PROGRAMMABLE DELAY GENERATOR

## AD9500 Converts an 8-Bit Digital Input to an Output Time Interval FS Range Is from 2.5 ns (with 10-ps Resolution) to 100 $\mu$ s And More

The AD9500 Programmable Delay Generator\* receives a digital *trigger* pulse and outputs a signal after a specified delay period, as programmed by an 8-bit digital input. The full-scale delay range is flexible, ranging from a few nanoseconds to more than 100  $\mu$ s; it is set by an externally connected R-C combination. Compact, low-cost single-chip digitally programmable delays have immediate practical applications in test systems: eliminating signal skews in high-speed systems, measuring unknown delays, and constructing programmable ring oscillators.

Figure 1 shows the various functions within the AD9500. The key functions are the reference and the timing-control circuit—which form an analog integrator; an 8-bit d/a converter, set by the 8-bit digital control input; and a high-speed precision comparator with complementary ECL outputs. Inputs are differential *trigger* and *reset* signals, which may also be used with single-ended inputs. The maximum triggering rate is 100 MHz.

### HOW IT WORKS

The *trigger* and *reset* inputs are designed primarily for ECL signal levels, but they can function with analog and TTL input levels. An on-board reference midpoint allows both of the inputs to be driven by either single-ended or differential ECL circuits.

As the timing diagram in Figure 2 shows, the delay is initiated when the trigger input goes *high*. The integrator generates a downgoing ramp; when it crosses a level established by the 8-bit DAC, the comparator output changes state, producing the delayed outputs, Q and  $\bar{Q}$ . A parallel  $\bar{Q}_R$  output circuit is available for uses where the AD9500 drives its own *reset*.

Its delay is equal to the programmed delay,  $t_D$ —a function of the selectable RC time constant (Figure 3) and the precision threshold set by the DAC—plus a propagation delay ( $t_{PD} = 7.4$  ns max with a 5-ns full-scale input).

$$\begin{aligned} \text{Total delay} &= t_{PD} + t_D \\ &= t_{PD} + \frac{\text{digital value}}{256} R_{SET} (C_{EXT} + 10 \text{ pF}) \end{aligned}$$

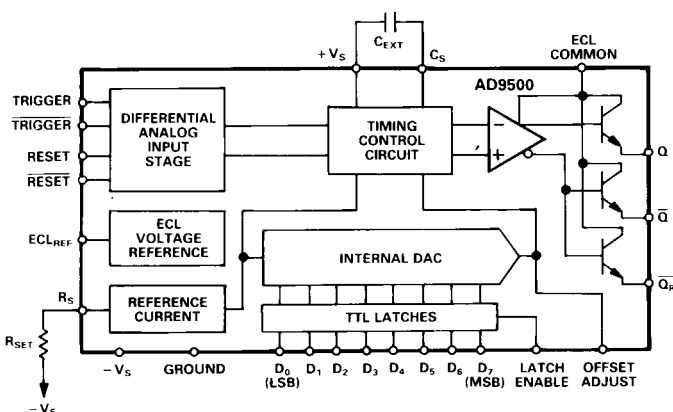
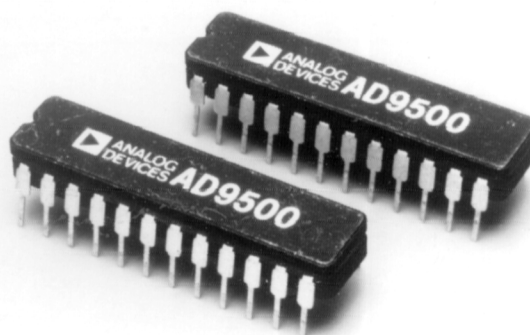


Figure 1. Block diagram of the AD9500.



**Reset:** A pulse of appropriate width applied at the Reset input resets the integrator and the Q outputs to prepare the device for the next trigger. At the end of the reset propagation delay ( $t_{RD}$ , approximately equal to  $t_{PD}$ ), Q returns to its original state; 0.2 ns after the Reset input goes low, the device is ready for the next trigger. A *reset* interval,  $t_{LRS}$ , should be allowed for the linear ramp to return and settle to its original level.

When  $C_{EXT} = 0$ , and  $R_{SET} = 250 \Omega$ , the full-scale programmed delay time is 2.5 ns, and the LSB (one increment of delay) is  $2,500 \text{ ps}/256 \approx 10 \text{ ps}$ , which is also the typical jitter level; this establishes the basic delay-time resolution.

The digital control data is passed to the AD9500 via a transparent latch, controlled by the *latch enable* signal. In the transparent mode, the DAC follows changes at the inputs; the *latch enable* signal is used to strobe the digital data into the AD9500's latches.

Because the DAC has fast response, the programmed delay may in principle be updated in the same time frame as the signals being

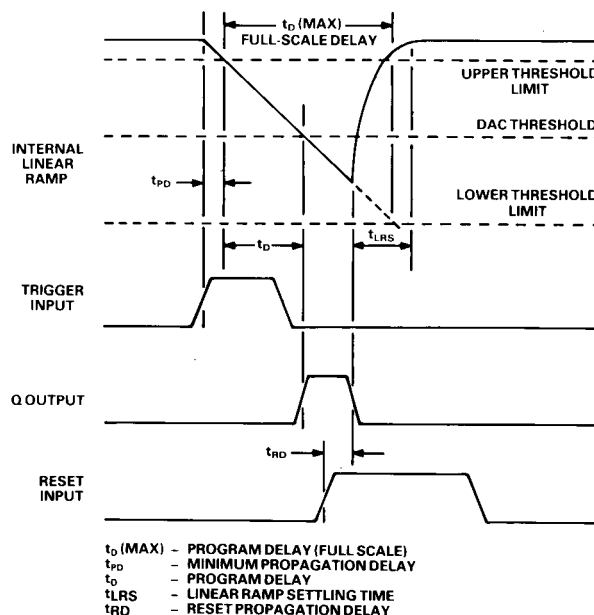


Figure 2. Timing diagram.

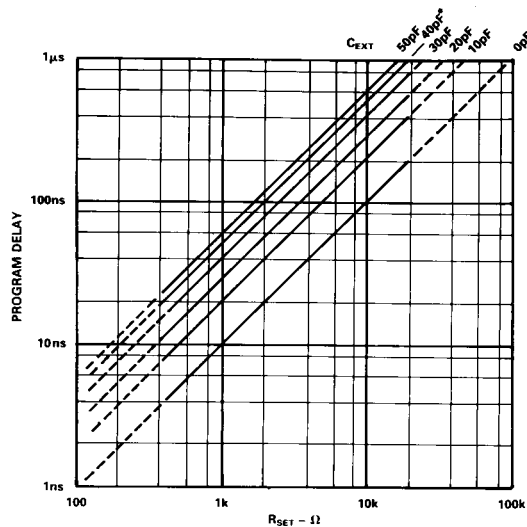


Figure 3. Typical values of programmed delay ranges as a function of resistance and capacitance.

delayed. However, the next trigger should wait for the DAC to settle, typically 29 ns after latching in a new value.

The AD9500's programmed time delay is linear to within 1 LSB maximum integral nonlinearity with  $\geq 100$ -ns full-scale input, with 1/2-LSB max differential nonlinearity; monotonicity is guaranteed over the full specified operating temperature range. 312mW of power is drawn from the +5-V and -5.2-V supplies.

Devices are graded to operate from -25 to +85°C (B grades) and -55 to +125°C (T grades). Except for operating temperature range, all grades have identical electrical specs. Available packages include 28-pin PLCC (P) and LCC (E) packages and 24-pin ceramic "skinny" DIPs (Q). Prices in 100s start at \$16.00.

### APPLICATIONS

**Multichannel Deskewing:** A highly effective use of the AD9500 is in multiple delay-matching applications. For example, in a high-speed, high-pin-count logic tester, slight differences in impedance and cable length can create large timing skews. The high speed of modern test systems makes timing accuracy particularly important, and the large number of driver lines (e.g., 128 driver lines with switching capabilities in excess of 100 MHz) requires the use of compensating circuitry. In practice, each signal line would drive an AD9500; its output would drive a logic test-head line (Figure 4). With one line as a standard, the programmed delays of the others are adjusted to eliminate the timing skews.

With the very fine timing adjustments possible from the AD9500 (as small as 10 ps), nearly any high-speed system should be able to

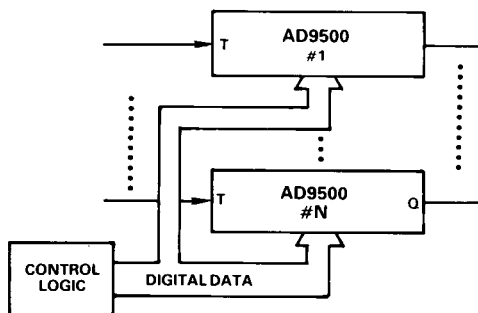


Figure 4. Multiple delay matching.

adjust itself automatically to within very tight tolerances.

**Measuring Unknown Delays:** Two AD9500s can measure delays precisely (Figure 5). One is set with little or no programmed delay; its output drives the unknown-delay circuit, which in turn drives the input of the "D"-type flip-flop. The second AD9500 drives the clock input of the flip-flop. With both triggered together repetitively, the programmed delay of the second unit is varied to detect the output edge from the unknown delay.

Detecting the output edge is straightforward. If the programmed delay through the second AD9500 is too long, the flip-flop output will be at logic high—if too short, at logic low. When the unknown is very closely matched, the flip-flop's output will bounce between high and low. The digital code value used to create the second programmed delay is a direct indication of the delay through the unknown circuit. Best results are achieved by calibrating the system with the unknown delay removed.

**Programmable Oscillator:** A digitally programmed oscillator for frequencies up to 67 MHz is an interesting use of the AD9500. The high-precision delays it generates can be exploited to create a ring oscillator with variable duty cycle (Figure 6). The delayed output of the first AD9500 is used to drive the trigger input of the second unit; the output of the second, in turn, drives the trigger

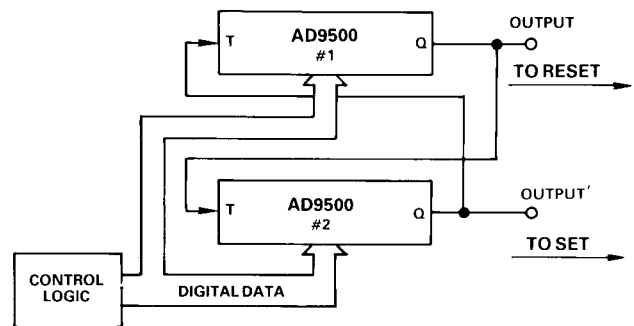


Figure 5. Programmable oscillator.

input of the first. Together, the devices will alternately trigger one another, creating two pulse chains on their outputs.

The total delay through both AD9500s determines the period of the oscillation. The duty cycle can be controlled by using the outputs to drive the set and reset inputs of a flip-flop. The delay through the first AD9500 controls the flip-flop logic low output pulsewidth; the second controls the logic high pulsewidth.

*The AD9500 was designed by Jeff Barrow at ADI's Computer Labs Division, in Greensboro NC. Critical portions of this circuit are covered by U.S. Patents 4,742,331 (Jeff Barrow and A. Paul Brokaw) and 4,349,811 (A. Paul Brokaw). ▀*

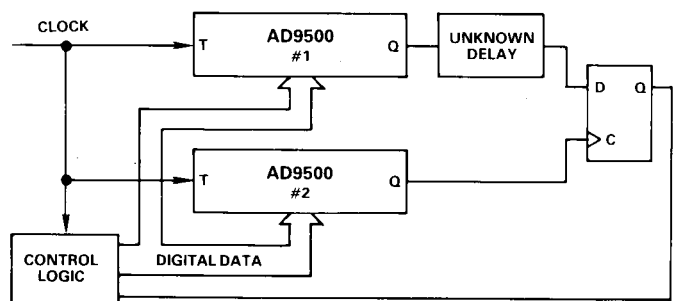


Figure 6. Measuring unknown delays.