

LEVEL-INDEPENDENT AUTOMATIC GAIN CONTROL

LOGDAC™ Controls Output Signal Amplitude Over Wide Range of Input

AD7111 Resolves to 0.375 dB, Provides Digital Readout of Input Level

by John Wynne

Figure 1 shows the essential components of a basic automatic gain-control (AGC) loop: the dc reference signal, V_{REF} , establishes the output amplitude set-point; the output-measurement circuit obtains a running measure of the output level, based on a property (peak, average, rms, etc.) of the output signal; a comparator, derives a control signal; and a gain-adjustment circuit, applies enough distortionless gain or attenuation to the input signal to maintain the output level sufficiently close to the reference value.

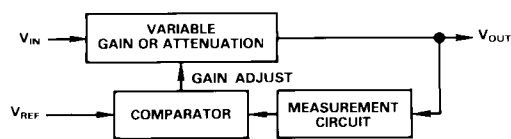


Figure 1. Automatic-gain-control loop.

The circuit examples shown here were designed to control output amplitudes for more than 40 dB of input range, for signal frequencies to beyond 20 kHz. Two cases are shown: in one, the input signal arrives at a higher level than the required output and must be attenuated; in the other, a low-level signal requires gain.

AGC WITH LOGDACs

The LOGDAC™ is a class of multiplying digital-to-analog converter that accepts bipolar analog input signals and provides an exponential (antilog) relationship between the digital input and the analog gain (or attenuation). For example, the AD7111* has an 8-bit μ P-compatible digital input, with resolution of 0.375 dB per bit and a dynamic range of up to 88.5 dB of attenuation.

Among their many applications, logarithmic DACs are useful in automatic level control applications employing multiplying DACs. The salient features that make them desirable include their wide dynamic range and their equal-percentage-per-bit gain change. For example, when the input code of a *linear* 8-bit DAC changes by 1 bit near full scale, the fractional gain change is of the order of $1/250$, and when the code changes by 1 bit near zero, the percentage gain change is of the order of 100%; on the other hand, the nominal gain change of an AD7111 over the active range of digital input is a fixed 0.375 dB—or 4.4% of reading—per bit.

In Figure 2, an AD7111 controls the attenuation for applications in which the input is at a high level compared to the output. With op amp A1, the regulator output amplifier, the AD7111 produces whatever attenuation of the analog signal input is required to maintain the output level. The digital input is increased or decreased, one 0.375-dB step at a time, by an 8-bit up/down counter. The counter, pulsed by a clock, is driven in the appropriate direction by the output of a comparator, A6, which compares the reference voltage with an amplified (A2), peak-rectified (A3) version of the measured output voltage. The window comparator, A4 & A5, provides hysteresis, so that counting is inhibited when the output level is within a defined range of values.

*RMS could also be employed, with excellent results, using the AD636 RMS-to-DC Converter.

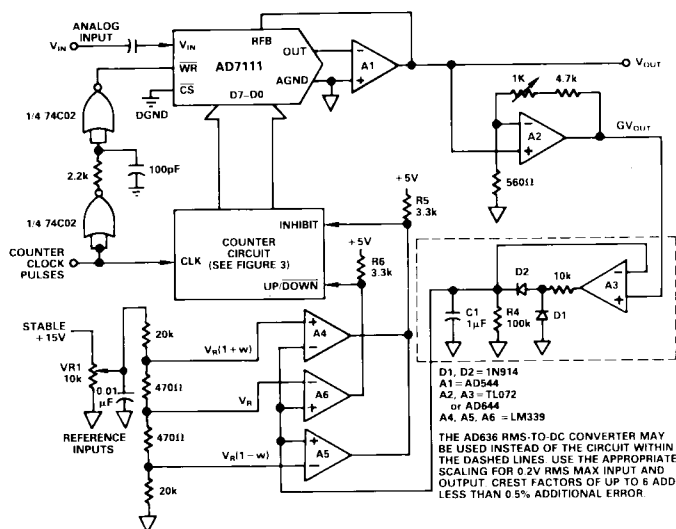


Figure 2. AGC loop using AD7111 for attenuation.

For the application shown here, the nominal output level is about 100 mV peak-to-peak. A2 provides amplification of the signal, about 10X, before it is peak-rectified. The reason for amplification is that the ripple content of the peak-detector output is not a constant percentage of signal amplitude—lower signal levels are accompanied by higher percentage ripple, which can lead to poor regulation when the input to the rectifier is well below 0.5V peak. V_{REF} should be scaled by the same amount as the closed-loop gain of A2. Thus, if A2's closed-loop gain is 10, V_{REF} should be 0.5V for a 50-mV peak output level. The input should be either ac-coupled, as shown, or symmetric about zero, to avoid the possibility of an input bias driving the peak-follower negative.

The output of the peak follower is compared with V_{REF} in A6, and with $V_{REF}(1 + W)$ and $V_{REF}(1 - W)$ in A4 and A5. The counter (Figure 3) will count down if the rectified voltage is less than V_{REF} , decreasing the AD7111's attenuation—and up if greater, to increase attenuation. If the rectified voltage is within about $\pm W$ of

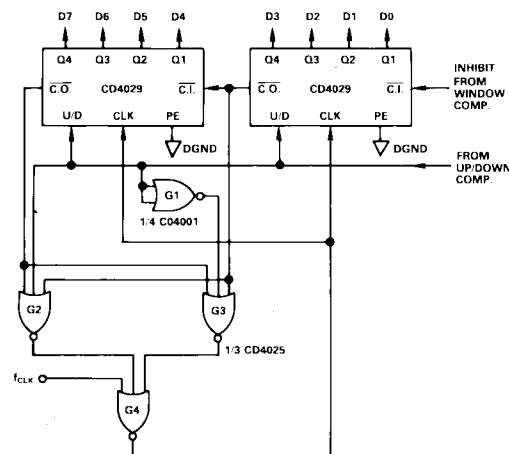


Figure 3. Counter circuit for Figures 1 and 4.

V_{REF} , the count will be inhibited, in order to provide sufficient hysteresis to avoid a ± 1 -bit high-frequency “hunting” of the amplitude. In this example, W is about 2.3%.

Figure 4 is a plot of response at selected frequencies from 100 Hz to 20 kHz for a sine wave input from 0 dB to +40 dB, relative to the output level, which corresponds to 100 mV peak-to-peak. Note the flat response over the whole range of amplitudes. There is some variation with frequency (not a problem at fixed carrier frequencies) due to the rectifier’s dynamic response characteristics.

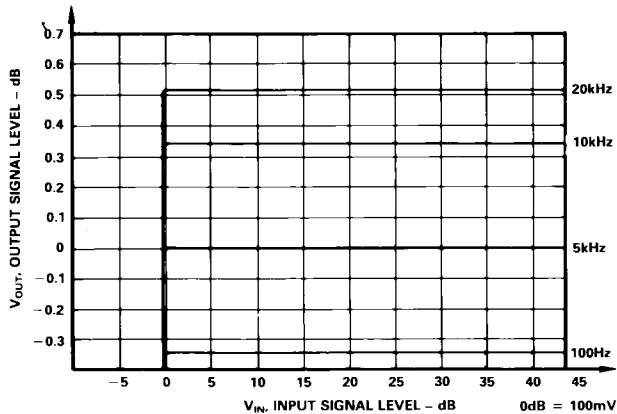


Figure 4. Response characteristics of circuit of Figure 2.

Figure 5 shows the corresponding circuit employed for applications in which the input is low and must be amplified to reach the desired output level. The AD7111 is connected to attenuate the feedback around A1, thus providing overall gain. An increasing digital input to the AD7111 will cause the feedback attenuation to increase, thus increasing the overall gain in 0.375-dB-per-bit steps. Since the output level is sufficiently high for good results with the peak detector, the scaling amplifier (A2 in Figure 1) is omitted. Thus, for 6.5 volts peak-to-peak, V_{REF} is 3.25 V.

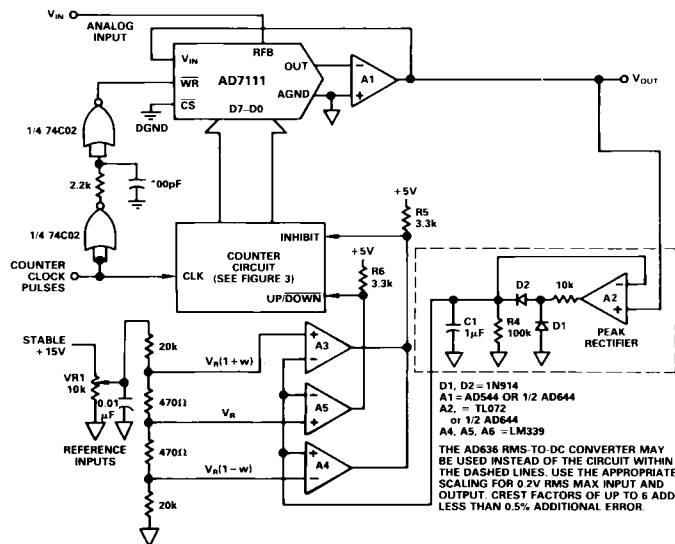


Figure 5. AGC loop using AD7111 for gain.

The response of this circuit, for an input sine wave of amplitude from 0 to -40 dB, referred to the output, is similar to that shown in Figure 4. Figure 6 shows the transient response of the circuit of Figure 5 to $+6$ and -6 -dB steps (50% amplitude changes) of a 1-kHz input signal. Settling occurs within about 130 milliseconds, using a 125-Hz clock frequency for the counter circuit. (At 125 Hz,

the pulse period is 8 ms, and at 0.375 dB per step, 16 steps are required to reach 6 dB. The count stops when the *inhibit* band is reached.)

The response of the system is determined by the relation between the frequency of the clock used for the up/down counter and the lowest expected fundamental signal frequency. The lower that signal frequency, the longer the filter discharge time-constant must be, in order for the ripple to be kept within the comparator window between signal peaks. Then, if the clock frequency is too high, a step increase in the signal level will result in an undershoot of the regulated response. The reason? Although the output responds immediately to the input and the gain control, the peak-follower output that is fed back responds quickly to increases but decays slowly on decreases—one or more additional clock cycles may occur before the reference level is reached, temporarily allowing the actual amplitude to be brought below its final value. A useful rule of thumb: establish a clock frequency from $1\times$ to $2\times$ the lowest signal frequency.

If the input can be both larger and smaller than the output, the regulating circuit must be able to provide both amplification and attenuation. This is achieved by increasing the gain of A2 in Figure 1 by an amount equal to the lowest value of the minimum signal level (in dB, referred to the output). For example, if the input signal is expected to swing from -10 dB to $+20$ dB, referred to the output, then the gain of A2 should be increased by 10 dB to insure that the AGC loop is active over the entire input signal swing.

A/D CONVERSION

While performing their AGC function, these circuits also act as tracking analog-to-digital converters, since the varying digital code present at the counter output (AD7111 input) represents a logarithmic measure of the ratio between the analog input and output levels (i.e., the attenuation or gain required for correction). This output may be used for any digital purpose (storage, computation, etc.) or for driving slaved AD7111s to set gains elsewhere in the system in proportion to changes in the analog input.

Since the AD7111 has on-chip registers, the digital code can be latched, freezing the gain of the system. This can be vital in applications where the input signal may disappear altogether, e.g., due to excessive fading or an interruption in the signal path. In many AGC systems, when this happens, the gain of the loop will increase to maximum, which can result in system oscillation when the input signal is restored. The digital control word (Figure 1 or Figure 4) can be frozen by bringing \overline{CS} (Chip Select) high. In such applications, \overline{CS} can be driven by a suitable input signal detector, set to detect out-of-range input signals. ▀

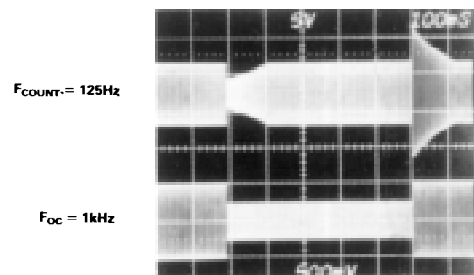


Figure 6. Response of circuit of Figure 5 to ± 6 -dB input changes.