

# TESTING A/D CONVERTERS AUTOMATICALLY

## How the LTS-2010 Tests High-Performance ADCs

### Test Routines are Downloaded to a Smart Family Board

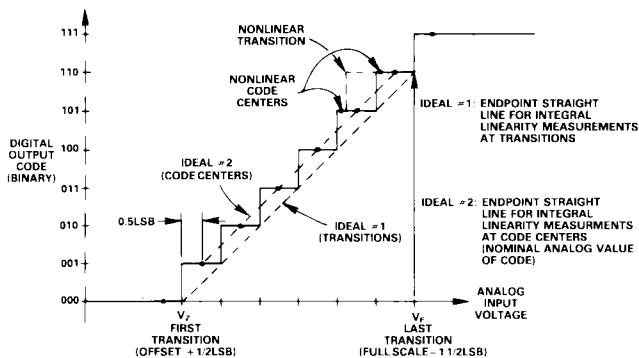
by Tim Wilhelm

Testing a/d converters for linearity—a key specification—is a lengthy and difficult procedure because each of the  $2^n$  output codes could be produced by a continuum of analog input values. Although only the two values bounding each code (the *transitions*) are of interest for each test (Figure 1a), they are not known *a priori* or directly measurable; they must be found by some sort of search requiring a series of discrete conversions.

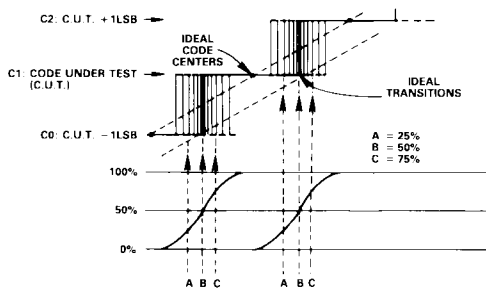
This process must be repeated for as many codes as are necessary to insure that all the significant linearity errors have been found. In addition, one group of conversions may establish transition values that are significantly different from those found in subsequent repetitions of the test, due to noise, drifts, and dynamic errors in conversion (Figure 1b). To eliminate this as a problem, the measurements must be repeated a sufficient number of times to provide an adequate statistical evaluation of the errors.



If automated high-speed ADC testing, with recorded test data, is needed, using a standard bench-top test system, such as the LTS-2010, the most productive techniques are those based on the use of slave microprocessors to operate and control tests and perform calculations. Test data can be easily produced in suitable form, whether pass/fail or as a datalogged list of the errors at all codes, with appropriate statistical parameters. The Analog Devices LTS-2010 Linear Test System's A/D-Conversion Family Board,\* employing a 16-bit TMS9900, tests a/d converters, including high-performance (12-bit, 5-50 $\mu$ s successive-approximation) types, for a wide range of parameters, including offset, gain, and linearity errors, rapidly and by fully automatic means.† This note discusses the approach to determining the key parameters of linearity error and transition uncertainty.



1a. Output vs. input for a 3-bit converter, showing ideal transitions and code centers.



1b. The transition as a probability function.

Figure 1. A/D converter output staircase.

To speed up evaluation of data, the most widely used benchtop approaches involve repeated conversions of a fixed voltage summed with a 2-bit slow dither, and inspection of the "stepstool" figure produced by an oscilloscopic expanded crossplot of the decoded output variations vs. the input dither. Individual code widths, their variations, and transition noise are easily seen in plots of this kind, but the technique calls for time, technical knowhow, and the unique integrating ability of the human visual function.

### FINDING TRANSITIONS

Transition locations are the key to measuring converter performance. Transition voltage (for a voltage-input converter) is defined as that input voltage which has equal probability of producing either of the adjacent existing codes. The nominal analog value corresponding to the digital code produced by any analog input value in the range between a pair of transitions is defined by the midpoint of the range. If the transitions are known, the midpoint can be computed easily and automatically, as can differential and integral linearity errors.

The tests (except for device calibration) are normalized to the ADC's output range, by measuring the first ( $V_T$ ) and last ( $V_F$ ) transitions and dividing the total interval by the number of codes between them, i.e.,  $(V_F - V_T)/(2^n - 2)$ , to establish the magnitude of the ideal LSB value.

Figures 2 and 3 illustrates an automated means of finding a transition. A 16-bit DAC feeds an accurately known voltage, corresponding to the ideal value for the transition between a given pair

†For example, an optional software package exists to thoroughly test 5200 and 5210 Series 12-bit a/d converters to subgroups 1 and 4 of the JEDEC 38510 slash sheet.

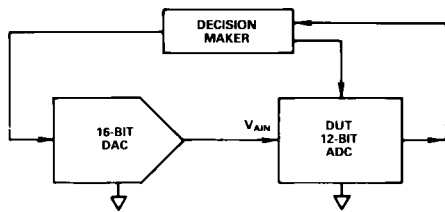


Figure 2. 16-bit DAC as a forcing input for an ADC under test in a feedback loop.

of codes, into a 12-bit ADC under test. A conversion is performed (A), and the “decision maker” checks the resulting output code of the ADC-under-test (DUT) to determine whether it corresponds to a voltage below or above the ideal transition (in this case, the low-side transition—LST). If it is below, the DAC output is incremented by 1 LSB (of the DUT’s resolution), and a new conversion and comparison (B) are performed (if it were above, the DAC output would be decremented by 1 LSB).

As Figure 3 shows, if the voltage is still below the transition, the DAC output is again incremented by 1 LSB and the cycle is repeated (C). When the code is eventually identified as above the transition (for a linear DAC, this would happen on the first trial), the DAC output is decremented by 1/2 LSB, and the cycle is repeated (D). After several conversions (E,F,G), with successively smaller DAC-output increments or decrements—as appropriate, in the manner of successive approximations—the analog value of the DAC output is within 0.06 LSB (1/16 of 1 LSB) of the actual transition voltage, and the input to the DAC is the corresponding digital code, to 16 bits ± 1 count.

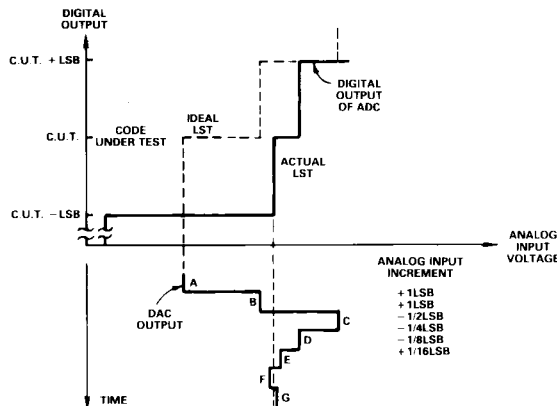


Figure 3. Finding the transition by tracking and successive approximations.

To correct for variations in the transition produced by noise, a number of readings of the transition voltage are taken and averaged. However, it is unnecessary to start from the theoretical transition; since the value obtained by the above procedure is presumably close to any other likely reading of the transition voltage, it is used as the starting point for determining the next value. The same kind of search is used, except that the initial constant increment (or decrement) is 1/4 LSB until the transition has been crossed, then successive approximations are used for subsequent conversions, until the DAC output is again within 0.06 LSB of the transition. This value is the starting point for the next search, etc. After the desired number of values,  $m$ , have been found, they are summed and divided by  $m$  to determine the average transition value.

For flexibility, the scheme actually used in the LTS-2010 employs a 12-bit main DAC calibrated to 16-bit accuracy and a 12-bit “Dither DAC” (Figure 4), with 100:1 or 500:1 (or user-arbitrary)

attenuated output. The ideal transition code is set in the main DAC; and the dither DAC is set for a bipolar output contribution in increments of 1/2-LSB of the DUT (instead of 1 LSB increments, as above), followed by successive approximations of 1/4, 1/8, 1/16, and 1/32 LSB, for a final resolution to within 0.03 LSB (at 100:1, 3 counts of the Dither DAC, in this case).

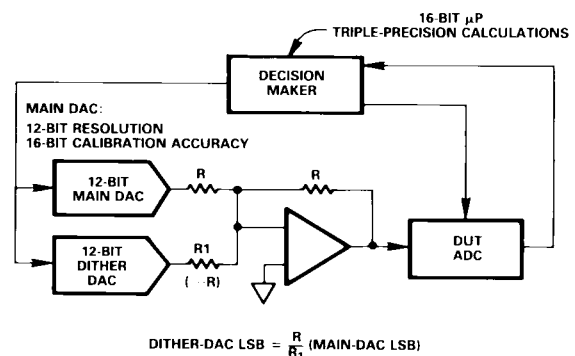
## LINEARITY TESTING

A code is tested for differential linearity by comparing its width (between two adjacent transitions) with  $1/(2^n - 2)$  of the voltage between the first and last transitions. If the code is missed, its width will be zero, since its transitions, in effect, coincide. The code is tested for integral linearity by comparing its low-side transition (LST) with the calculated LST (on locus “Ideal 1” in Figure 1a), or by comparing its center (half the sum of the adjacent transitions) with the LST + 1/2 LSB (locus “Ideal 2”).

ADC linearity tests typically call for differential linearity measurements at the codes involved in all major carries (e.g., 1000/0111, 0100/0011, etc.), the carries at the sums of the MSBs (e.g., 1100/1011, 1110/1101, etc.), and plus/minus two codes around each. To this might be added a bit-superposition test at the expected worst-case summation codes: first determine the nonlinearity associated with each bit, then form two words, one consisting of all bits having positive errors (the worst-case positive error), the other consisting of all bits having negative errors (the worst-case negative error), and test them and plus/minus two codes around each.

Finally, if the DUT is expected to perform at high conversion rates, if it is of a type whose history records anomalous nonlinearities, or if it is a characterization sample, it may be desirable that all codes be tested for nonlinearity. Typically, the LTS-2010 can test all 4094 intermediate codes of a 12-bit 25µs converter for nonlinearity within about 15 seconds, using these techniques.

The technology used here permits quantitative evaluation of transition uncertainty by the performance of large numbers of measurements in a short time to map out the statistical behavior of transitions. Figure 1b shows that, as the input to the converter is reduced from the center of the code under test (C1) to the center of the next lower one (C0), the proportion of conversions to C1 decreases from nearly 100% to 50% (at the transition) to nearly 0 (at the center of C0). The transition could be mapped by fixing the Dither DAC output at a sequence of values; performing (say) 1000 conversions at each input value; counting the number of conversions to C1 and C0; and computing the ratio for each input value by dividing conversions to C1 by the total. The entire mapping of the transition, plus computation of the 50% point and the standard deviation, could be completed in less than a second. □



$$\text{DITHER-DAC LSB} = \frac{R}{R_1} (\text{MAIN-DAC LSB})$$

Figure 4. Using compounded main and dither DACs in testing.