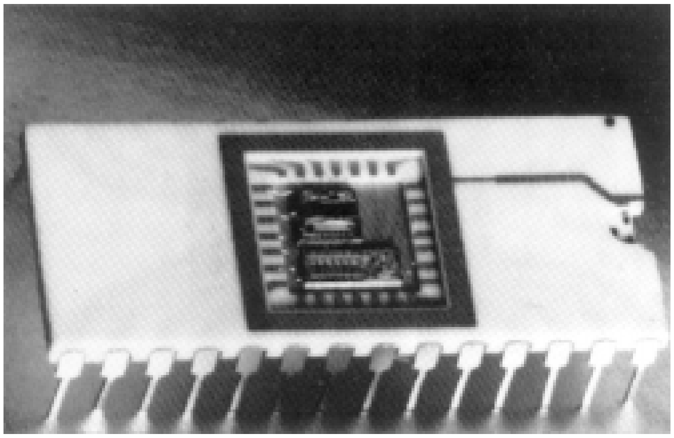
COMPLETE 12-BIT 2-CHIP IC A/D CONVERTER

25μs Successive-Approximation AD574 Is Fully Bus-Compatible Versatile Interface Controls Provide Applications Flexibility

by Mike Timko and Peter Holloway

The Analog Devices AD574 is a complete 12-bit integrated-circuit analog-to-digital converter in a 28-pin hermetically sealed dual in-line package. Using a successive-approximations approach, the AD574 performs a complete 12-bit conversion in 25μs (35μs *max*). The two complementary chips contain all the necessary circuitry, including a stable buried-Zener reference, d/a converter, comparator, successive-approximations register, three-state output gates, and all the interface logic needed for total self-sufficiency as either a conventional stand-alone ADC or as a memory-managed ("-mapped") microprocessor peripheral (Figure 1). The fast, current-output DAC and its reference, on a single monolithic chip, are available separately as the AD565 . Cost of the AD574 is only $36 (J Grade in 100's).



WHY THE AD574?

Digital technology is increasingly being used in measurement, control, communication, and signal processing, in an ever-widening circle of real-world applications, from industrial processes and heavy machinery to automobiles and appliances. The needs for interfacing analog variables in these applications often demand no more than either high-resolution, slow, integrating a/d converters or faster 8-bit devices; but there is an increasing number of applications that call for fast conversion with 12 bits or more of resolution with accuracy, reliable performance, and low cost.

It is manifestly true that the systems engineer would benefit greatly by having all stages, from sensor to processor, combined inside a single IC package. No minor advantage would be relief from the task of dealing with the assembly of pieces of a circuit comprising 0.01% dc accuracy, 25μs conversion time, and the implied need for the equivalent of 1.5MHz full-power system bandwidth, 30nV/$\sqrt{\text{Hz}}$ noise levels, and VHF layout techniques.

The AD574 is a big step towards this goal, solving (as it does) the problem of designing the interface between the two worlds and relegating most of the remaining design problems to either purely analog or purely digital – and, in most cases, purely routine – considerations.

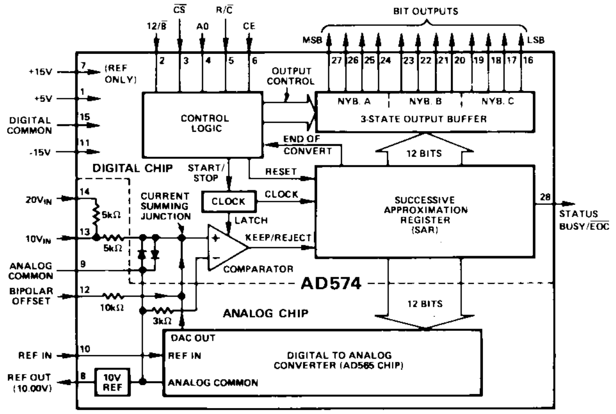


Figure 1. Block diagram of AD574 12 bit A-to-D converter.

Designed as a single unit, the AD574 is the most-complete, lowest-cost, and easiest-to-use fast 12-bit IC converter available. Drift with time and temperature are minimized by closely tracking monolithic thin-film resistors and a low-drift, low-noise buried-Zener reference. Excellent absolute accuracy and linearity are achieved by judicious use of both laser (wafer) trimming (LWT) and Zener-zap trimming (ZZT). Noise is minimized by the use of the buried-Zener reference and a controlled-bandwidth-front-end latching comparator. Flexibility is available at both the analog end(choice of ranges and use of the reference), and at the digital end (variety of TTL control logic), implemented in integrated injection logic (I^2L). Cost is minimized by manufacturing the ADC as two chips, optimized for size and performance, trimmed at the wafer stage, and combined in a 28-pin integrated-circuit package.

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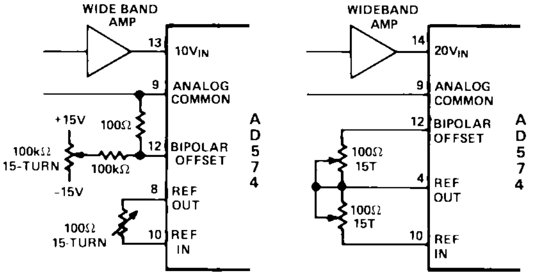
SALIENT ANALOG FEATURES OF THE AD574

Figure 1 is a functional block diagram of the AD574, showing both the analog and the digital sections. The analog chip contains the 10V reference, the current-output DAC, and the bipolar-offset and scaling resistors; the digital chip contains the SAR, control logic, clock, comparator, and 3-state buffer.

The connection between the precision reference and the DAC reference input is made externally. This permits the slaving of several ADC's to a single reference, ratiometric operation, and optional trimming of the scale factor. For bipolar input voltage, the BIPOLAR OFFSET terminal is connected to the reference output to offset the input by half-scale (an external offset trim is optional). The 20V and 10V span inputs permit ranges of 0 to +10V, –5V to +5V, 0 to +20V, and –10V to +10V. Figures 2a and 2b show the connections, including optional trims, for 0 to +10V and –10V to +10V operation.



0 TO +10V UNIPOLAR CIRCUIT WITH TRIMS

-10V TO +10V BIPOLAR CIRCUIT WITH TRIMS

Figure 2.

Besides providing the current available for local use, the +10V (±25mV, 20ppm/°C) reference can furnish up to 2.5mA for external use when connected for unipolar operation, and 1.5mA in the bipolar connection. A single reference can accommodate two AD574's in bipolar operation or six AD574's in the unipolar mode. If a device's internal reference is not used, the +15V connection, which supplies the reference only, may be omitted.

CONTROLLING THE AD574

The AD574's parallel data output consists of a 12-bit 3-state (1, 0, open) buffer. Depending on the logic inputs and the device wiring, the eight more-significant bits (nybbles[1] A & B), the four less-significant bits (nybble C and zeros at nybble B), or all twelve bits can be enabled. A STATUS (BUSY-$\overline{\text{EOC}}$) output goes high when a conversion is in progress. As will be shown, conversion may be stopped after eight bits ("short cycle") for a tradeoff of resolution for speed.

Five control inputs provide flexible means of controlling both the start of conversion and the choice of output display. Their functions are tabulated below.

AD574 CONTROL TABLE

CONTROL INPUT	CONVERT FUNCTION	DISPLAY FUNCTION
CE, "Chip Enable" (Clock synchronization in μP applications)	Must be *high* for a conversion to be initiated.	Must be *high* for the results of a conversion to appear at the output.
$\overline{\text{CS}}$, "$\overline{\text{Chip Select}}$" (Address pin in μP applications)	Must be *low* for a conversion to be initiated.	Must be *low* for the results of a conversion to appear at the output.
$R/\overline{C}$, READ/$\overline{\text{CONVERT}}$	Must be *brought low* before a conversion (each conversion) can be initiated	Must be *high* for the results of a conversion to appear at the output
A0 "Address"	Selects conversion mode to be initiated: 12 bits, if *low*, 8 bits (short cycle) if *high*	Selects output word in multiplexed conversion: Most-significant byte (nybbles A & B) if *low*, Least-significant byte (nybble C and all-zeros at B) if *high*
$12/\overline{8}$, 12 Bits/$\overline{8\ \text{Bits}}$ output format, hard wired to +5V, *high*, or digital common, *low*	No function	Output format is 12-bit parallel if *high*, 8-bit multiplexed if *low*

While many combinations of signals at these inputs will operate the device, each of the apparently redundant inputs has a specific reason for being included and does one kind of job best. For instance, the Chip-Enable pin (CE) has the fastest response of all the inputs. If all the other inputs are in the appropriate states, the width of a pulse at CE to start a conversion need not exceed 300ns. CE also brings the three-state outputs *on* in the shortest time, about 350ns. Therefore, CE is the most likely to be used to synchronize the AD574 to a microprocessor data bus. Though $\overline{\text{CS}}$ ($\overline{\text{CHIP SELECT}}$) is 100ns slower than CE, it has the correct sense for many common address-decoding schemes.

The READ/$\overline{\text{CONVERT}}$ pin ($R/\overline{C}$) selects either the conversion mode or the output mode during a μP instruction cycle; or it can control the entire device in the 12-bit stand-alone mode. A conversion starts whenever CE is *high*, $\overline{\text{CS}}$ is *low*, and $R/\overline{C}$ has gone *low*. The conversion is edge-triggered; within 400ns the STATUS output goes *high* (BUSY), the outputs are forced into the *off* state (if they weren't there already), and all further inputs are ignored until the conversion is complete.

In stand-alone operation, CE and $\overline{\text{CS}}$ are wired *high* and *low*, and $R/\overline{C}$ is toggled; bringing it *low* starts a conversion. After 400ns, it can be brought *high* without affecting the progress of conversion; the outputs will remain inhibited until the end of conversion, then come on. If, on the other hand, $R/\overline{C}$ is held *low*, the outputs will be held in the *off* state until $R/\overline{C}$ is returned *high*, at which time they will be activated.

Once $R/\overline{C}$ has been brought *low*, a conversion can be initiated by bringing CE *high* ($\overline{\text{CS}}$ *low*) or $\overline{\text{CS}}$ *low* (CE *high*). However, one of the three must be cycled before another conversion can take place, even if the output is not to be read out. (Readout is inhibited by bringing CE *low* or $\overline{\text{CS}}$ *high*, while $R/\overline{C}$ is *high* or bringing $R/\overline{C}$ *low* before the end of conversion).

The hard-wired output-format connection, $12/\overline{8}$ selects between 12-bit parallel output and 8-bit multiplexed outputs (left-justified). With $12/\overline{8}$ programmed *low*, only two output nybbles at a time can be enabled, preventing bus conflicts for parallel-wired multiplexing schemes.

The state of A0 at the start of conversion determines whether the conversion is to be a full 12-bit conversion or an 8-bit "short cycle". The state of A0 when the outputs are enabled determines whether the high or the low byte is selected in 8-bit multiplexed operation. For example, if the result of a 12-bit conversion is 1 0 0 1 0 1 1 0 0 0 1 0, in multiplexed operation (to be described), A0 *low* outputs 1 0 0 1 0 1 1 0, and A0 *high* outputs 0 0 1 0 0 0 0 0 on the 8-bit bus.

In memory-managed interfacing, A0 can be viewed as a pair of read-write memory locations for both "read" and "write". A *write* command at the lower address at the start of conversion produces a full 12-bit conversion; a *write* command at the upper address produces an 8-bit conversion. A *read* command at either address when $12/\overline{8}$ is *high* will result in full 12-bit output data (for a 12-bit conversion); but if $12/\overline{8}$ is *low*, a *read* command at the lower address will output the 8 more-significant bits, and a *read* command at the higher address will output the 4 less-significant bits and four trailing zeros.

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[1] See Bibbero, R. J., *Microprocessors in Instruments and Control*, John Wiley and Sons, 1977, page 107" . . . four bits have been termed a *nybble* (obviously a small byte)."

MULTIPLEXING AD574 ON 8-BIT BUSSES

As we have noted, the same output buffers which can present 12-bit parallel data are also designed to multiplex directly into an 8-line microprocessor bus. Multiplexing is accomplished by grounding the output mode pin, $12/\overline{8}$, and paralleling nybble C, which contains the 4 lowest-order bits, with output nybble A, which has the 4 highest-order bits. Wiring $12/\overline{8}$ low prevents simultaneous enabling of A and C, and causes four zeros to appear at B when the low-order word is enabled.

Perhaps the simplest interface configuration, with the 6800 μP, is shown in Figure 3. The AD574 is shown directly connected, with no external control logic, to the data, control, and address buses of the microprocessor. While few systems will ever be this simple, the number of additional component packages required will in general be considerably less than are usually required for interfacing analog signals to μP's. For larger systems, appropriate decoding between the address bus and $\overline{CS}$ will be required; a convenience of the AD574 is that $\overline{CS}$ is of the right polarity for the active-*low* output of most decoders.

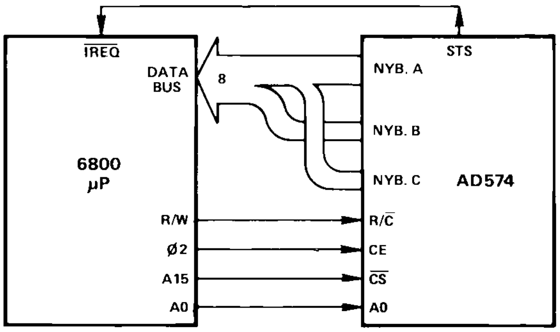


Figure 3. Basic interface between AD574 and a standard 6800 system.

CE is timed to enable the AD574 when phase 2 of the clock, (the bus-synchronizing signal) goes *high*, as $\overline{CS}$ goes *low* when the AD574 is selected. The STATUS line of the AD574 is shown connected to $\overline{IREQ}$, the maskable *interrupt* line of the 6800, it goes low and serves as a means to request attention from the processor after the conversion has been completed. Since this channel is software-maskable, the processor need not service an *interrupt* routine, but may be programmed to time out the 35μs needed for conversion instead.

Figure 4 shows the connection of the AD574 to a standard 8080A system, which includes an 8228 system controller. While the 8080A does not produce signals that will operate the AD574 directly, the appropriate signals can be synthesized by a single NAND gate. Address bit A15 is shown connected to the same NAND gate, an alternate way of addressing.

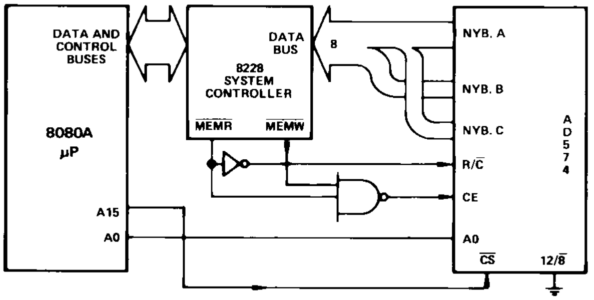
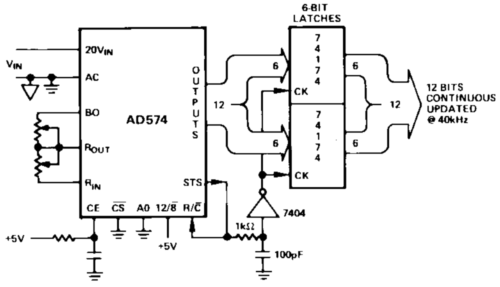


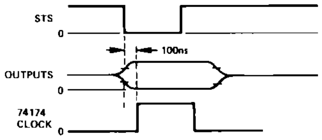
Figure 4. Basic interface between the AD574 and a standard 8080A system.

BASIC STAND-ALONE CONVERSION

In the quest for μP compatibility, it is easy to lose sight of ADC application features that are traditionally necessary. One of the oldest—but still quite common—requirements is self-triggered continuous conversion, illustrated in Figure 5.



(a) Block diagram.



(b) Timing diagram.

Figure 5. Continuous conversion application with dual-rank output latching.

The key to continuous conversion is feeding the STATUS line back to the R/$\overline{C}$ input. In each cycle, the following chain of events occurs repetitively: As a conversion begins, STS goes high, programming the control logic (via R/$\overline{C}$) for an output *read*. The outputs are kept in the *off* state, as part of the normal internal program, until the conversion is complete. When the data is ready, the inherent timing is such that the outputs automatically come *on* (in response to R/$\overline{C}$ *high*) within 80ns of the *low* transition of STS, allowing the STS transition to its low (end-of-conversion) state to be used, with a 100ns delay, as a strobe to latch the output data into the 74 latches. The STS transition also initiates another conversion and starts the sequence all over again, with another STS low-to-high transition occurring about 400ns later.

Since the AD574 has a stable latchup mode, which can only be entered during power-up or fault conditions (STS and R/$\overline{C}$ both coming on *low*), CE is used here as an initialization control, operating from a power-up pulse, or some other suitable source.

EXTENDING RESOLUTION TO 15 BITS

Real-world signals often have dynamic ranges that greatly exceed the 72-dB span of a 12-bit converter. The manner of performing the conversion depends on the desired relationship between dynamic range, resolution, and accuracy. Obviously, if all of these characteristics must be preserved for a 15-bit linear conversion (32,768 unique codes, each occurring within ±1/2LSB of the ideal analog value), a true 15-bit converter must be used.

However, a true 15-bit converter is not always necessary. For example, if a dynamic range of 2^{15} is desired (i.e., the LSB is 2^{-15} of full scale), but it is not necessary to resolve large signals to better than 2^{-12}, a technique often used is to employ a programmable-gain amplifier with precise gains of 1, 2, 4, 8, ahead of the 12-bit a/d conversion. The effect of this is to shift the output word by 0, 1, 2, or 3 bits, increasing the size of the word to 15 bits, and providing 15-bit resolution for signals from 2^{-15} to 2^{-3} of full-scale range, 14-bit resolution for signals from 2^{-3} to 2^{-2} of FSR, 13-bit resolution for signals from 2^{-2} to 2^{-1} of FSR, and 12-bit resolution for signals from 2^{-1} of FSR to $(1 - 2^{-12})$ FSR.

A key consideration in many applications is that there be no loss of resolution through missing codes in the vicinity of transitions where gain is switched. Examples of applications where abrupt discontinuities in the transfer curve destroy essential information include digitized audio, detection of visual image contours from photomultiplier-tube outputs, and rate-sensing in liquid-chromatography experiments. If you build a 15-bit ADC by gain-ranging at the input of a 12-bit ADC, then the gain function (including drift and offset) must itself be good to better than 15 bits, to ensure monotonic behavior at the boundaries between the top of one gain range and the midpoint of the next range, which has twice the gain.

A useful way of achieving 15-bit resolution (over the *whole* range) is shown in Figure 6. It utilizes a precision differential amplifier, an AD574, a microprocessor as the controller, and a rudimentary 3-bit DAC with 12-bit or better accuracy. Here, the gain of the basic a/d conversion never changes from 1.25V full-scale, referred to the analog input. Instead, the 0-10V input signal is dealt with by subtracting multiples of 1.25V (i.e., $10V/2^3$) from the input, searching for the condition where the remainder is between 0 and 1.25V in magnitude. The residual voltage (amplified 8x) is converted by the AD574, which (in effect) interpolates to twelve bits of resolution between the appropriate adjacent segment boundaries (0, 1.25V, 2.5V, . . . 8.75, 10.0V)

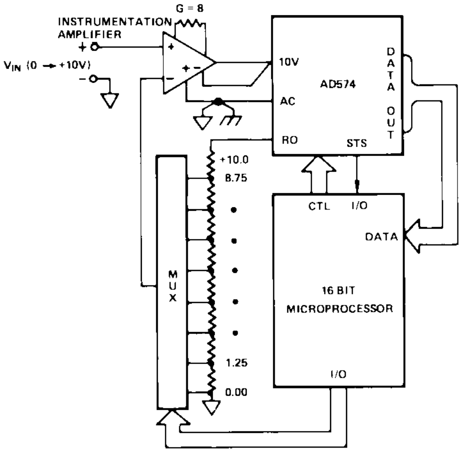


Figure 6. 15-bit ADC application.

The important distinction here is that the 3-bit DAC doing the offsetting need not have 15-bit accuracy. Because the ADC never spans more than one segment at a time, the endpoints will match to the ultimate resolution of the system if the magnitude of the voltage across each of the 1.25V segments agrees with the 1.25V(amplified) full-scale of the converter *to within one LSB*. Thus, a 12-bit-resolution, 12-bit-accuracy ADC and a 3-bit-resolution, 12-bit-accuracy DAC can team up to make a monotonic 15-bit-resolution, 12-bit-accuracy ADC.

The fastest way to run this system is to implement a successive-approximation routine for the three range bits in a controller or microprocessor, comparing the output of the AD574 with the digital threshold values, to determine whether to keep or reject each range bit as it is tested. Using this approach, four conversions will be needed, three for range, and one for 12-bit interpolation. The processor (e.g., 8086, 9940) controls the timing and the 3-bit SAR routine, and completes the arithmetic to provide a 15-bit conversion every 100-150μs.

The DAC consists of an 8-channel CMOS multiplexer and a string of eight equal resistors matched to within 0.01%. The taps on the divider chain are switched through the multiplexer and applied to the high-impedance subtracting input of the instrumentation amplifier. The AD574's reference is used for both the a/d converter and the feedback DAC, to insure ratiometric tracking of the two DAC's with time and temperature.

Since we are concerned with 15-bit operation (LSB = 31ppm = 0.3mV), extreme care must be taken to minimize IR drops and avoid ground loops. In Figure 6, we show a high-quality ground at the analog common (AC) pin of the AD574, and all signal grounds are returned to this point separately. If the signal-input low cannot be accurately referenced to the AC pin because of heavy currents flowing through the signal lines— which the designer is powerless to reduce further – then dc common-mode rejection must be incorporated. This can be implemented by connecting the positive output-sense line of the instrumentation amplifier to an inverting-ground sensing amplifier with a gain of 1/8, instead of the AC pin. Of course, all of the usual tradeoffs of noise and bandwidth apply, but remember that a single feedback capacitor alone won't control the noise bandwidth. The reference noise, less than 1mV peak-to-peak in 1MHz bandwidth, can be further reduced by shunting the RO pin with a large tantalum capacitor $C > 0.1\mu F$, but care must taken that the equivalent series resistance (ESR) of the capacitor be no more than a few ohms, to maintain loop stability.

A FEW WORDS ABOUT TECHNOLOGY

The photograph on page 3 shows the two complementary chips in the open package. The long, thin chip ($2 \times 5.6mm^2$) contains the comparator, successive-approximation register, output gates, and control logic; the other chip ($3.3 \times 3.7mm^2$) is the DAC.

The silicon-chromium thin-film resistors are trimmed by cutting into the tab areas of the resistors with a 0.4 mil He laser, which vaporizes the Si-Cr film. This trimming occurs during functional probe at the wafer stage; a computer actively monitors parameters of interest, and trimming is a real-time feedback event. 22 trims are performed, many to an overall resolution of 0.001%.

The SAR chip requires trimming of the comparator offset only. Currents through a network of diffused resistors are switched by selective automatic "zapping" (melting) of 5 fusible Zener diodes (32 choices) by programmed current overloads, forming a permanent low-impedance path, and making it possible to adjust the comparator offset to within 100μV.

Since both chips are manufactured by a linear-compatible-I^2L diffusion process, it is feasible (at some future time) to merge the two chips without substantially modifying either the circuitry or the trimming strategy. ▶▶▶