

KEYS TO LONGER LIFE FOR CMOS HERE'S HOW CMOS CAN BE PROTECTED AGAINST ABUSES

by Jerry Whitmore

The two principal dangers to analog CMOS (Complementary-symmetry Metal-Oxide Semiconductors) are static electricity and overvoltage (signal voltages exceeding the supply). Both can be effectively dealt with by the aware user.

STATIC ELECTRICITY

The danger from electrostatic voltage buildup is that of "punch-through" of the thin oxide (or nitride) layer that insulates the gate from the substrate, due to accumulation of static charge ($V = q/C = 1\text{kV/nC/pF}$). This danger is minimal in working circuits, because the gate is protected by zener diodes on the chip, which permit depletion of the charge at safe levels. However, during socket insertion, it is possible for a large static charge to exist between the CMOS device and the socket. If the first pin plugged into the socket happens not to be common to the zener-diode protection circuit, the charge on the gate will discharge through the oxide layer, destroying the device. These four steps will help the device survive the system assembly stage.

1. Keep unused CMOS devices in the black conductive foam in which they were shipped to prevent charge buildup between pins.
2. Ground the operator, who is inserting the devices, to the system power ground with a plastic ground strap.
3. Before pulling the CMOS device from the protective foam, ground the foam to power common to deplete accumulated charge.
4. After the circuit has been inserted into a circuit board, keep the board grounded or shielded when carrying it around.

THE SCR "LATCH"

When working with analog CMOS circuits, the safest practice is to make sure that no analog or digital voltage applied to the device exceeds the supply voltage, and that the supply voltage itself is within ratings. Nevertheless, occasions do arise where it is necessary to tolerate overvoltage. Protection is possible in most cases, if the mechanism of failure is understood.

Figure 1 shows the circuit and cross-section of a typical CMOS output switching element. From the connections and associa-

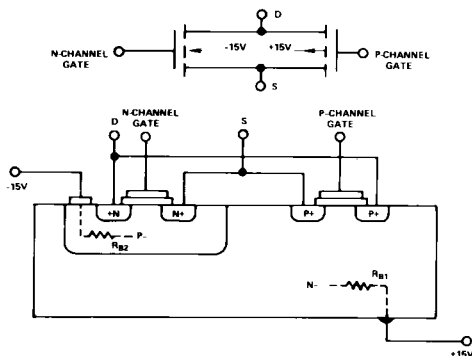


Figure 1. Cross-section of CMOS switching element

tions of the various elements and regions, we can draw an equivalent diode circuit (Figure 2). If the analog input voltage at either the S or the D terminals exceeds the power-supply

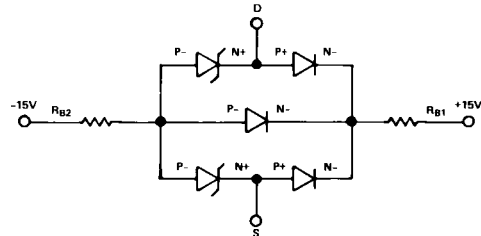
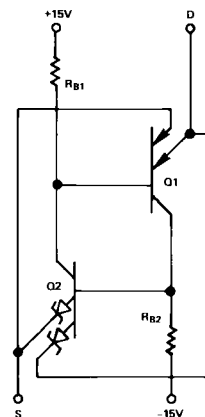


Figure 2. Diode equivalent circuit of CMOS switching element

voltages, the parasitic transistors formed by the various diode junctions are placed in the forward bias mode. These parasitic NPN and PNP transistors appear to form the SCR ("silicon controlled-rectifier") circuit shown in Figure 3. Overvoltage



IF, FOR EXAMPLE, A POSITIVE OVERVOLTAGE IS APPLIED TO THE DRAIN TERMINAL, THE BASE OF Q1 WILL CONDUCT WHEN ITS EMITTER VOLTAGE EXCEEDS V_{DD} BY ONE BASE-EMITTER DROP. THE COLLECTOR CURRENT WILL INCREASE TO A LEVEL LIMITED ONLY BY THE V_{SS} AND V_D CURRENT LIMITATIONS. SINCE THE METAL INTERCONNECT TO THE SUPPLY TERMINAL IS NORMALLY DESIGNED TO HANDLE SMALL CURRENTS, THE CURRENT DENSITIES INVOLVED CAN CAUSE DEVICE FAILURE.

Figure 3. Parasitic transistor action in CMOS switch

can cause excessive current and metallization failure. Normally, the outputs of op amps are used as the voltage sources feeding the S or D terminals, so the currents cannot exceed the op amps' dc output current limitations. Nevertheless, it is still possible for transient induced currents to destroy the CMOS device; protection is therefore desirable.

Figure 4 illustrates a means of preventing turn-on of the parasitic transistors by means of diodes (say 1N459's) in series with the supply leads. If the S or D terminal is at a higher-than-supply voltage, CR1 and/or CR2 are reverse-biased and base drive is unavailable to turn the transistors on. A separate pair of diodes should be used for each CMOS device to be protected. Though powerful, the method is not infallible. If one terminal of the switch is tied to a negative potential (e.g., a charged capacitor), and the other terminal is raised above V_{DD} ,

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USING DPM'S IN OUR OWN TEST EQUIPMENT FOR FAST, EASY, ACCURATE TESTING OF ELECTRONIC PRODUCTS

by Jim Hayes

Since entering the Digital Panel Meter market, we have discovered (to no one's surprise) that DPM's are useful in production test equipment for our other electronic products. The advantages are like those for any other application: the DPM allows the user to make accurate, unambiguous readings of electrical quantities without the errors associated with conventional analog meters. The digital readout and fast response relieve even the unskilled operator of the necessity for interpolating between analog scale divisions and waiting for the pointer to settle. Using the digital output, the operator can even be relieved of the task of writing down the readings. The low bias current and high input impedance of the DPM further simplify its application, since buffering is seldom necessary.

Using the digital data outputs, the meter can be interfaced with comparators to provide an accurate go/no-go indication, to data processors for storage and evaluation of test results, and to printers for hard-copy test data for quality-assurance records. As an A/D converter, the DPM is, of course, the key link in automated test systems with optional on-line operator control.

In addition to the above advantages, test-equipment operators find test sets with DPM readouts to be easier and less tiring to use, allowing faster and more-accurate testing of all relevant product parameters in full operation. Here are a few examples:

TESTING OP AMPS. Many specified op-amp parameters are tested on a 100%-sample basis, often over specified temperature ranges. To check compliance with tempco specs, test fixtures

are loaded with devices to be tested, placed in "ovens," and cycled over the full temperature range. A DPM rapidly reads out the voltage offset and bias-current error of every device in sequence, so that all devices can be fully tested at every temperature checkpoint in a short time.

TESTING D/A AND A/D CONVERTERS. To check d/a converter outputs for accuracy and linearity, the analog output is measured with a DPM and compared with the digital input. The operator can use the direct reading of the output to make test adjustments or go/no-go decisions rapidly. DPM's can also be used to measure magnitude and polarity of errors directly. An example of A/D converter testing is shown in the photograph: The ADC1100, a 0.05%-resolution converter, has its BCD output displayed digitally, and compared with the analog input, as measured with a 0.005% AD2004* DPM. By matching the two displays, the operator can test ADC1100's to specified accuracy in minimal time.

TESTING DPM'S. Since DPM's use several circuit boards for different functions, the test fixture for each board is an "incomplete DPM," consisting of the other boards and appropriate connectors. The board is placed in the test fixture, and the DPM is checked as a whole. DPM's are used for troubleshooting in these fixtures by checking for proper voltages at specified test points. On ac-powered DPM's the power-supply board's output of $\pm 15V$, $+5V$ and (for gas-discharge displays) $200V$, can be tested with a single DPM (with attenuators and switch controlled decimal points) by an untrained operator in seconds.

THE TEST DEPARTMENTS' FAVORITE DPM. Which DPM is the most-used in our test equipment? Our test-equipment engineers prefer the AD2004* ($+5V$ -powered, $4\frac{1}{2}$ -digits). Besides the reasons discussed above, the high resolution, accuracy, and stability of the AD2004 make it ideal for test equipment, allowing precise measurements of test parameters, with long intervals between calibrations. But plenty of our other DPM's are also used (for the simpler tests).

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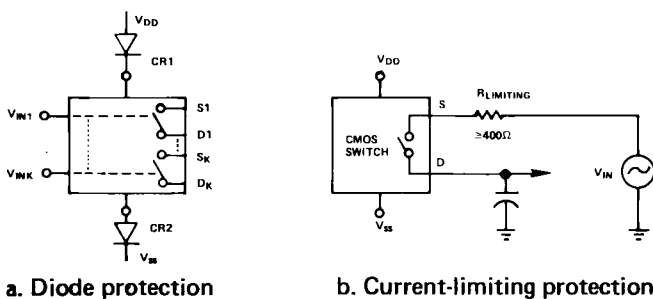


Figure 4. Circuit protection schemes

the avalanche diode at one emitter of Q2 is sufficient to supply enough base drive to turn Q2 on, despite the protective diodes. For such a situation, a current-limited supply, or resistance in series with the capacitor is necessary.

If transient overvoltages are expected at the S or D terminals, $300\text{--}400\Omega$ in series with the terminal to be fed by the voltage source is suggested (Figure 4b).

