

# Understanding Sample-Hold Modules

a guide to their specifications and application

by A. Sanchez

A Sample-Hold module is a device having a signal input, an output, and a control input. It has two steady-state operating modes: *Sample*, (or "Track") in which it acquires the input signal as rapidly as possible and tracks it faithfully until commanded to *Hold*, at which time it retains the last value of input signal that it had at the time the control signal called for a mode change. Sample-Holds are often more-appropriately known as "Track-Holds" if they spend the major portion of the time in *sample*, tracking the input.

Sample-Holds usually have unity gain and are non-inverting. The control inputs are operated by "standard" logic levels, and are usually TTL-compatible. Logic "1" is usually the *Sample* command and logic "0" the *Hold* command.

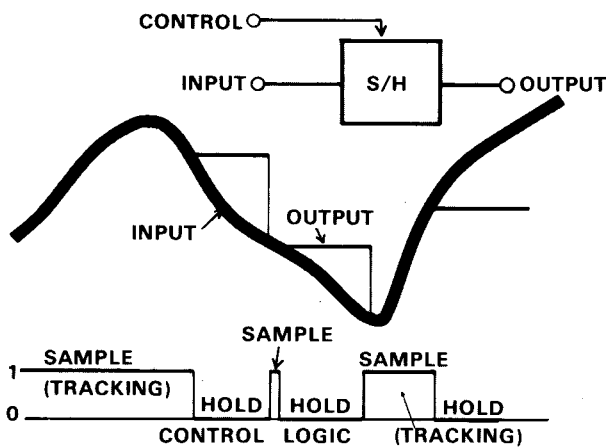


Figure 1. Typical Sample-Hold Waveforms

## USES OF SAMPLE-HOLDS

In data-acquisition systems, Sample-Holds are used either to "freeze" fast-moving signals during conversion or to store multiplexer outputs while the signal is being converted and the multiplexer is seeking the next signal to be converted. In analog data-reduction, they may be used to determine peaks or valleys, establish amplitudes in resolver-to-digital conversion, and facilitate analog computations involving signals obtained at different instants of time. In data-distribution systems, Sample-holds are used for holding converted data between updates. Fast Sample-Holds may be used to acquire and measure fast pulses of arbitrary timing and width.

## CHARACTERISTICS OF REAL SAMPLE-HOLDS

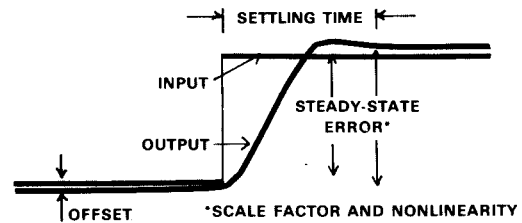
In the ideal Sample-Hold of Figure 1, tracking is error-free, acquisition and release occur instantaneously, settling times are zero, and hold is infinite. Commercially-available units\* are specified in terms of the extent to which they depart from the ideal. Here are some of the commonly-occurring deviations (See also Figure 2):

During *SAMPLE* (Figure 2a):

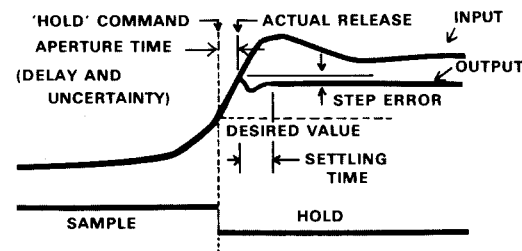
**OFFSET:** For zero input, the extent to which the output deviates from zero, a function of time and temperature

**NONLINEARITY:** The amount by which the plot of output vs input deviates from a "best straight line"

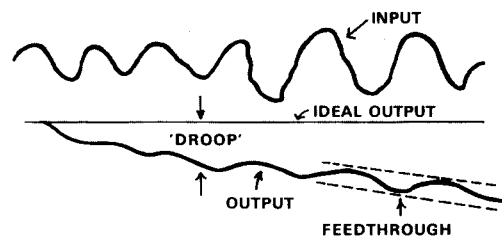
**SCALE FACTOR ERROR:** The amount by which the output deviates from specified gain (usually unity)



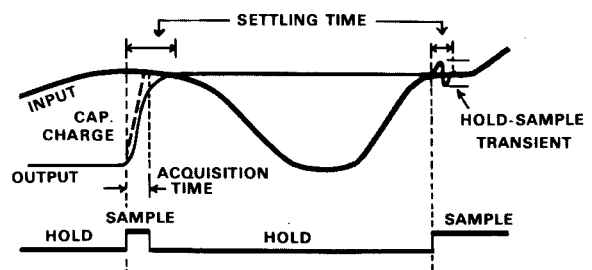
a. Tracking Errors During Sample



b. Sample-to-Hold Errors



c. Errors in Hold. Droop may be either Positive or Negative



d. Hold-to-Sample Errors

Figure 2. Sample-Hold Errors, Shown Qualitatively. Magnitude Scale is Greatly Exaggerated.

**SETTLING TIME:** The time required for the output to attain its final value within a specified fraction of full scale when a full-scale input step is applied (0 to  $\pm$ FS or  $-$ FS to  $+$ FS). See also *Acquisition time* (Fig. 2d).

In this state, the unit behaves as a slow unity-gain follower. Thus one might expect to encounter other specifications typical of such devices, such as phase shift, slew rate, full-power bandwidth, small-signal bandwidth, etc.

#### **SAMPLE to HOLD (Figure 2b):**

**APERTURE TIME:** The time elapsing between the command to *Hold* and the actual opening of the *Hold* switch. It has two components: a nominal time delay, and an uncertainty caused by jitter or variation from time-to-time or unit-to-unit. If a signal changing at a rate of  $1\text{V}/\mu\text{s}$  must be resolved to within 0.1% of 10V (FS), the aperture *uncertainty* must be less than 10ns, provided that it is possible to anticipate the nominal delay and advance the command by an appropriate interval. In some sampled-data system applications, such as spectrum analyzers, auto- and cross-correlation function generators, the delay is unimportant, but the uncertainty directly affects uniformity of the sampling rate. Manufacturers – to date – have not displayed consistency in their usage of *aperture time*; hence it is a good idea to find out exactly what the specification means for a unit you may be considering.\*

**SWITCHING TRANSIENTS:** At the time the switch opens, the circuit may not be in equilibrium – especially if the signal is changing rapidly – because of amplifier delay error, etc. This will cause transients at the time the switch opens.

**SETTLING TIME:** The interval required for the output to attain its final value within a specified fraction of full scale, following the opening of the switch.

**SAMPLE-TO-HOLD OFFSET:** A step error occurring at the initiation of the *Hold* mode caused by “dumping” of charge into the storage capacitor via the capacitance between the control circuit and the capacitor side of the switch (e.g., the gate-to-drain capacitance of a field-effect transistor). It can be partially compensated by coupling an out-of-phase signal through a compensating capacitor, but usually only under a given set of tightly-controlled and highly-“tweaked” conditions. This offset does not occur in units having digital *Hold*.

#### **During HOLD (Figure 2c):**

“DROOP:” A drift of the output at an approximately constant rate caused by the flow of current through the storage capacitor. ( $dV/dt = I/C$ ) The current is the sum of the leakage across the switch, the amplifier’s bias current, and leakage to the power supplies and to ground. In a well-designed unit, only the first is of any consequence. Units having digital storage have no droop. A rough figure-of-merit for analog Sample-holds is the ratio of droop time to settling time for the same percentage (FS) error. For example, a unit having settling time of  $5\mu\text{s}$  to 0.01% and droop rate of  $50\text{mV/s}$  ( $0.02\text{s}$  to  $1\text{mV}$ ), would have a figure-of-merit of  $20,000/5 = 4,000$ .

\*The inconsistency in the industry extends even to the spelling. However, there seems little question that *aperture*, which is derived from the Latin *apertura* (from *apertus*, open) is the correct spelling, preferable to *aperature*, which cannot be found in most dictionaries.

**FEEDTHROUGH:** The fraction of input signal that appears at the output in *Hold*, caused primarily by capacitance across the switch. Usually measured by applying a full-scale sinusoidal input at a fixed frequency (e.g.,  $20\text{Vp-p}$  at  $10\text{kHz}$ ), and observing the output.

**DIELECTRIC ABSORPTION:** The tendency of charges within a capacitor to redistribute themselves over a period of time, resulting in “creep” to a new level when allowed to rest after large, fast changes. Less than 0.01% for good polystyrene and teflon capacitors, as large as several percent for ceramic and mylar capacitors.

Output impedance of the Sample-Hold should be low and recovery fast to minimize transients caused by dynamic loads, such as A/D converter inputs.

#### **HOLD to SAMPLE (Figure 2d):**

**ACQUISITION TIME:** The time duration for which an input must be applied for sampling to the desired accuracy. Essentially the same as *Settling time* for feedback types, but shorter than *Settling time* for two-stage units and for open-loop follower types in which the amplifier’s settling time is appreciable compared to the capacitor’s charging time.

**HOLD-TO-SAMPLE TRANSIENTS:** Transients (e.g. spikes) occurring between the *Sample* command and final settling. Not too important for large changes, but can be crucially important in some applications if the spikes are large compared to the actual change (e.g., at constant input). Such “glitch”-like spikes may be due to limiting and other sources of dynamic disequilibria within the Sample-Hold circuit, or to capacitive feedthrough from the control signals.

### **TYPICAL DESIGNS**

The choice of storage element divides Sample-holds into two major classes. The more conventional, popular, and the lower in cost employs a capacitor for storage (*analog storage*); several forms of this design will be discussed here. The other technique, which uses an A/D converter and a register for storage, and reads out via a D/A converter, is somewhat more complex and costly (especially where high accuracy or fast sampling are necessary), but it has the undisputed advantage of arbitrary – and essentially “infinite” – *hold* time. Some ways of instrumenting that approach are discussed on page 15 of this issue.

#### **Open-Loop Follower (Figures 3, 4, 5)**

The most obvious circuit to come to mind is that shown in Figure 3. When the switch is closed, the capacitor charges exponentially to the input voltage, and the amplifier’s output follows the capacitor’s voltage. When the switch is opened, the charge remains on the capacitor. The capacitor’s *acquisition time* depends on the series resistance and the current available to charge its capacitance. Once charge is acquired, to the appropriate accuracy, the switch may be opened, even though the amplifier has not yet settled, without affecting the final

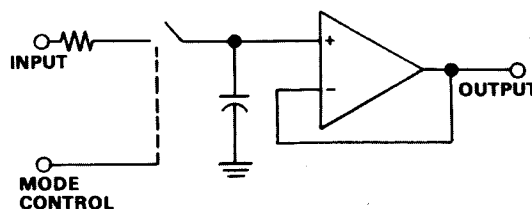


Figure 3. Simple Follower

output value or the settling time (assuming that the amplifier's input stage does not draw appreciable current at any time). The switch is typically a FET, and the amplifier is a FET-input type. This circuit has the disadvantage that the capacitor loads the input source, which — often enough — will either oscillate or lack sufficient current to charge the capacitor speedily. The circuit of Figure 4 includes a follower to isolate the source. The Analog Devices general-purpose SHA-1A uses this scheme.

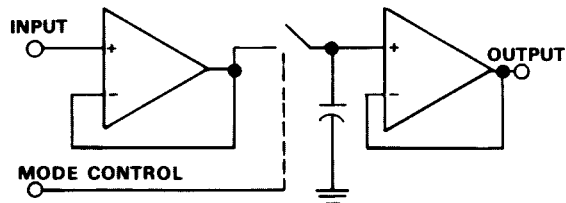


Figure 4. Same as Fig. 3 but with Isolated Input.\*

For extremely fast charging at approximately a linear slew rate, a diode bridge scheme may be used, essentially as shown in Figure 5. Here, current sources are switched on to charge the capacitor. If the bridge and current sources are appropriately balanced, current flow into the capacitor will cease when the capacitor voltage is equal to the input voltage. Figure 5 is a simplified block diagram of the SHA-II, which has an acquisition time of 200ns to 0.1%, for a 10V step.

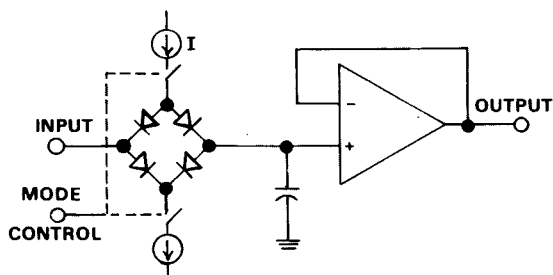


Figure 5. Switched Current Sources for Shorter Acquisition Time

#### Feedback Circuits (Figures 6 & 7)

The circuits of Figures 3, 4, 5 have the essential advantage of potentially fast acquisition and settling, but they are open-loop devices. If low-frequency tracking accuracy is more important than speed, the cascaded configuration of Figure 4 will be less satisfactory than a configuration which is, in effect, a single amplifier, yet provides isolation. This can be accomplished by closing the loop around a storage capacitor, and using high loop gain to enforce tracking accuracy. Figure 6 shows a

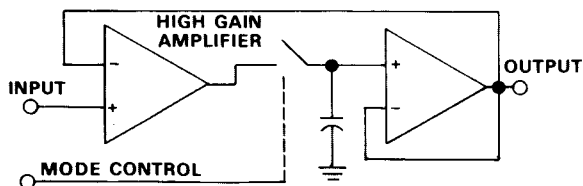


Figure 6. Track-hold Employing Feedback

\* See Vol. 5, No. 2, P. 14, for a complete practical circuit, employing a FET switch and two AD503 FET-input IC op amps

configuration in which the input follower of Figure 4 is replaced by a high-gain difference amplifier. Now, when the switch is closed, the output (which represents the charge on the capacitor) is forced to track the input, within the gain and common-mode errors and the current-driving ability of the input amplifier.

Common-mode and offset errors in the output follower are automatically compensated for by adjusting the charge on the capacitor. When the switch is opened, the output retains the final value.

In Figure 7 (a simplified schematic of the SHA-IIA, SHA-3 and SHA-4), an integrator is used, permitting the switch to operate at ground potential.

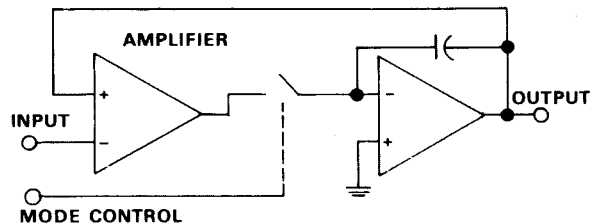


Figure 7. Feedback Track-Hold with an Integrator

In the circuits of both Figure 6 and Figure 7, because the charge on the capacitor is controlled by the output, as well as the input, the *acquisition time* and the *settling time* are identical. If the circuit of Figure 6 is switched into *hold* before the output has settled at the input value, the sample may be in error. Also, because the loop is open during *hold*, it must re-acquire the input when returned to *sample*, even if the input is unchanged. As a rule, this will result in a spike, if the input amplifier has high voltage gain.

#### Cascaded Sample-Holds (Figure 8)

If a long period of *hold* is required, in conjunction with very fast acquisition, a fast Sample-Hold, such as SHA-II, may be cascaded with one having slower acquisition but less droop. The resulting figure-of-merit can approach the product of the two.

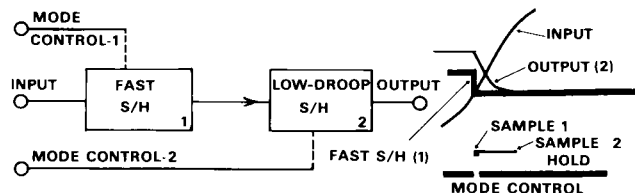


Figure 8. Use of Two Cascaded Sample-Holds for Fast Acquisition and Long Hold

#### APPLICATIONS

Sample-Holds are most-widely used in data acquisition systems, typically as shown in Figure 9. The Sample-Hold maintains the input to the A/D converter constant during the conversion interval; meanwhile, the multiplexer is seeking the next channel to be converted, either randomly or sequentially. As soon as conversion is completed, the Sample-Hold samples the newly-established input, and the cycle is repeated. This mode of operation is known as *synchronous* sampling; the Sample-Hold

operates in synchronism with the other system elements. If the input signals vary at widely disparate rates, programmed random access is necessary, to ensure that the signals with the most information are sampled most often. In another mode

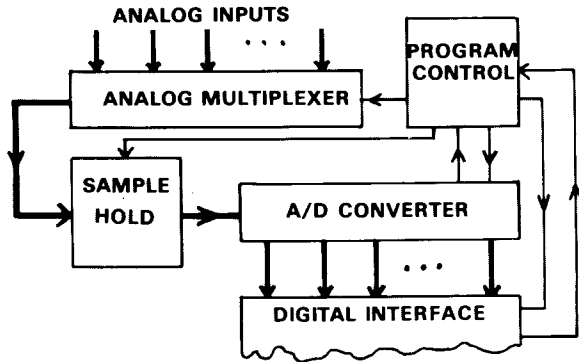


Figure 9. Typical Data-Acquisition System

(viz., *asynchronous*), a large number of Sample-Holds are used, to acquire and store data at rates pertinent to each individual channel. They are then either interrogated by analog multiplexers, or the signals are individually converted asynchronously, then multiplexed digitally, sometimes after preliminary digital processing.\*

In data distribution, 0.01% Sample-Holds may be less costly than large numbers of D/A converters having comparable accuracy. A typical data distribution system is shown in Figure 10. A fast, accurate D/A converter updates a large

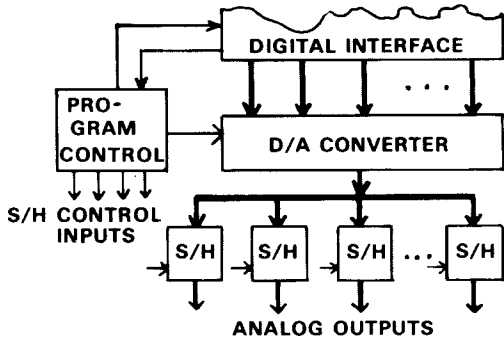


Figure 10. Data Distribution System with Analog Storage

number of Sample-Holds at speed and accuracy levels appropriate to the individual channels. Sample-Holds may be used to "de-glitch" D/A converters, in systems that are sensitive to spikes, by sampling their outputs after they've settled.

\* See the discussion of an adaptive low-redundancy data-acquisition system in *Dialogue*, Vol. 5, No. 1: "New Approaches to Data-Acquisition System Design," by Tage Anderson.

There are many applications in analog and hybrid computing and data-reduction. A typical example is shown in Figure 11: a peak follower, using a Sample-Hold and a comparator circuit. The Sample-Hold output (or the Comparator input) is biased by a few millivolts of hysteresis to avoid ambiguity during step inputs, and minimize false triggering by noise. Here's how the circuit works: When the input is greater than the S/H output, the comparator's positive output causes the S/H to track. When the input backs away and becomes less than the S/H output, the comparator's "0" output causes the S/H to *Hold* until the input once again becomes greater than the output. To reset, the control input is arbitrarily switched into *Sample*, and the lowest level contemplated is applied at the input.

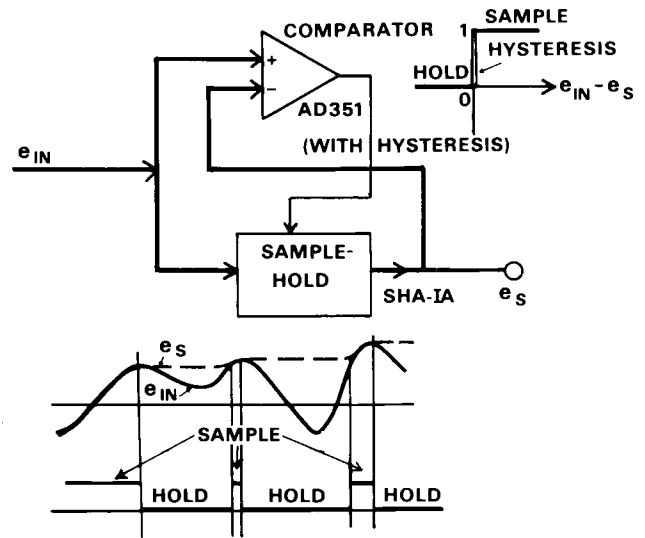


Figure 11. Peak-Follower using Sample-Hold and Comparator

The above are but a few examples of the wide applicability of these versatile modules. ▣▣▣