

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD7292 10-Bit Monitor and Control System

FEATURES

Full featured evaluation board for the AD7292
Operates from a single 5 V power supply
PC control in conjunction with the system demonstration platform (EVAL-SDP-CB1Z)
PC software for control and data analysis (time and frequency domain)
Standalone capability

ONLINE RESOURCES

Evaluation Kit Contents

EVAL-AD7292SDZ evaluation board Evaluation software CD for AD7292 USB cable Documents Needed AD7292 data sheet EVAL-AD7292SDZ user guide Required Software

EVAL-AD7292SDZ evaluation software Design and Integration Files Schematics, layout files, bill of materials

EQUIPMENT NEEDED

EVAL-AD7292SDZ evaluation board EVAL-SDP-CB1Z system demonstration platform Precision analog signal source SMB connectors/cables USB cable PC running Windows with USB 2.0 port

GENERAL DESCRIPTION

This user guide describes the evaluation board for the AD7292, which is a 10-bit monitor and control system integrated circuit with ADCs, DACs, a temperature sensor, and GPIOs. The AD7292 contains all the functions required for general-purpose monitoring of analog signals and control of external devices integrated into a single-chip solution. The AD7292 includes an 8-channel, 10-bit SAR ADC; four 10-bit DACs; a $\pm 1^{\circ}$ C accurate internal temperature sensor; and 12 GPIOs to aid system monitoring and control. Full details about the device are available in the AD7292 data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

On-board components of the evaluation board include the ADP170 low dropout, CMOS linear regulator and the AD8066 high speed, low noise amplifier. The evaluation board can be used in conjunction with the SDP demonstration platform or in standalone mode. The Link Configuration Options section of this user guide should be consulted when configuring the device for standalone operation.

TABLE OF CONTENTS

Features 1
Online Resources
Equipment Needed 1
General Description
Revision History
Functional Block Diagram
Getting Started
Quick Start Steps 4
Software Installation Procedures5
Evaluation Board Setup Procedures
Evaluation Board Hardware9
Power Supplies
Input Signals9
Output Signals9

Link Configuration Options	10
Evaluation Board Circuitry	12
Overview	12
Sockets and Connectors	12
Modes of Operation	13
Serial Interface Mode	13
Standalone Mode	13
How to Use the Software for Evaluating the AD7292	14
Setting Up the System for Data Capture	14
Overview of the Main Window	15
Evaluation	17
Evaluation Procedures for EVAL-AD7292SDZ	17
Related Links	25

REVISION HISTORY

10/12—Revision 0: Initial Revision

FUNCTIONAL BLOCK DIAGRAM

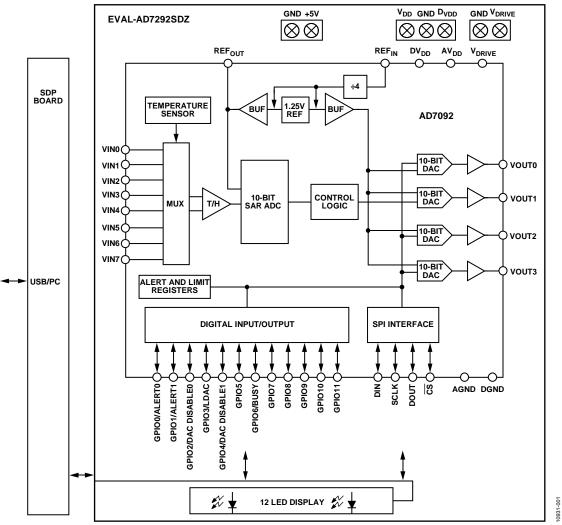


Figure 1.

GETTING STARTED QUICK START STEPS

To begin using the evaluation board, do the following:

- With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, install the AD7292 evaluation board software from the CD included in the evaluation board kit. The PC must be restarted after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)
- 2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7292SDZ board as shown in Figure 2.
 - a. Screw the two boards together using the nylon screwnut set included in the evaluation board kit to ensure that the boards are connected firmly together.

- 3. Connect a 5 V dc power supply to Connecter J3 on the EVAL-AD7292SDZ board.
- Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable. If you are using Windows[®] XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.
- Launch the EVAL-AD7292SDZ software from the Analog Devices subfolder in the Programs menu.
- 6. If it is required to use the EVAL-AD7292SDZ board with an application specific development board, review the Modes of Operation section.

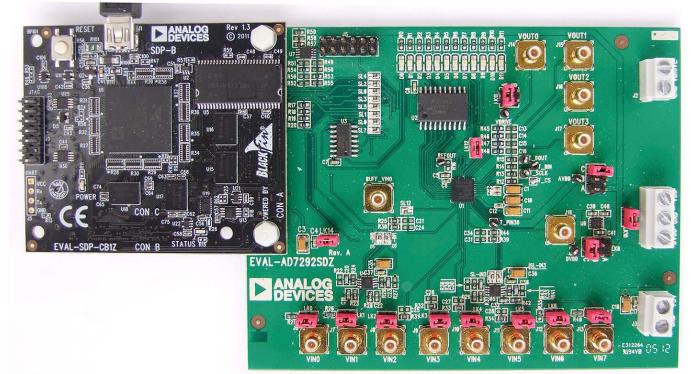


Figure 2. Hardware Configuration—Setting Up the EVAL-AD7292SDZ (EVAL-SDP-CB1Z on Left and EVAL-AD7292SDZ on Right)

SOFTWARE INSTALLATION PROCEDURES

The EVAL-AD7292SDZ evaluation kit includes a CD containing software to be installed on your PC before you begin using the evaluation board.

There are two parts to the installation:

- AD7292 evaluation board software installation
- EVAL-SDP-CB1Z system demonstration platform board drivers installation

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Installing the AD7292 Evaluation Board Software

To install the AD7292 evaluation board software,

- With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.
- Double-click the setup.exe file to begin the evaluation board software installation. The software is installed to the following default location: C:\Program Files\Analog Devices\AD7292.
- 3. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.



Figure 3. AD7292 Evaluation Software Installation: Granting Permission for Program to Make Changes Select the location to install the software, and then click Next. (Figure 4 shows the default locations, which are displayed when the window opens, but you can select another location by clicking Browse.)

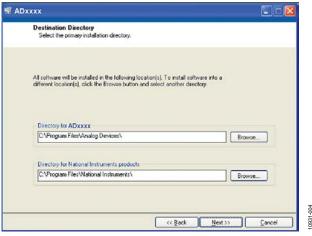


Figure 4. AD7292 Evaluation Software Installation: Selecting the Location for Software Installation

5. A license agreement appears. Read the agreement, and then select **I accept the License Agreement** and click **Next**.

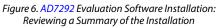
I ADXXXX	
License Agreement You must accept the license(s) displayed below to proceed.	
NATIONAL INSTRUMENTS SOFTWARE LICENSE AGREE	
INSTALLATION NOTICE: THIS IS A CONTRACT. BEFORE YOU DOWNLOAD THE SOFTW AND/OR COMPLETE THE INSTALLATION PROCESS, CAREFULLY READ THIS AGREEM DOWNLOAND'THE SOFTWARE AND/OR CLICKING THE APPLICABLE BUTTON TO COMPLETE THE INSTALLATION PROCESS, YOU CONSENT TO THE TERMS OF THIS AGREEMENT AND YOU AGREE TO BE BOUND BY THIS AGREEMENT, IF YOU DO NOT BECOME A PARTY TO THIS AGREEMENT AND BE BOUND BY ALL OF ITS TERMS AND CONDITIONS, CLICK THE APPROPRIATE BUTTON TO CANCEL THE INSTALLATION PR DO NOT INSTALL OR YOU FILS SOFTWARE, AND RETURN THE SOFTWARE WITHINT (30) DAYS OF RECEIPT OF THE SOFTWARE, WITH ALL ACCOMPANYING WRITTEN MAI ALONG WITH THEIR CONTINNERS) TO THE PLACE YOU DO NOT. INS THEN ALL RETUR SHALL BE SUBJECT TO N'S THEN CURRENT RETURN POLICY.	IENT. BY MISH TO ROCESS, HIRTY FERIALS,
Level a start to so that a second to	<u>×</u>
(e) accept the License Agreement.	
O I do not accept the License Agreeme	nt.
<< Back Next >>	Cancel

Figure 5. AD7292 Evaluation Software Installation: Accepting the License Agreement

10931-005

6. A summary of the installation is displayed. Click **Next** to continue.

Start Installation				
Review the following sum	nary before continuing.			
Adding or Changing +ADxxxx Files				
ck the Next button to begin installati	on. Click the Back button	to change the inst	allation settings	



7. A dialog box informs you when the installation is complete. Click **Next**.

🛒 ADxxxx	
Installation Complete	
The installer has finished updating your system	
	<< <u>R</u> ack Next>> Frish

Figure 7. AD7292 Evaluation Software Installation: Indicating When the Installation is Complete

010

093

Installing the EVAL-SDP-CB1Z System Demonstration **Platform Board Drivers**

After the installation of the evaluation software is complete, a welcome window is displayed for the installation of the EVAL-SDP-CB1Z system demonstration platform board drivers.

With the EVAL-SDP-CB1Z board still disconnected from 1. the USB port of the PC, make sure that all other applications are closed, and then click Next.



Figure 8. EVAL-SDP-CB1Z Drivers Setup: Beginning the Drivers Installation

Select the location to install the drivers, and then click Next. 2.

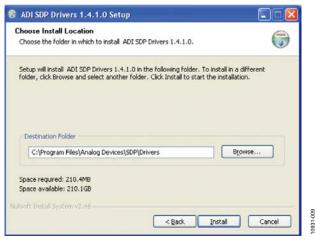


Figure 9. EVAL-SDP-CB1Z Drivers Setup: Selecting the Location for Drivers Installation

Click Install to confirm that you would like to install the 3. drivers.

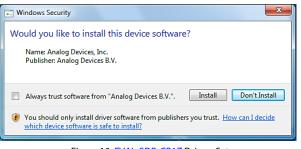


Figure 10. EVAL-SDP-CB1Z Drivers Setup: Granting Permission to Install Drivers

4. To complete the drivers installation, click Finish, which closes the installation wizard.



Completing the Drivers Setup Wizard

5. Before using the evaluation board, you must restart your computer.

008

EVALUATION BOARD SETUP PROCEDURES

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Boards

- 1. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7292SDZ board as shown in Figure 2.
 - a. Screw the two boards together using the nylon screwnut set included in the evaluation board kit to ensure that the boards are connected firmly together.
- 2. Connect a 5 V dc power supply to Connecter J3 of the EVAL-AD7292SDZ board.
- 3. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable.
- 4. If it is required to use the EVAL-AD7292SDZ board with an application specific development board, review the Modes of Operation section.

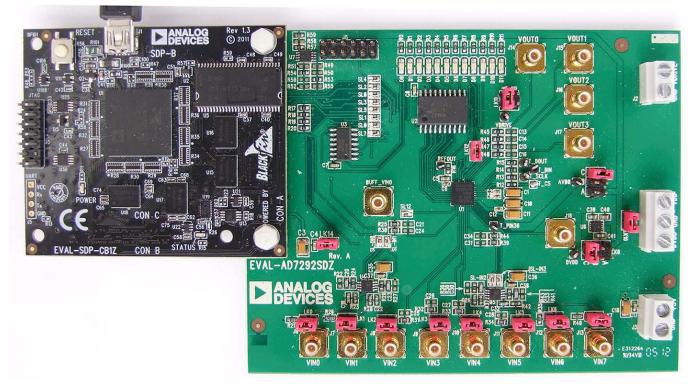


Figure 12. Hardware Configuration—Setting Up the EVAL-AD7292SDZ (EVAL-SDP-CB1Z on Left and EVAL-AD7292SDZ on Right) 10931-028

EVALUATION BOARD HARDWARE POWER SUPPLIES

When the EVAL-AD7292SDZ board is used in conjunction with the EVAL-SDP-CB1Z board (serial interface mode), the V_{DRIVE} supply is provided from the SDP board. A 5 V supply should be applied to J3. Each supply is decoupled on the EVAL-AD7292SDZ board. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

INPUT SIGNALS

There are eight input channels, VIN0 to VIN7, where an input signal between 0 V and 5 V can be applied. Refer to the schematic diagram that is available on the EVAL-AD7292SDZ Web page. VIN2 to VIN5 are directly connected to the AD7292 device inputs via a 22 Ω resistor, and provision for a low-pass filter capacitor is available on the PCB. The links on each of these

inputs hold the input to GND and should be removed when using any of the inputs $V_{\rm IN2}$ to $V_{\rm IN5}.$

The other inputs—VIN0, VIN1, VIN6, and VIN7—are buffered through a AD8066 device in a noninverting configuration. The links on each of these inputs hold the input to GND via a 50 Ω resistor.

OUTPUT SIGNALS

There are four output channels, V_{OUT0} to V_{OUT3} , where an output signal between 0 V and 5 V can be generated by the internal DACs. The outputs are directly connected to the AD7292 device outputs via a 0 Ω resistor, and provision for a low-pass filter capacitor is available on the PCB. Refer to the schematic diagram that is available on the EVAL-AD7292SDZ Web page.

LINK CONFIGURATION OPTIONS

There are multiple link (LKn) and solder link (SLn) options that must be set correctly to select the appropriate operating setup before you begin using the evaluation board. The functions of these options are outlined in Table 1.

Setup Conditions

Link

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode. There are two modes in which to operate the evaluation board. The evaluation board can be operated in

serial interface mode to be used with the SDP board, or the evaluation board can be used in standalone mode.

Table 2 shows the position in which all the links are set when the evaluation board is packaged. When the board is shipped, it is assumed that the user is operating with the SDP board. The links are set so that the control signals and VDRIVE are supplied by the SDP board. An external 5 V dc power supply must be applied to External Connector J3.

Table 1. Link Option Functions Eunstian

Link	Function
LK0	When inserted, this link connects the VIN0 input to a 50 Ω input resistor tied to ground. The input is floating when this link is not inserted.
LK1	When inserted, this link connects the VIN1 input to a 50 Ω input resistor tied to ground. The input is floating when this link is not inserted.
LK2	When inserted, this link connects the VIN2 input to ground. The input is floating when this link is not inserted.
LK3	When inserted, this link connects the VIN3 input to ground. The input is floating when this link is not inserted.
LK4	When inserted, this link connects the VIN4 input to ground. The input is floating when this link is not inserted.
LK5	When inserted, this link connects the VIN5 input to ground. The input is floating when this link is not inserted.
LK6	When inserted, this link connects the VIN6 input to a 50 Ω input resistor tied to ground. The input is floating when this link is not inserted.
LK7	When inserted, this link connects the VIN7 input to a 50 Ω input resistor tied to ground. The input is floating when this link is not inserted.
LK8	This link option determines the voltage applied to the DVDD pin of the AD7292.
	In Position A, the internal 3.3 V supply is applied to the DVDD pin.
	In Position B, the voltage applied to Jumper J4-1 is applied to the DVDD pin.
	In Position C, the 5 V supply is applied to the DVDD pin if the 5 V supply is connected to the J3 connector.
LK9	This link option determines the voltage applied to the AVDD pin of the AD7292.
	In Position A, the internal 3.3 V supply is applied to the AVDD pin.
	In Position B, the voltage applied to Jumper J4-3 is applied to the AVDD pin.
	In Position C, the 5 V supply is applied to the AVDD pin if the 5 V supply is connected to the J3 connector.
LK10	When this link is inserted, Jumper Connections J4-1 (which is connected to DVDD) and J4-3 (which is connected to AVDD) are tied together.
LK11	In Position A, the V _{DRIVE} voltage is supplied by the SDP VIO_CONNECTOR from the SDP board.
	In Position B, the V _{DRIVE} voltage must be supplied via External Connector J2.
LK12	When inserted, this link connects Pin 14 of the AD7292 to ground.
LK14	When inserted, this link connects the 5 V supply to Pin 1 of the SDP connector (J1).
SL-IN0	This solder link option determines whether an input amplifier is used on the VINO analog input channel.
SE IIIO	In Position A, there is no amplifier included in the analog input channel path.
	In Position B, there is an amplifier included in the analog input channel path.
SL-IN1	This solder link option determines whether an input amplifier is used on the VIN1 analog input channel.
	In Position A, there is no amplifier included in the analog input channel path.
	In Position B, there is an amplifier included in the analog input channel path.
SL-IN2	This solder link option determines whether an input amplifier is used on the VIN6 analog input channel.
52 1112	In Position A, there is no amplifier included in the analog input channel path.
	In Position B, there is an amplifier included in the analog input channel path.
SL-IN3	This solder link option determines whether an input amplifier is used on the VIN7 analog input channel.
SEINS	In Position A, there is no amplifier included in the analog input channel path.
	In Position B, there is an amplifier included in the analog input channel path.
SL0	This solder link option determines whether the GPIO0 pin is routed to the GPIO0 connector of the SDP board or to Connector J5-1.
SEC	In Position A, the pin is routed to the GPIO0 connector of the SDP.
	In Position B, the pin is routed to Connector J5-1.
SL1	This solder link option determines whether the GPIO1 pin is routed to the GPIO1 connector of the SDP board or to Connector J5-2.
JET	In Position A, the pin is routed to the GPIO1 connector of the SDP.
	In Position B, the pin is routed to Connector J5-2.
SL2	This solder link option determines whether the GPIO2 pin is routed to the GPIO2 connector of the SDP board or to Connector J5-3.
JLL	In Position A, the pin is routed to the GPIO2 connector of the SDP.
	In Position B, the pin is routed to the Groz connector of the SDF.
SL3	This solder link option determines whether the GPIO3 pin is routed to the GPIO3 connector of the SDP board or to Connector J5-4.
563	In Position A, the pin is routed to the GPIO3 connector of the SDP.
	In Position B, the pin is routed to the GPIOS connector of the SDP.

Link	Function
SL4	This solder link option determines whether the GPIO4 pin is routed to the GPIO4 connector of the SDP board or to Connector J5-5.
	In Position A, the pin is routed to the GPIO4 connector of the SDP.
	In Position B, the pin is routed to Connector J5-5.
SL5	This solder link option determines whether the GPIO5 pin is routed to the GPIO5 connector of the SDP board or to Connector J5-6.
	In Position A, the pin is routed to the GPIO5 connector of the SDP.
	In Position B, the pin is routed to Connector J5-6.
SL6	This solder link option determines whether the GPIO6 pin is routed to the GPIO6 connector of the SDP board or to Connector J5-7.
	In Position A, the pin is routed to the GPIO6 connector of the SDP.
	In Position B, the pin is routed to Connector J5-7.
SL7	This solder link option determines whether the GPIO7 pin is routed to the GPIO7 connector of the SDP board or to Connector J5-8.
	In Position A, the pin is routed to the GPIO7 connector of the SDP.
	In Position B, the pin is routed to Connector J5-8.
SL12	This solder link option determines whether the voltage from SL-INO is routed to the VINO SMB connector or to the BUFF_VINO SMB connector.
	In Position A, the input is routed to SMB Connector VINO.
	In Position B, the input is routed to SMB Connector BUFF_VIN0.

Table 2. Default Link Positions for Packaged EVAL-AD7292SDZ

Link No.	Position	Function
LK0	Inserted	Connects the VIN0 input to a 50 Ω input resistor tied to ground.
LK1	Inserted	Connects the VIN1 input to a 50 Ω input resistor tied to ground.
LK2	Inserted	Connects the VIN2 input to ground.
LK3	Inserted	Connects the VIN3 input to ground.
LK4	Inserted	Connects the VIN4 input to ground.
LK5	Inserted	Connects the VIN5 input to ground.
LK6	Inserted	Connects the VIN6 input to a 50 Ω input resistor tied to ground.
LK7	Inserted	Connects the VIN7 input to a 50 Ω input resistor tied to ground.
LK8	Position C	Connects DVDD to 5 V.
LK9	Position C	Connects AVDD to 5 V.
LK10	Inserted	Connects DVDD and AVDD together (via J4-1 and J4-3).
LK11	Position A	V _{DRIVE} voltage is supplied by the SDP board VIO_CONNECTOR.
LK12	Inserted	Connects Pin 14 of the AD7292 to ground.
LK14	Inserted	Connects the 5 V supply to Pin 1 of J1 to supply power to the SDP board.
SL-IN0	Position B	Amplifier U4-A is included on the analog input channel path from SMB Connector VIN0.
SL-IN1	Position B	Amplifier U4-B is included on the analog input channel path from SMB Connector VIN1.
SL-IN2	Position B	Amplifier U5-A is included on the analog input channel path from SMB Connector VIN6.
SL-IN3	Position B	Amplifier U5-B is included on the analog input channel path from SMB Connector VIN7.
SL0	Position A	Signal to/from GPIO0 pin is routed to GPIO0 connector of the SDP.
SL1	Position A	Signal to/from GPIO1 pin is routed to GPIO1 connector of the SDP.
SL2	Position A	Signal to/from GPIO2 pin is routed to GPIO2 connector of the SDP.
SL3	Position A	Signal to/from GPIO3 pin is routed to GPIO3 connector of the SDP.
SL4	Position A	Signal to/from GPIO4 pin is routed to GPIO4 connector of the SDP.
SL5	Position A	Signal to/from GPIO5 pin is routed to GPIO5 connector of the SDP.
SL6	Position A	Signal to/from GPIO6 pin is routed to GPIO6 connector of the SDP.
SL7	Position A	Signal to/from GPIO7 pin is routed to GPIO7 connector of the SDP.
SL12	Position B	Signal from SL-IN0 is routed to the BUFF_VIN0 SMB connector.

EVALUATION BOARD CIRCUITRY overview

The circuitry contained within the EVAL-AD7292SDZ board is designed to operate from a single 5 V power supply. It is also possible to connect an application specific power supply voltage to Connector J4 or to use the internal 3.3 V regulator based on the ADP170 device.

There are eight input channels, VIN0 to VIN7, where an input signal between 0 V and 5 V can be applied. VIN2 to VIN5 are directly connected to the AD7292 device inputs via a 22 Ω resistor, and provision for a low-pass filter capacitor is available on the PCB. The links on each of these inputs hold the input to GND and should be removed when using any of the following inputs: VIN2 to VIN5. The other inputs—VIN0, VIN1, VIN6, and VIN7—are buffered through a AD8066 device in a noninverting configuration. The links on each of these inputs hold the input to GND via a 50 Ω resistor.

The internal 1.25 V voltage reference of the AD7292 is used and allows a programmable voltage input range from 0 V to 1.25 V, 2.5 V, or 5 V and can be programmed for each input channel individually.

There are four output channels, VOUT0 to VOUT3, where an output signal between 0 V and 5 V can be generated by the internal DACs. The outputs are directly connected to the AD7292 device outputs via a 0 Ω resistor, and provision for a low-pass filter capacitor is available on the PCB.

The GPIO pins of the AD7292 are connected to a bank of LEDs and are also made available to PCB Header J5 via the SL0 to SL7 solder links.

SOCKETS AND CONNECTORS

There are 13 SMB input sockets and five tab connectors that affect the operation of the AD7292 on this evaluation board. When operating the board with the SDP board, an external 5 V supply is required for the AD7292 board. The functions of the SMB sockets are outlined in Table 3.

Socket	Function
VIN0 to VIN7	SMB socket for a single-ended input that is applied to the VIN0 to VIN7 pins of the AD7292.
VOUT0 to VOUT4	SMB socket for a single-ended output that comes from the VOUT1 to VOUT4 pins of the AD7292.
BUFF_VIN0	SMB socket for the buffered VIN0 input. (SL-IN0 and SL12 must be in Position B.)
J1	This connector connects the AD7292 board to the SDP board.
J2	In standalone mode, VDRIVE should be supplied via this connector. (LK11 must be in Position B.)
J3	Connect a 5 V supply to this input.
J4	This connection provides the user with the option of connecting external voltages for the DVDD and AVDD pins. (If different voltages are required at these pins, ensure that LK10 is removed.)
J5	This 14-pin header connects to the GPIO pins of the AD7292.

MODES OF OPERATION

SERIAL INTERFACE MODE

The AD7292 uses a high speed serial interface that allows sampling rates of up to 1 MSPS. For more information about the operation of the serial bus, refer to the AD7292 data sheet.

The EVAL-AD7292SDZ communicates with the EVAL-SDP-CB1Z board using level shifters. The EVAL-SDP-CB1Z operates at a 3.3 V logic level, which allows V_{DRIVE} voltages that exceed 3.3 V to be used without damaging the SDP interface.

Details about the serial interface can be found in the AD7292 data sheet.

SDP Limitations

Due to software limitations of the EVAL-SDP-CB1Z, high sample rates entered into the dialog box may not reflect the

actual sample rate running on the AD7292. In this case, the analysis results will not show true values. This may occur if the value for SCLK is too slow for a given sample rate entered.

This limitation does not apply when using the EVAL-AD7292SDZ in standalone mode.

STANDALONE MODE

The EVAL-AD7292SDZ can also be used without the EVAL-SDP-CB1Z controller board. In this case, the customer application board is connected to the digital interface using the J5 header connector (or, if preferred, using the test points), an external V_{DRIVE} voltage (ranging from 1.8 V to 5.25 V) is connected to J2, and LK11 is moved to Position B. Refer to the schematic diagram that is available on the EVAL-AD7292SDZ Web page for more details.

HOW TO USE THE SOFTWARE FOR EVALUATING THE AD7292

SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Software Installation Procedures and Evaluation Board Setup Procedures sections, set up the system for data capture as follows:

- 1. Allow the Found New Hardware Wizard to run after the EVAL-SDP-CB1Z board is plugged into your PC. (If you are using Windows XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.)
- 2. Check that the board is connecting to the PC correctly using the **Device Manager** of the PC.
 - a. Access the **Device Manager** as follows:
 - i. Right-click My Computer and then click Manage.
 - ii. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.
 - iii. The Computer Management box appears. Click Device Manager from the list of System Tools (see Figure 13).
 - b. The EVAL-SDP-CB1Z board should appear under ADI Development Tools. This indicates that the driver software is installed and that the board is connecting to the PC correctly.

Eile Action View Help		
🗢 🤿 🙍 🔂 🚺 😥 👘		
Computer Management (Local System Tools Carlot Gashed Content of the second of the second of the second second of the second	ADI Development Tools ADI Development Tools ADI Development Tools Development Platform (32MB) Disk drives Disk drives	

Figure 13. Device Manager: Checking that the Board Is Connected to the PC Correctly

Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, launch the AD7292 software as follows:

- From the Start menu, select Programs > Analog Devices > AD7292. The main window of the software then displays.
- 2. If the AD7292 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 14). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and then follow the onscreen instructions.

🖻 Hardware Select 🛛 🔀			
No matching system found. Press Rescan to retry or Cancel to abort.			
Previous Next			
Rescan Select Cancel			

Figure 14. Connectivity Error Alert

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the generic SDP attached to the PC is detected, and then the main window appears (see Figure 15).

Evaluation Board User Guide

EVAL-AD7292SDZ

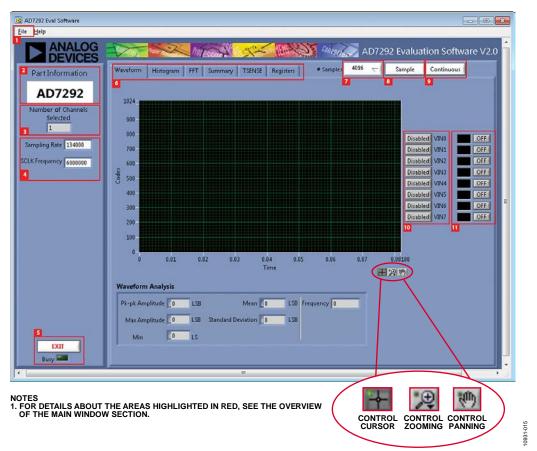


Figure 15. Evaluation Software Main Window: Setup Screen

OVERVIEW OF THE MAIN WINDOW

The main window of the software is shown in Figure 15 and has the features described in this section.

File Menu (Section 1)

The File menu (labeled 1 in Figure 15) offers the choice to

- Load data: load previously captured data or example files in .tsv (tab separated values) format for analysis (see Figure 16). (The default location for the example files is C:\Program Files\Analog Devices\AD7292\examples.)
- **Save Data as .tsv**: save captured data in .tsv format for future analysis (see Figure 17).
- **Print Front Panel Picture**: print the main window to your default printer.
- **Save Picture**: save the current screen capture.
- Exit: quit the application.



Figure 16. Load File Dialog Box: Loading Previously Captured Data or Example Files in .tsv Format

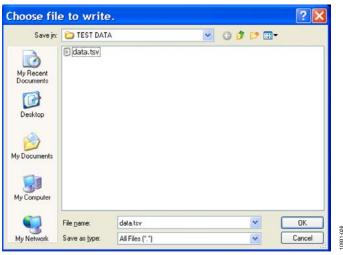


Figure 17. Save File Dialog Box: Saving Data as .tsv

Part Information Box (Section 2)

The **Part Information** box (labeled 2 in Figure 15) displays the generic being evaluated and is for informational purposes only.

Number of Channels Selected Box (Section 3)

The **Number of Channels Selected** box (labeled 3 in Figure 15) shows the total number of input channels that are enabled.

Sampling Rate and SCLK Frequency Boxes (Section 4)

The values entered into the **Sampling Rate** and **SCLK Frequency** boxes (labeled 4 in Figure 15) affect one another. The default sampling frequency matches the maximum sample rate of the ADC selected from the drop-down menu. Although you can adjust the sampling frequency, there are limitations in terms of the sample frequencies that can be entered. If an unusable sample frequencies is input, the software automatically adjusts the sample frequency accordingly. Units can be entered as, for example, 10k for 10,000 Hz. Because the maximum sample frequency is device dependent—some of the ADCs are capable of operating at up to 250 ksps while others can run to 1.3 MSPS—the software automatically adjusts the sample frequency according to the ability of the ADC being evaluated. For example, if you enter a value

that is beyond the ability of the device, the software indicates this and reverts to the maximum sample frequency.

Exit Button (Section 5)

Clicking **Exit** (labeled 5 in Figure 15) closes the software. Alternatively, you can select **Exit** from the **File** menu.

Tabs Area (Section 6)

There are six tabs available in the tabs area (labeled 6 in Figure 15) of the main window: **Waveform**, **Histogram**, **FFT**, **Summary**, **TSENSE**, and **Registers**. These tabs display ADC data in different formats, and the Registers tab allows you to change the register configuration settings. Navigation tools are provided within each tab, with the exception of the **Registers** tab, to allow you to control the cursor, zooming, and panning (see Figure 15).

Each tab is described in more detail in the Generating a Waveform Analysis Report; Generating a Histogram of the ADC Code Distribution; Generating a Fast Fourier Transform of AC Characteristics; Generating a Summary of the Waveform, Histogram, and Fast Fourier Transform; Displaying Temperature Measurements; and Modifying Control Register Settings sections.

Samples Box (Section 7)

The **# Samples** box (labeled 7 in Figure 15) allows you to select the number of samples to analyze.

Sample Button (Section 8)

Clicking Sample (labeled 8 in Figure 15) performs a single capture.

Continuous Button (Section 9)

Clicking **Continuous** (labeled 9 in Figure 15) performs a continuous capture from the ADC. Clicking **Continuous** a second time stops sampling.

Enable ADC Input Channels Buttons (Section 10)

Clicking the buttons in this area (labeled 10 in Figure 15) enable or disable the respective ADC input channels.

Channel Display Buttons (Section 11)

Clicking the buttons in this area (labeled 11 in Figure 15) allows you to display multiple channel reads. (Note that for FFT analysis, you can select only one channel to be displayed.)

EVALUATION EVALUATION PROCEDURES FOR EVAL-AD7292SDZ

Generating a Waveform Analysis Report

Figure 18 illustrates the waveform capture tab for a 5 V p-p, 1 kHz sine wave input signal.

The **Waveform Analysis** area reports the amplitudes recorded from the captured signal.

To scale the x-axis of the waveform diagram, right-click on the rightmost value and clear the autoscale function from the menu that appears. Then enter the required value.

To scale the y-axis of the waveform diagram, right-click on the topmost value and clear the autoscale function from the menu that appears. Then enter the required value.

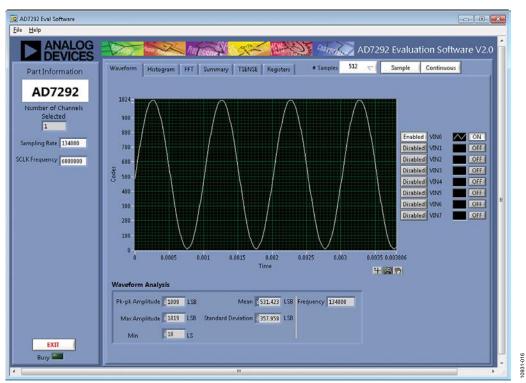


Figure 18. Waveform Tab

Generating a Histogram of the ADC Code Distribution

The **Histogram** tab can be used to perform ac testing or, more commonly, dc testing. This tab shows the ADC code distribution of the input and computes the mean and standard deviation, which are displayed as **Mean** and **Transition Noise**, respectively, in the **Histogram Analysis** area (see Figure 19).

Figure 19 shows the histogram for a 5 V p-p, 1 kHz sine wave applied to the ADC input and the resulting calculations.

AC Input

To perform a histogram test of ac input,

- 1. Apply a signal source to the VIN0 to VIN7 input connectors.
- 2. Click the **Histogram** tab from the main window.
- 3. Click Sample.

Raw data is then captured and passed to the PC for statistical computations, and various measured values are displayed in the **Histogram Analysis** area.

DC Input

To perform a histogram test of dc input,

- 1. If an external source is being used, apply a signal source.
- 2. Click the **Histogram** tab from the main window.
- 3. Click Sample.

Raw data is then captured and passed to the PC for statistical computations, and various measured values are displayed in the **Histogram Analysis** area.

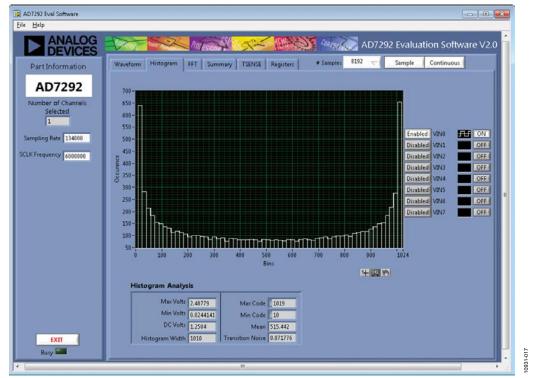


Figure 19. Histogram Tab

Generating a Fast Fourier Transform of AC Characteristics

Figure 20 shows the **FFT** tab. This feature tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results.

To perform an ac FFT test,

- 1. Apply a sinusoidal signal with low distortion (better than 115 dB) to the evaluation board. To attain the requisite low distortion, which is necessary to allow true evaluation of the part, one option is to
 - a. Filter the input signal from the ac source. Choose an appropriate band-pass filter based on the sinusoidal signal applied.
 - b. If a low frequency band-pass filter is used when the full-scale input range is more than a few volts peak-to-peak, use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

- 2. Click the **FFT** tab from the main window.
- 3. Click Sample.

As in the histogram test, raw data is then captured and passed to the PC, which performs the FFT and displays the resulting SNR, THD, and SINAD.

The **Spectrum Analysis** box displays the results of the captured data.

- The area labeled 1 in Figure 20 shows the input signal information.
- The area labeled 2 in Figure 20 displays the fundamental frequency and amplitude in addition to the second to fifth harmonics.
- The area labeled 3 in Figure 20 displays the performance data, including the SNR, THD, and SINAD.

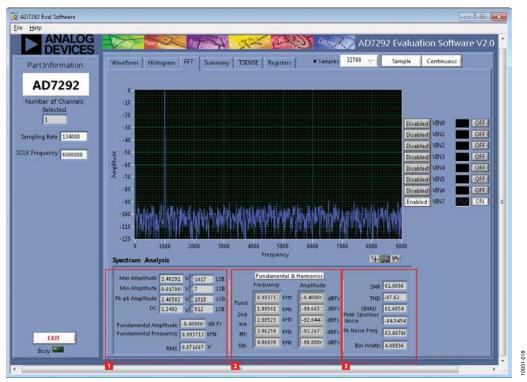


Figure 20. FFT Tab

Generating a Summary of the Waveform, Histogram, and Fast Fourier Transform

Figure 21 shows the **Summary** tab. The **Summary** tab captures all the display information and provides it in one panel with a synopsis of the information, including key performance parameters such as SNR and THD.

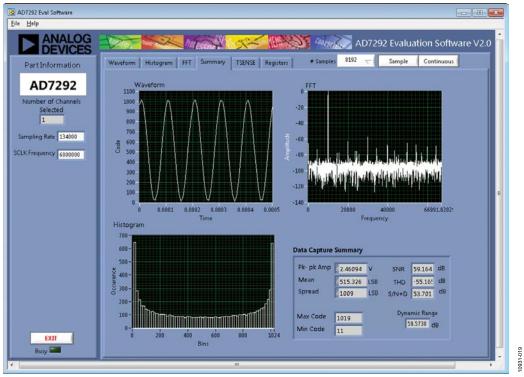


Figure 21. Summary Tab

Displaying Temperature Measurements

Figure 21 shows the **TSENSE** tab. There are two modes of operation (continuous and single sample), and the controls are located at the bottom of the panel.

Before temperature measurements can be displayed, the control bit must be set to active in the **Configuration Register Bank** (see Figure 23 and Figure 24). A digital filter can also be applied to this measurement.

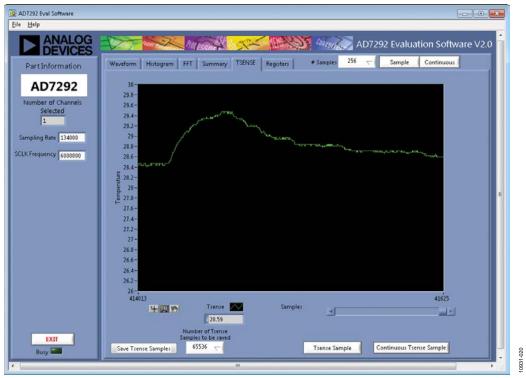


Figure 22. TSENSE Tab

Evaluation Board User Guide

Modifying Control Register Settings

Figure 23 shows the **Registers** tab. There are 87 registers used to configure the AD7292. Consult the AD7292 data sheet for a detailed explanation of each control register and an overview of the functions and features of the device.

The power-on default values for all registers are shown in Figure 24 to Figure 27.

For basic operation of the ADCs, it is not necessary to modify any of the registers directly. Provision is made on the **Waveform** tab (see Figure 18), which allows you to click **Enable** or **Disable** to select which input ADC channels are activated and to click **ON** to display the waveform of the input signal in the window.

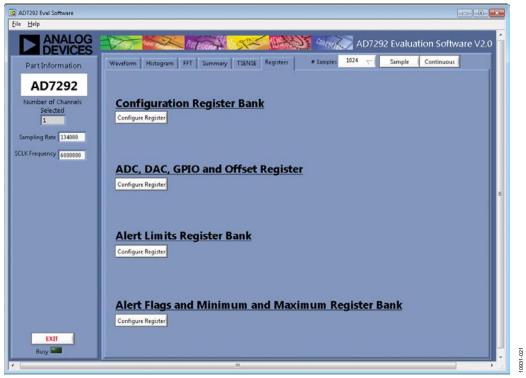


Figure 23. Registers Tab

Evaluation Board User Guide

EVAL-AD7292SDZ

10931-022

Digital Output Driver	00000		VIN Range1 Sub- 00	000000		Configuration R	enister l	R
Name Settin			Name Setti			Configuration R	egisteri	Dall
GPIO0 Output/Alert0	Disable	[0]	Set VIN0 Range	Do not divide	[0]			
GPIO1 Output/Alert1	Disable	[1]	Set VIN1 Range	Do not divide	[1]	CANCEL	OK	
GPIO2 Output/DAC DISABLE 0	Disable	[2]	Set VIN2 Range	Do not divide	[2]	CANCEL	OR	
GPIO3 Output/LDAC	Disable	[3]	Set VIN3 Range	Do not divide	[3]			
GPIO4 Output/DAC DISABLE 1	Disable	[4]	Set VIN4 Range	Do not divide	[4]	VIN Filter Sub-Register	0000000	
GPIO5 Output	Disable	[5]	Set VIN5 Range	Do not divide	[5]	Name Set	inin	
GPI06 Output/ADC Busy	Disable	[6]	Set VIN6 Range	Do not divide	[6]	Filtering of VIN0	Disable	[[0]
GPIO7 Output	Disable	[7]	Set VIN7 Range	Do not divide	[7]	Filtering of VIN1	Disable	[0]
GPIO8 Output	Disable	[8]	VIN Range0 Sub- 00	000000		Filtering of VIN2	Disable	[2]
GPIO9 Output	Disable	[9]	Name Setti	0.0		Filtering of VIN3	Disable	[3]
GPI010 Output	Disable	[10]	Set VIN0 Range	Do not divide	[0]	Filtering of VIN4	Disable	[4
GPI011 Output	Disable	[11]	Set VIN1 Range	Do not divide	[1]	Filtering of VIN5	Disable	15
Digitial VO Function	00000		Set VIN2 Range	Do not divide	[2]	Filtering of VIN6	Disable	[6
Name Settin			Set VIN3 Range	Do not divide	[3]	Filtering of VIN7	Disable	17
GPIO0 Function	ALERTO		Set VIN4 Range	Do not divide	[4]		1	10
GPIOU Function GPIO1 Function	ALER 10	[0]	Set VIN5 Range	Do not divide	[5]	GPIO2/DAC Disable0 0	0000000	
GPI01 Function		[1]	Set VIN6 Range	Do not divide	[6]	Name Set		
GPIO2 Function GPIO3 Function	DAC Disable([2]	Set VIN7 Range	Do not divide	[7]	Control VOUT0	Enable	[[0
GPIO4 Function	DAC Disable1		And a subscription of the	000000	1.1	Control VOUT1	Enable	[1
GPI05 Function	Reserved	[5]		the second se		Control VOUT2	Enable	[2
GPIO6 Function	ADC Busy	[5]	Name Setti		Bit	Control VOUT3	Enable	[3
1000	and the owner of the	[0]	VIN0 Alerts to ALERT0 pin	Disable	[0]	GPIO4/DAC Disable1	0000000	
General Sub-Register 000	00000		VIN1 Alerts to ALERT0 pin	Disable	[1]			
			VIN2 Alerts to ALERT0 pin	Disable	[2]	Name Set		
DAC disable mode control	1k and 100k r	[1:2]	VIN3 Alerts to ALERT0 pin	Disable	[3]	Control VOUT0	Enable	0]
ALERT0 Polarity	Active Low	[4]	VIN4 Alerts to ALERT0 pin	Disable	[4]	Control VOUT1	Enable	[1
Conversion Delay Sub- 1000	00000		VIN5 Alerts to ALERT0 pin	Disable	[5]	Control VOUT2	Enable	[2
Name Settin			VIN6 Alerts to ALERT0 pin	Disable	[6]	Control VOUT3	Enable	[3
Conversion Delay Control		10:151	VIN7 Alerts to ALERT0 pin	Disable	[7]	ADC Sampling Mode 0	0000000	
	0	[0.15]	VIN Alert 1 Routing Sub- 00	000000		Name Sett		
emperature Sensor	00001		Name Setti			VIN0 Single/Differential input	n Single Ende	ol be
Name Settin			VIN0 Alerts to ALERT1 pin	Disable	[0]	Measure VIN0 wrt. AVDD or A	G AVDD	[8]
Enable/Disable TSENSE Conv	Enable	[0]	VIN1 Alerts to ALERT1 pin	Disable	[1]	Measure VIN1 wrt. AVDD or A	AVDD	[9
Enable/Disable digital filtering	Disable	[8]	VIN2 Alerts to ALERT1 pin	Disable	[2]	Measure VIN2 wrt. AVDD or A	G AVDD	[1
			VIN3 Alerts to ALERT1 pin	Disable	[3]	Measure VIN3 wrt. AVDD or A	AVDD	[1
	00000		VIN4 Alerts to ALERT1 pin	Disable	[4]	Measure VIN4 wrt. AVDD or A	G AVDD	[1
Name Settin		Bit	VIN5 Alerts to ALERT1 pin	Disable	[5]	Measure VIN5 wrt. AVDD or A	G AVDD	[1
TSENSE alert to ALERT0 pin	Disable	[0]	VIN6 Alerts to ALERT1 pin	Disable	[6]	Measure VIN6 wrt. AVDD or A	G AVDD	[1
TSENSE alert to ALERT1 pin	Disable	[8]	VIN7 Alerts to ALERT1 pin	Disable	[7]	Measure VIN7 wrt. AVDD or A	G AVDD	[19

Figure 24. Configuration Register Bank Window

ADC, DAC, GPIO and	Offset Register				_			-23
						VIN0 Offset	000000	
						Name	Setting	
ADO	C, DAC, GP	IO ar	nd Offset Reg	ister		VIN0 Offset	0	[0:7]
						VIN1 Offset	000000	
						Name	Setting	
CANCEL	ок		DAC Buffer Enable	00000F		VIN1 Offset	0	[0:7]
			Name	Setting		(Internet internet)	1	
			Enable DAC0	Enable	[0]	VIN2 Offset	000000	
			Enable DAC1	Enable	[1]	Name	Setting	Ðit
ADC Sequence	000007		Enable DAC2	Enable	[2]	VIN2 Offset	0	[0:7]
Name			Enable DAC3	Enable	[3]	-	1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 -	
ADC Channel 0	Enable	[0]			1.0	VIN3 Offset	000000	
ADC Channel 1	Enable	[1]	DAC Channel 0	008AC0		Name	Setting	Bit
ADC Channel 2	Enable	[2]	Name	Setting		VIN3 Offset	0	[0:7]
ADC Channel 3	Disable	[3]	LDAC	DAC updat		-	Illennen	
ADC Channel 4	Disable	[4]	Copy	Updates or	and the second se	VIN4 Offset	000000	
ADC Channel 5	Disable	[5]	DAC0 Output	555	[6:15]	Name	Setting	
ADC Channel 6	Disable	[6]	and the second se		[0.15]	VIN4 Offset	0	[0:7]
ADC Channel 7	Disable	[7]	DAC Channel 1	008AC0				
TSENSE read back ena	able Disable	[8]	Name	Setting	Bit	VIN5 Offset	000000	
			LDAC	DAC updat	ed [0]	Name	Setting	
GPIO Register	0000FF		Сору	Updates or		VIN5 Offset	0	[0:7]
Name	Setting		DAC1 Output	555	[6:15]	VIIV5 Oliset	0	[0.7]
GPI00	High	[0]	DAC Channel 2	008AC0		VIN6 Offset	000000	
GPI01	High	[1]	Name	Setting		Name	Setting	
GPI02	High	[2]	LDAC			VIN6 Offset		
GPI03	High	[3]		DAC updat	statement and statements	VIN6 Unset	0	[0:7]
GPIO4	High	[4]	Copy DAC2 Output	Updates or 555		VIN7 Offset	000000	
GPI05	High	[5]	DAC2 Output	000	[6:15]			
GPI06	High	[6]	DAC Channel 3	008AC0		Name	Setting	
GP107	High	[7]	and the second second second	and the second se		VIN7 Offset	0	[0:7]
GPI08	Low	[8]	Name	Setting	Bit	Temp Sensor Offset	000000	
GPI09	Low	[9]	LDAC	DAC updat			and the second se	
GPI010	Low	[10]	Сору	Updates or		Name	Setting	Bit
GPI011	Low	[11]	DAC3 Output	555	(6:15)	Temp Sensor Offset	0	[0:7]

Figure 25. ADC, DAC, GPIO, and Offset Register Window

Evaluation Board User Guide

			Alert Limits	Register B	Bank	CANCEL	. ОК	
VINO ALERT LIMIT High	0000FFC0		VIN3 ALERT LIMIT High	0000FFC0		VIN6 ALERT LIMIT High	0000FFC0	
Name	Setting		Name	Setting		Name	Setting	
VINO ALERT LIMIT High	1023	[6:15]	VIN3 ALERT LIMIT High	1023	[6:15]	VIN6 ALERT LIMIT High	1023	[6
VINO ALERT LIMIT LOW	00000000		VIN3 ALERT LIMIT LOW	00000000		VING ALERT LIMIT LOW	0000000	
Name	Setting	Bit	Name	Setting	Bit	Name	Setting	
VIN0 ALERT LIMIT Low	0	[6:15]	VIN3 ALERT LIMIT Low	0	[6:15]	VIN6 ALERT LIMIT Low	0	[6
VINO Hysteresis	00000000		VIN3 Hysteresis	00000000		VIN6 Hysteresis	00000000	
			Name				Setting	
VIN0 Hysteresis	0	[6:15]	VIN3 Hysteresis	0	[6:15]	VIN6 Hysteresis	0	[6
VIN1 ALERT LIMIT High	0000FFC0		VIN4 ALERT LIMIT High	0000FFC0		VIN7 ALERT LIMIT High	0000FFC0	
Name			Name			Name		
VIN1 ALERT LIMIT High	1023	[6:15]	VIN4 ALERT LIMIT High	1023	[6:15]	VIN7 ALERT LIMIT High	1023	[8
VIN1 ALERT LIMIT LOW	00000000		VIN4 ALERT LIMIT LOW	00000000		VIN7 ALERT LIMIT LOW	00000000	
VIN1 ALERT LIMIT Low	0	[6:15]	VIN4 ALERT LIMIT LOW	0	[6:15]	VIN7 ALERT LIMIT LOW	0	[[6
/IN1 Hysteresis	00000000		VIN4 Hysteresis	00000000		VIN7 Hysteresis	00000000	
	Setting	Bit	Name		Bit	Name		
VIN1 Hysteresis	0	[6:15]	VIN4 Hysteresis	0	[6:15]	VIN7 Hysteresis	0	[6
VIN2 ALERT LIMIT High	0000FFC0		VIN5 ALERT LIMIT High	0000FFC0		TSENSE ALERT LIMIT	0000FFC0	
		Bit	Name		Bit			8
VIN2 ALERT LIMIT High	1023	[6:15]	VIN5 ALERT LIMIT High	1023	[6:15]	TSENSE ALERT LIMIT HI	gh 1023	[8
VIN2 ALERT LIMIT LOW	00000000		VIN5 ALERT LIMIT LOW	00000000		TSENSE ALERT LIMIT	00000000	
Name	Setting	Bit	Name	Setting	Bit		Setting	B
VIN2 ALERT LIMIT Low	0	[6:15]	VIN5 ALERT LIMIT Low	0	[6:15]	TSENSE ALERT LIMIT LO	w O	16
VIN2 Hysteresis	00000000		VIN5 Hysteresis	00000000		TSENSE Hysteresis	00000000	

10931-024

10931-025

Figure 26. Alert Limits Register Bank Window

			VINO Maximum Value	x 0000FFC0		VIN4 Minimum Value	× 00000000	
			Name			Name		
Alert	Flags and		VIN0 Maximum Value	1023	[6:15]	VI4 Minimum Value	0	[6:15
Minimum	and Maxim	um	VINO Minimum Value	00000000		VIN5 Maximum Value	00000000	
Ponic	ter Bank		Name	Setting		Name	Setting	
Kegis	ter bank		VIN0 Minimum Value	0	[6:15]	VIN4 Maximum Value	0	[6:15
			VIN1 Maximum Value	00000000		VIN5 Minimum Value	00000000	
CANCEL	OK		Name	Setting		Name	Setting	
			VIN1 Maximum Value	0	[6:15]	VIN5 Minimum Value	0	[6:15
ADC Alert Flags Sub-	00000000		VIN1 Minimum Value	00000000		VIN6 Maximum Value	00000000	
			Name	Setting		Name	Setting	
VINO Limit Low Flag	No Flag	[0]	VIN1 Minimum Value	0	[6:15]	VIN6 Maximum Value	0	[6:15
VIN0 Limit High Flag	No Flag	[1]	and the second se	-		(1	
VIN1 Limit Low Flag	No Flag	[2]	VIN2 Maximum Value	00000000		VIN6 Minimum Value	00000000	
VIN1 Limit High Flag	No Flag	[3]						
VIN2 Limit Low Flag	No Flag	[4]	VIN2 Maximum Value	0	[6:15]	VIN6 Minimum Value	0	[6:15
VIN2 Limit High Flag	No Flag	[5]					-	
VIN3 Limit Low Flag	No Flag	[6]	VIN2 Minimum Value	0000000		VIN7 Maximum Value	00000000	
VIN3 Limit High Flag	No Flag	[7]	Name					
VIN4 Limit Low Flag	No Flag	[8]	VIN2 Minimum Value	0	[6:15]	VIN7 Maximum Value	0	[6:15
VIN4 Limit High Flag	No Flag	[9]		1			1	
VIN5 Limit Low Flag	No Flag	[10]	VIN3 Maximum Value	00000000		VIN7 Minimum Value	00000000	
VIN5 Limit High Flag	No Flag	[11]	Name	Setting	Bit	Name	Setting	Bit
VIN6 Limit Low Flag	No Flag	[12]	VIN3 Maximum Value	0	[6:15]	VIN7 Minimum Value	0	[6:15
VIN6 Limit High Flag	No Flag	[13]	VIN3 Minimum Value	00000000		TSENSE Maximum	0000F540	
VIN7 Limit Low Flag	No Flag	[14]		and the second se				
VIN7 Limit High Flag	No Flag	[15]	Name	Setting	Bit	Name	Setting	Bit
TSENSE Alert Flags	0000FFFF		VIN3 Minimum Value	0	[6:15]	TSENSE Maximum Valu	Je 981	(6:15
Name	Setting		VIN4 Maximum Value	00000000		TSENSE Minimum	00000000	
TSENSE Limit Low Flag	TSENSE Li	mi (0)	Name	Setting		Name	Setting	
TSENSE Limit High Fla			VIN4 Maximum Value	0	[6:15]	TSENSE Minimum Valu	ie 0	[6:15

Figure 27. Alert Flags and Minimum and Maximum Register Bank Window

Rev. 0 | Page 24 of 28

RELATED LINKS

Resource	Description
ADP170	Product Page, Low Dropout CMOS Linear Regulator
AD8066	Product Page, High Speed Low Noise Amplifier
EngineerZone	Online Community, Analog Devices Online Technical Support Community
Circuits from the Lab	Reference Circuits, Circuit Designs That Have Been Built and Tested to Ensure Function and Performance and That Address Common Analog, RF/IF, and Mixed-Signal Design Challenges by Applying Analog Devices' Vast Applications Expertise

NOTES

NOTES

NOTES



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL. SPECIAL INDIRECT. OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL, ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

©2012 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. UG10931-0-10/12(0)



www.analog.com

Rev. 0 | Page 28 of 28