Hardware User Guide
UG-399

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2.25 GHz HDMI XpressView Advantiv 1:2 Splitter with 4:1 Input Mux Functionality and Features

SCOPE

This user guide provides a detailed description of the XpressView™ Advantiv® ADV7630 functionality and features.

DISCLAIMER

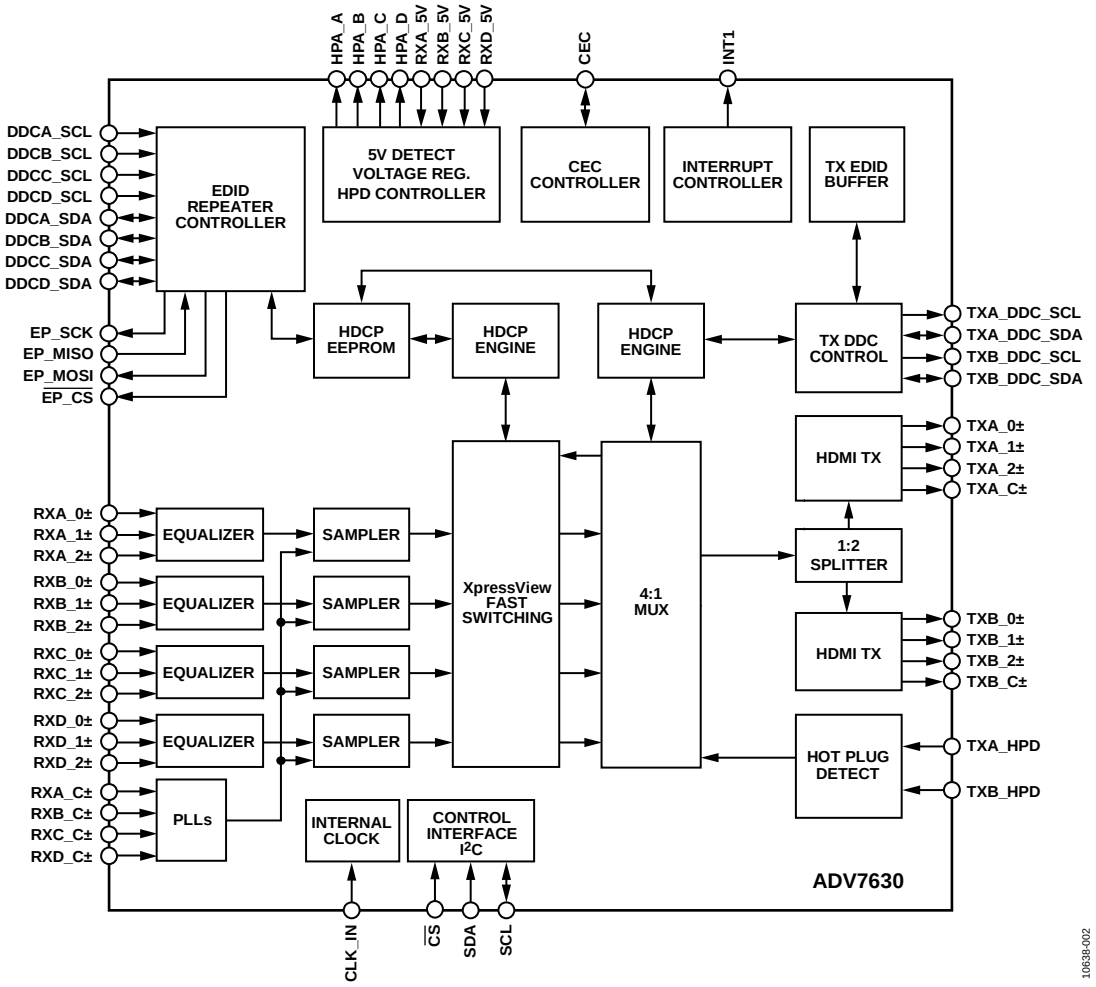

Figure 1. Functional Block Diagram

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REVISION HISTORY

9/12—Revision 0: Initial Version

USING THE ADV7630 HARDWARE USER GUIDE

NUMBER NOTATIONS

Table 1.

Notation	Description
Bit N	Bits are numbered in little endian format; that is, the least significant bit of a number is referred to as Bit 0.
V[X:Y]	Bit field representation covering Bit X to Bit Y of a value or a field (V).
0xNN	Hexadecimal (base-16) numbers are preceded by the prefix 0x.
0bNN	Binary (base-2) numbers are preceded by the prefix 0b.
NN	Decimal (base-10) are represented using no additional prefixes or suffixes.

REGISTER ACCESS CONVENTIONS

Table 2.

Mode	Description
R/W	Memory location has read and write access.
R	Memory location is read access only. A read always returns 0 unless otherwise specified.
W	Memory location is write access only.

ACRONYMS AND ABBREVIATIONS

Table 3.

Acronym/Abbreviation	Description
ACP	Audio content protection
ACR	Audio clock regeneration
ADC	Analog-to-digital converter
AFE	Analog front end
AGC	Automatic gain control
Ainfo	HDCP register (refer to HDCP documentation)
AKSV	HDCP transmitter key selection vector (refer to HDCP documentation)
An	64-bit pseudo-random value generated by HDCP cipher function of Device A
AVI	Auxiliary video information
Aux	Auxiliary
BCAPS	HDCP register (refer to HDCP documentation)
BGA	Ball grid array
BKSV	HDCP receiver key selection vector (refer to HDCP documentation)
CP	Component processor
CDC	CEC discovery control
CEC	Consumer electronics control
CSC	Color space converter/conversion
CSync	Composite synchronization
CTS	Cycle time stamp
DCM	Decimation
DDR	Double data rate
DDFS	Direct digital frequency synthesizer
DE	Data enable
DID	Data identification word
DLL	Delay locked loop
DNR	Digital noise reduction
DPP	Data preprocessor
DUT	Device under test (designate the ADV7630, unless stated otherwise)
DVI	Digital visual interface
EAV	End of active video
ED	Enhanced definition
EMC	Electromagnetic compatibility
EQ	Equalizer
E-EDID	Extended EDID
HBR	High bit rate
HD	High definition
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High definition television

Acronym/Abbreviation	Description
HPD	Hot Plug detect
HSync	Horizontal synchronization
IC	Integrated circuit
ISRC	International standard recording code
I^2S	Inter IC sound
I^2C	Inter integrated circuit
GCP	General control packet
GMP	Gamut metadata packet
KSV	Key selection vector
LLC	Line locked clock
LSB	Least significant bit
L-PCM	Linear pulse coded modulated
Mbps	Megabit per second
MPEG	Moving Picture Experts Group
ms	Millisecond
MSB	Most significant bit
NC	No connect
OSD	On screen display
OTP	One time programmable
PAR	Parallel
Pj'	HDCP enhanced link verification response (refer to HDCP documentation)
Ri'	HDCP link verification response (refer to HDCP documentation)
Rx	Receiver
SA	Slave address
SAV	Start of active video
SD	Standard definition
SDP	Standard definition processor
SDR	Single data rate
SHA-1	Refer to HDCP documentation
SMPTE	Society of Motion Picture and Television Engineers
SNR	Signal-to-noise ratio
SOG	Sync on green
SOY	Sync on Y
SPA	Source physical address
SPD	Source production descriptor
SRM	System renewability message
SSPD	Synchronization source polarity detector
STDI	Standard identification
TBC	Timebase correction
TMDS	Transition minimized differential signaling
Tx	Transmitter
US	Up sampling
VBI	Video blanking interval
VDP	VBI data processor
VIC	Video identification code
VSync	Vertical synchronization
XTAL	Crystal oscillator

FIELD FUNCTION DESCRIPTIONS

Throughout this user guide, a series of function tables is provided. The function of a field is described in a table preceded by the bit name, a short function description, the I²C map, the register location within the I²C map, and a detailed description of the field.

The detailed description consists of:

- For a readable field, the values the field can take
- For a writable field, the values the field can be set to

Example Field Function Description

This section provides an example of a field function table, followed by a description of each part of the table.

CLK_IN_FREQ_SEL[1:0], IO Map, Address 0x04[2:1].

A control to set the CLK_IN frequency used.

Function

CLK_IN_FREQ_SEL[1:0]	Description
00	27 MHz
01	28.63636 MHz
10	24.576 MHz
11	24.000 MHz

In this example

- The name of the field is CLK_IN_FREQ_SEL, and it is two bits long.
- Address 0x04 is the I²C location of the field in big endian format (MSB first, LSB last), followed by the [2:1] bit range.
- The address is followed by a detailed description of the field.
- The first column of the table lists values the field can take or can be set to. These values are in binary format if not preceded by 0x or in hexadecimal format if preceded by 0x.
- The second column describes the function of each field for each value the field can take or can be set to. Values are in binary format.

REFERENCES

CEA, CEA-861-D, A DTV Profile for Uncompressed High Speed Digital Interfaces, Revision D, July 18, 2006.

Digital Content Protection (DCP) LLC, High-Bandwidth Digital Content Protection System, Revision 1.4, July 8, 2009.

HDMI Licensing and LLC, High-Definition Multimedia Interface, Revision 1.4a, March 4, 2010.

ITU, ITU-R BT.656-4, Interfaces for Digital Component Video Signals in 525-Line and 625-Line Television Systems Operating at the 4:2:2 Level of Recommendation ITU-R BT.601, February 1998.

INTRODUCTION TO THE ADV7630

The ADV7630 is a high quality 1:2 HDMI® splitter with 4:1 input multiplexer. It incorporates a four-input HDMI receiver and dual-transmitter functions onto a single chip. The ADV7630 is an ideal front end for splitters, AVRs with a second zone function, and DTVs with a repeater function.

Featuring the Analog Devices Xpressview™ fast switching technology, the ADV7630 provides the ability to switch between any connected ports in less than one second with minimal software overhead.

The ADV7630 supports HDMI streams with a data rate from 250 Mbps to 2.25 Gbps. These data rates include all mandatory 3DTV formats as well as all HDTV formats up to 1080p60 12-bit Deep Color.

The HDMI front end of the ADV7630 decodes simultaneously up to two digital streams out of the four TMDS streams it can receive. The two transmitter cores of the ADV7630 can re-encode digital streams from the front-end section into TMDS streams, which are sent to downstream devices. The ADV7630 supports the reception of HDMI streams that are HDCP encrypted. The ADV7630 front end also supports programmable equalization that ensures robust operation of the interface at cable lengths of up to 30 meters. The ADV7630 can optionally encrypt the HDMI streams it outputs according to the HDCP Specification 1.4.

Fabricated in an advanced CMOS process, the ADV7630 is provided in a 14 mm × 14 mm, 128-lead, surface-mount TQFP_EP, RoHS-compliant package that is specified over the 0°C to +70°C temperature range.

HDMI RECEIVER

The HDMI receiver section of the ADV7630 incorporates the Xpressview fast switching feature that allows any inactive input ports to be authenticated for instantaneous source switching between HDMI ports.

The ADV7630 features active equalizer for the input HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. The equalizer is programmable and is capable of equalizing for cable lengths of up to 30 meters to achieve robust receiver performance at even high HDMI data rates.

The ADV7630 features an Extended EDID (E-EDID) replicator and internal E-EDID RAM that reduce BOM requirements for external E-EDID EEPROMs. The ADV7630 incorporates an internal regulator, which allows the E-EDID functionality of the front end to be powered from the HDMI cable when ac power is removed from the system.

HDMI TRANSMITTER

The ADV7630 features two transmitters capable of outputting HDMI at a TMDS clock frequency of up to 225 MHz. Transmitters are also capable of reading back EDID content when HDMI sinks are attached.

MAIN FEATURES OF THE ADV7630

HDMI Receiver

- 3D HDMI 1.4a video format support
- Full colorimetry including sYCC601, Adobe RGB, Adobe YCC601, xvYCC extended gamut color
- CEC 1.4-compatible
- HDCP 1.4 support
- 3D video support, including Frame packing for all 3D formats up to a 225 MHz TMDS clock
- Xpressview fast switching between HDMI ports
- Supports Deep Color up to 48 bits per pixel
- Supports the reception of any audio data conforming to the HDMI specification, such as L-PCM at up to 192 kHz, compressed audio (IEC 61937), DSD, DST, DTS, and HBR
- +5 V detect and hot plug assert for all HDMI ports
- Features internal E-EDID functions

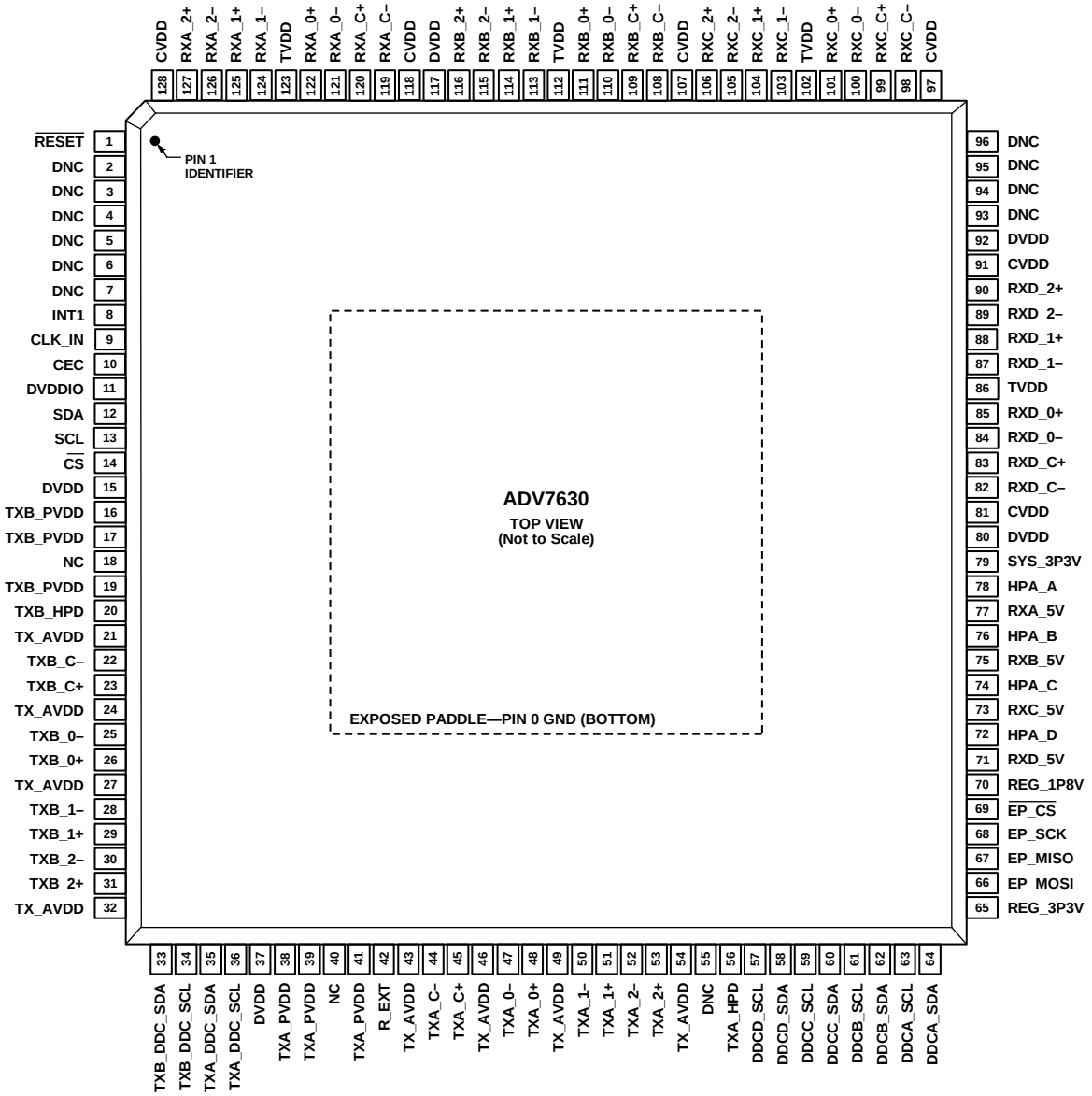
HDMI Transmitter

- 3D HDMI 1.4a video format support
- Full colorimetry including sYCC601, Adobe RGB, Adobe YCC601, xvYCC extended gamut color
- CEC 1.4 compatible
- HDCP v1.4a compliant transmitter
- Operates for TMDS clock frequencies up to 225 MHz
- EDID data extraction on both HDMI transmitters

Chip-Wide Features

- Internal CEC controller
- HDCP repeater support up to 127 KSVs
- Maskable interrupts on interrupt request output pin
- Temperature range: 0°C to +70°C
- Surface-mount, 128-lead, 14 mm × 14 mm TQFP_EP, RoHS-compliant package

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. EXPOSED PAD SHOULD BE CONNECTED TO GND.
3. DNC = DO NOT CONNECT TO THIS PIN.

10638-008

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	GND	Ground	Ground on Exposed Paddle. Exposed paddle should be connected to GND.
1	RESET	Miscellaneous digital	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7630 circuitry.
2 to 7, 55, 93 to 96	DNC	Do not connect	Do not connect to this pin.
8	INT1	Miscellaneous digital	Interrupt Output Pin.
9	CLK_IN	Digital input	Input Pin for a 3.3 V, 27.000 MHz Clock Oscillator. The following frequencies are also supported: 24 MHz, 24.576 MHz, and 28.63636 MHz. Refer to the CLK_IN_FREQ_SEL[1:0] register for more information.
10	CEC	Digital input/output	Consumer Electronic Control Channel (5 V Tolerant).
11	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
12	SDA	Digital input/output	I²C Port Serial Data Input/Output Pin. SDA is the data line for the control port.

Pin No.	Mnemonic	Type	Description
13	$\overline{\text{SCL}}$	Digital input	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
14	$\overline{\text{CS}}$	Digital input	Chip Select Pin. Pulling up this pin causes the I^2C state machine to ignore I^2C transmission. This pin has internal pull-down.
15	DVDD	Power	Digital Core Supply Voltage (1.8 V).
16	TXB_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separate from TXA_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
17	TXB_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separate from TXA_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package..
18, 40	NC	Not connected	Pins labeled as NC can be allowed to float, but it is better to connect these pins to ground. Avoid routing high speed signals through these pins because noise coupling may result.
19	TXB_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separate from TXA_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
20	TXB_HPD	Digital input	Hot Plug Detect Signal of HDMI Output Port B. This pin indicates to the interface whether the receiver is connected. It supports 1.8 V to 5 V CMOS logic levels.
21	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
22	TXB_C−	HDMI output	TMDS Clock Output; Complement of HDMI Output Port B.
23	TXB_C+	HDMI output	TMDS Clock Output; True of HDMI Output Port B.
24	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
25	TXB_0−	HDMI output	TMDS Output Channel 0 Complement of HDMI Output Port B. This pin can alternatively output TXB_2+ (refer to the TMDS Lines Swapping section).
26	TXB_0+	HDMI output	TMDS Output Channel 0 True of HDMI Output Port B. This pin can alternatively output TXB_2− (refer to the TMDS Lines Swapping section).
27	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
28	TXB_1−	HDMI output	TMDS Output Channel 1 Complement of HDMI Output Port B. This pin can alternatively output TXB_1+ (refer to the TMDS Lines Swapping section).
29	TXB_1+	HDMI output	TMDS Output Channel 1 True of HDMI Output Port B. This pin can alternatively output TXB_1− (refer to the TMDS Lines Swapping section).
30	TXB_2−	HDMI output	TMDS Output Channel 2 Complement of HDMI Output Port B. This pin can alternatively output TXB_0+ (refer to the TMDS Lines Swapping section).
31	TXB_2+	HDMI output	TMDS Output Channel 2 True of HDMI Output Port B. This pin can alternatively output TXB_0− (refer to the TMDS Lines Swapping section).
32	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
33	TXB_DDC_SDA	Digital input/output	HDCP Master Serial Data of HDMI Output Port B. TXB_DDC_SDA is an open-drain input/output that is 3.3 V and 5 V tolerant.
34	TXB_DDC_SCL	Digital output	HDCP Master Serial Clock of HDMI Output Port B. TXB_DDC_SCL is an open-drain output that is 3.3 V and 5 V tolerant.
35	TXA_DDC_SDA	Digital input/output	HDCP Master Serial Data of HDMI Output Port A. TXA_DDC_SDA is an open-drain input/output that is 3.3 V and 5 V tolerant.
36	TXA_DDC_SCL	Digital output	HDCP Master Serial Clock of HDMI Output Port A. TXA_DDC_SCL is an open-drain output that is 3.3 V and 5 V tolerant.
37	DVDD	Power	Digital Core Supply Voltage (1.8 V).
38	TXA_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separate from TXB_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
39	TXA_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separate from TXB_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.

Pin No.	Mnemonic	Type	Description
41	TXA_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separate from TXB_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
42	R_EXT	Input	Sets internal reference currents. Place 470 Ω resistor (1% tolerance) between this pin and ground.
43	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
44	TXA_C−	HDMI output	TMDS Clock Output; Complement of HDMI Output Port A.
45	TXA_C+	HDMI output	TMDS Clock Output; True of HDMI Output Port A.
46	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
47	TXA_0−	HDMI output	TMDS Output Channel 0 Complement of HDMI Output Port A. This pin can alternatively output TXA_2+ (refer to the TMDS Lines Swapping section).
48	TXA_0+	HDMI output	TMDS Output Channel 0 True of HDMI Output Port A. This pin can alternatively output TXA_2− (refer to the TMDS Lines Swapping section).
49	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
50	TXA_1−	HDMI output	TMDS Output Channel 1 Complement of HDMI Output Port A. This pin can alternatively output TXA_1+ (refer to the TMDS Lines Swapping section).
51	TXA_1+	HDMI output	TMDS Output Channel 1 True of HDMI Output Port A. This pin can alternatively output TXA_1− (refer to the TMDS Lines Swapping section).
52	TXA_2−	HDMI output	TMDS Output Channel 2 Complement of HDMI Output Port A. This pin can alternatively output TXA_0+ (refer to the TMDS Lines Swapping section).
53	TXA_2+	HDMI output	TMDS Output Channel 2 True of HDMI Output Port A. This pin can alternatively output TXA_0− (refer to the TMDS Lines Swapping section).
54	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
56	TXA_HPD	Digital input	Hot Plug Detect Signal of HDMI Output Port A. This pin indicates to the interface whether the receiver is connected. It supports 1.8 V to 5 V CMOS logic levels.
57	DDCD_SCL	Digital input	HDCP Slave Serial Clock Port D. This pin is a 3.3 V input that is 5 V tolerant.
58	DDCD_SDA	Digital input/output	HDCP Slave Serial Data Port D. This pin is a 5 V-tolerant 3.3 V input and open-drain output.
59	DDCC_SCL	Digital input	HDCP Slave Serial Clock Port C. This pin is a 3.3 V input that is 5 V tolerant.
60	DDCC_SDA	Digital input/output	HDCP Slave Serial Data Port C. This pin is a 5V-tolerant 3.3 V input and open-drain output.
61	DDCB_SCL	Digital input	HDCP Slave Serial Clock Port B. This pin is a 3.3 V input that is 5 V tolerant.
62	DDCB_SDA	Digital input/output	HDCP Slave Serial Data Port B. This pin is a 5V-tolerant 3.3 V input and open-drain output.
63	DDCA_SCL	Digital input	HDCP Slave Serial Clock Port A. This pin is a 3.3 V input that is 5 V tolerant.
64	DDCA_SDA	Digital input/output	HDCP Slave Serial Data Port A. This pin is a 5 V tolerant 3.3 V input and open-drain output.
65	REG_3P3V	Power output	Output of Internal 3.3 V LDO. Must be connected to ground via decoupling capacitors (10 nF in parallel with 100 nF capacitor). This pin can be used to power up external EDID SPI EEPROM when part is in power-down mode and 5 V is connected to part from HDMI cable.
66	EP_MOSI	Digital output	SPI Master Output/Slave Input for External EDID Interface.
67	EP_MISO	Digital input	SPI Master Input/Slave Output for External EDID Interface.
68	EP_SCK	Digital output	SPI Clock for External EDID Interface.
69	$\overline{\text{EP\_CS}}$	Digital output	SPI Chip Select for External EDID Interface.
70	REG_1P8V	Power output	Output of Internal 1.8 V LDO. This pin must be connected only to decoupling capacitors (100 nF in parallel with 10 nF).
71	RXD_5V	HDMI input	5 V Detect Pin for Port D in the HDMI Interface. This pin is used to power EDID replicator.
72	HPA_D	HDMI output	Hot Plug Assert Signal Output for HDMI Port D.
73	RXC_5V	HDMI input	5 V Detect Pin for Port C in the HDMI Interface. This pin is used to power the EDID replicator.
74	HPA_C	HDMI output	Hot Plug Assert Signal Output for HDMI Port C.
75	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface. This pin is used to power the EDID replicator.
76	HPA_B	HDMI output	Hot Plug Assert Signal Output for HDMI Port B.
77	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface. This pin is used to power the EDID replicator.
78	HPA_A	HDMI output	Hot Plug Assert Signal Output for HDMI Port A.
79	SYS_3P3V	Miscellaneous power	3.3 V Power Supply.
80	DVDD	Power	Digital Core Supply Voltage (1.8 V).
81	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
82	RXD_C−	HDMI input	Digital Input Clock Complement of Port D in the HDMI Interface.
83	RXD_C+	HDMI input	Digital Input Clock True of Port D in the HDMI Interface.

Pin No.	Mnemonic	Type	Description
84	RXD_0−	HDMI input	Digital Input Channel 0 Complement of Port D in the HDMI Interface.
85	RXD_0+	HDMI input	Digital Input Channel 0 True of Port D in the HDMI Interface.
86	TVDD	Power	Terminator Supply Voltage (3.3 V).
87	RXD_1−	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
88	RXD_1+	HDMI input	Digital Input Channel 1 True of Port D in the HDMI Interface.
89	RXD_2−	HDMI input	Digital Input Channel 2 Complement of Port D in the HDMI Interface.
90	RXD_2+	HDMI input	Digital Input Channel 2 True of Port D in the HDMI Interface.
91	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
92	DVDD	Power	Digital Core Supply Voltage (1.8 V).
97	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
98	RXC_C−	HDMI input	Digital Input Clock Complement of Port C in the HDMI Interface.
99	RXC_C+	HDMI input	Digital Input Clock True of Port C in the HDMI Interface.
100	RXC_0−	HDMI input	Digital Input Channel 0 Complement of Port C in the HDMI Interface.
101	RXC_0+	HDMI input	Digital Input Channel 0 True of Port C in the HDMI Interface.
102	TVDD	Power	Terminator Supply Voltage (3.3 V).
103	RXC_1−	HDMI input	Digital Input Channel 1 Complement of Port C in the HDMI Interface.
104	RXC_1+	HDMI input	Digital Input Channel 1 True of Port C in the HDMI Interface.
105	RXC_2−	HDMI input	Digital Input Channel 2 Complement of Port C in the HDMI Interface.
106	RXC_2+	HDMI input	Digital Input Channel 2 True of Port C in the HDMI Interface.
107	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
108	RXB_C−	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
109	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
110	RXB_0−	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
111	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
112	TVDD	Power	Terminator Supply Voltage (3.3 V).
113	RXB_1−	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
114	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
115	RXB_2−	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
116	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
117	DVDD	Power	Digital Core Supply Voltage (1.8 V).
118	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
119	RXA_C−	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
120	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
121	RXA_0−	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
122	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
123	TVDD	Power	Terminator Supply Voltage (3.3 V).
124	RXA_1−	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
125	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
126	RXA_2−	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
127	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
128	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).

TMDS LINES SWAPPING

The ADV7630 allows for easy IC-to-IC connection. It implements a pin-swapping option on the output TMDS TX lines, which allows for easier routing. TMDS pin swapping is available for the TXA TMDS and TXB TMDS pins. In the TXA main map, swapping for the TXA TMDS pins is done using TX_CHANNEL_SWAP. In the TXB main map, swapping for the TXB TMDS pins is also accomplished using TX_CHANNEL_SWAP.

An example TMDS interconnection is shown in Figure 3.

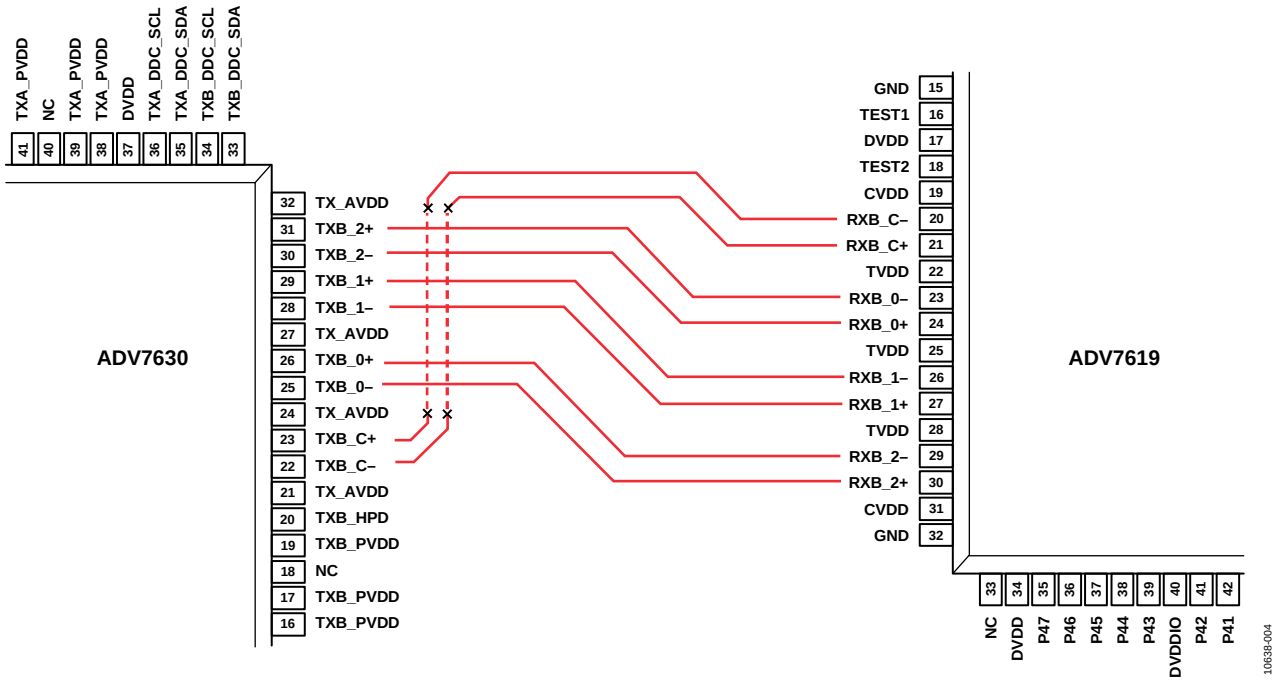


Figure 3. Example TMDS Line Swapping Between the ADV7630 and ADV7619

Table 5. TMDS Channel Swapping (TXA Main Map)

TX_CHANNEL_SWAP = 0	TX_CHANNEL_SWAP = 1
TXA_2+	TXA_0–
TXA_2–	TXA_0+
TXA_1+	TXA_1–
TXA_1–	TXA_1+
TXA_0+	TXA_2–
TXA_0–	TXA_2+
TXA_C+	TXA_C+ (not swapped internally)
TXA_C–	TXA_C– (not swapped internally)

Table 6. TMDS Channel Swapping (TXB Main Map)

TX_CHANNEL_SWAP = 0	TX_CHANNEL_SWAP = 1
TXB_2+	TXB_0–
TXB_2–	TXB_0+
TXB_1+	TXB_1–
TXB_1–	TXB_1+
TXB_0+	TXB_2–
TXB_0–	TXB_2+
TXB_C+	TXB_C+ (not swapped internally)
TXB_C–	TXB_C– (not swapped internally)

TXA_C+ and TXA_C– are not swapped internally by asserting TX_CHANNEL_SWAP in the TXA main map. Similarly, TXB_C+ and TXB_C– are not swapped internally by asserting TX_CHANNEL_SWAP in the TXB main map. TMDS clock lines (C+ and C–) are insensitive to polarity inversion. Therefore, Figure 3 is correct with connection TXB_C+ to RXB_C– and TXB_C– to RXB_C+.

TX_CHANNEL_SWAP, TXA Main Map, Address 0xFE[0]

A control to swap TXA TMDS pins.

Function

TX_CHANNEL_SWAP	Description
0 (default)	TMDS TXA pins not swapped
1	TMDS TXA pins swapped

TX_CHANNEL_SWAP, TXB Main Map, Address 0xFE[0]

A control to swap TXB TMDS pins.

Function

TX_CHANNEL_SWAP	Description
0 (default)	TMDS TXB pins not swapped
1	TMDS TXB pins swapped

GLOBAL CONTROL REGISTERS

The register control bits described in this section deal with the general control of the ADV7630 receiver and transmitter sections.

ADV7630 REVISION IDENTIFICATION

RD_INFO[15:0], IO, Address 0xEA[7:0]; Address 0xEB[7:0] (Read Only)

Chip revision code.

Function

RD_INFO[15:0]	Description
0x4041	ADV7630

POWER-DOWN CONTROLS

Primary Power-Down Controls

The ADV7630 features the following four controls to set the power mode in which the part operates:

- POWER_DOWN affects the power mode of the HDMI receiver section as well as the input clock pads. Note that the input clock is used by the interrupt controller.
- CEC_POWER_UP affects the power mode of the CEC section.
- The SYSTEM_PD control associated with TXA affects the power mode of the HDMI TXA transmitter section.
- The SYSTEM_PD control associated with TXB (refer to the HDMI Transmitter section) affects the power mode of the HDMI TXB transmitter section.

The descriptions of the power-down control bits are provided here. The Power-Down Modes section explains how to use these controls.

POWER_DOWN, IO, Address 0x0C[5]

A control to enable power-down mode. This is the main I^2C power-down control.

Function

POWER_DOWN	Description
0	Chip operational
1 (Default)	Enables chip power-down

CEC_POWER_UP, CEC, Address 0x2A[0]

Power mode of CEC module.

Function

CEC_POWER_UP	Description
0 (Default)	Powers down the CEC module
1	Powers up the CEC module

The powering down of TX sections is also possible with the following SYSTEM_PD registers that are located in the TXA and TXB maps.

SYSTEM_PD, TXA Main Map, Address 0x41[6]

Power mode of TXA.

Function

SYSTEM_PD	Description
0	Powers down the TXA section
1 (Default)	Powers up the TXA section

SYSTEM_PD, TXB Main Map, Address 0x41[6]

Power mode of TXB.

Function

SYSTEM_PD	Description
0	Powers down the TXB section
1 (Default)	Powers up the TXB section

Secondary Power-Down Controls

The following controls allow various sections of the ADV7630 to be powered down.

CLK_IN_PDN allows the user to power down the clock input through the CLK_IN pin.

- HDMI section
- DDC pads (active pull-up depends on XTAL)
- Reset

The input clock is also provided to the HDCP engine and the repeater controller within the HDMI receiver. Powering down CLK_IN with CLK_IN_PDN affects the HDCP engine.

CLK_IN_PDN, IO Map, Address 0x0B[0]

A power-down control for the CLK_IN in the digital blocks.

Function

CLK_IN_PDN	Description
0 (Default)	Powers up CLK_IN buffer to digital core
1	Powers down CLK_IN buffer to digital core

CORE_PDN, IO Map, Address 0x0B[1]

A power-down control for digital sections of the HDMI core.

Function

CORE_PDN	Description
0 (Default)	Powers up digital sections of HDMI block
1	Powers down digital section of HDMI block

POWER-DOWN MODES

The ADV7630 supports the independent power modes for the HDMI receiver and transmitter sections. This section describes the following power modes:

HDMI receiver power modes:

- Rx power-down mode
- Rx normal power mode

HDMI transmitter power modes:

- TXA and TXB power-down mode
- TXA and TXB normal power mode

The receiver and transmitter power modes are fully independent. When the ADV7630 is powered up, it runs in a power mode that is the combination of a receiver power mode and a transmitter power mode.

HDMI Receiver Power Modes

Rx Power-Down Mode

In power-down mode, selected sections and pads are kept active to provide E-EDID and +5 V antiglitch filter functionality. In power-down mode, all the sections of the ADV7630 are disabled except for the following blocks:

- I^2C slave section.
- Rx E-EDID/repeater controller
- Rx E-EDID/ring oscillator
  The receiver E-EDID ring oscillator provides a clock to the Rx E-EDID/repeater controller (refer to the E-EDID/Repeater Controller section) and the antiglitch filter for +5 V cable detection (refer to the +5 V Cable Detect section). The clock output from the ring oscillator runs at approximately 50 MHz.
- +5 V cable detection
- Hot plug assertion (HPA) function
- HDMI transmitter section (refer to the HDMI Transmitter section).

The following pads are the only HDMI receiver and general pads that are enabled in Rx power-down mode:

- Reset and I²C pads:
  - $\overline{\text{RESET}}$
  - $\overline{\text{CS}}$
  - SDA
  - SCL
- DDC pads:
  - DDCA_SCL
  - DDCA_SDA
  - DDCB_SCL
  - DDCB_SDA
  - DDCC_SCL
  - DDCC_SDA
  - DDCD_SCL
  - DDCD_SDA
- +5 V detection and HPA pads:
  - RXA_5V
  - RXB_5V
  - RXC_5V
  - RXD_5V
  - HPA_A
  - HPA_B
  - HPA_C
  - HPA_D
- SPI EEPROM interface pads:
  - EP_MOSI
  - EP_MISO
  - $\overline{\text{EP\_CS}}$
  - EP_SCK

Entering Power-Down Mode

When the part enters Rx power-down mode, the POWER_DOWN bit is set to 1.

EDID Available in Rx Power-Off Mode

The ADV7630 fully supports E-EDID read functionality in a powered-off configuration. The 5 V power signals from the HDMI source(s) connected to the ADV7630 can be used to power the E-EDID controller on the ADV7630. On-chip regulators provide a 3.3 V signal to power the SPI EEPROM.

The configuration in Figure 4 can be used to provide E-EDID functionality when in a powered-off state.

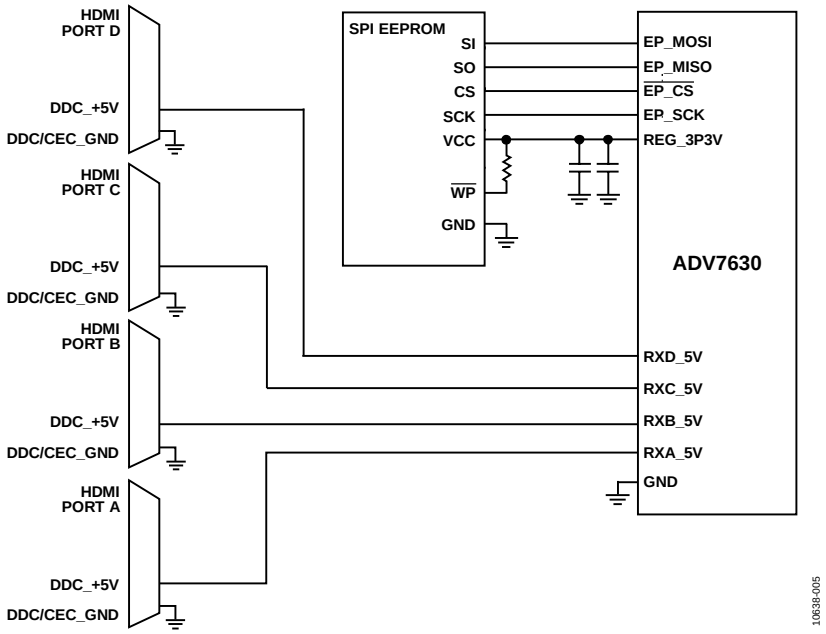


Figure 4. Required Hardware Configuration for E-EDID Support in Powered-Off State

EDID_PWRSW3P3, HDMI Map, Address 0x71[3:2]

Controls the switch related to the EDID power domain taking the system supply or the cable supply. Dedicated control for the 3.3 V domain.

Function

EDID_PWRSW3P3	Description
00	Power switch always takes the cable supply
01	Power switch takes the system supply whenever it is available; otherwise, takes the cable supply
10	Power switch takes the cable supply whenever it is available; otherwise, takes the system supply
11	Power switch takes the cable supply whenever it is available; otherwise, takes the system supply

EDID_PWRSW1P8, HDMI Map, Address 0x71[1:0]

Controls the switch related to EDID power domain taking the system or the cable supply. Dedicated control for the 1.8 V domain.

Function

EDID_PWRSW1P8	Description
00	Power switch always takes the cable supply
01	Power switch takes the system supply whenever it is available; otherwise, takes the cable supply
10	Power switch takes the cable supply whenever it is available; otherwise, takes the system supply
11	Power switch takes the cable supply whenever it is available; otherwise, takes the system supply

HDMI Transmitter Power Modes

The ADV7630 has two HDMI transmitters, TXA and TXB, that are controlled independently of each other. The following sections describe how to set the power mode of the TXA transmitter section. Unless stated otherwise, the TXB transmitter features the same power-down mode as the TXA transmitter. For simplicity's sake, the following sections do not describe the power-down modes of the TXB transmitter, but list the controls that are required to set the power mode of the TXB transmitter.

TXA Power-Down Mode

Sections Powered Up

In TXA power-down mode, selected sections and pads related to the TXA transmitter are kept active to monitor the presence of an active sink. All the TXA transmitter sections of the ADV7630 are disabled except for the following sections:

- TXA Hot Plug detect (HPD) circuitry
- TXA Rx sense circuitry
- Non TXA and TXB transmitter sections (for example, receiver section)

The following pads are the only TXA transmitter pads that are enabled in TXA power-down mode:

- HPD pad, TXA_HPD−
- TMDS clock output pad, TXA_C−
- Complementary TMDS clock output pad, TXA_C+

Entering TXA Power-Down Mode

The ADV7630 enters TXA power-down mode when SYSTEM_PD is set to 1.

Some registers are reset when the TXA section is put into the TXA power-down mode. Table 7 provides a list of TXA registers that are reset, as well as the registers that are not reset and, therefore, retain their values.

Table 7. TXA Registers Reset Strategy

TXA Registers	TXA_SOFT_RESET Set High or RESET Pin Set Low	TXA_HPD Pin Set Low	SYSTEM_PD[1] Set High
TXA Main Map 0x00 to 0x93	Reset	Reset	Not reset
TXA Main Map 0x94 to 0x97 (except 0x96[7:6])	Reset	Reset	Reset
TXA Main Map 0x96[7:6]	Reset	Not reset	Not reset
TXA Main Map 0x98 to 0xAE	Reset	Not reset	Not reset
TXA Main Map 0xAF to 0xCC	Not reset	Reset	Reset
TXA Main Map 0xCD to 0xFF	Not reset	Not reset	Not reset
TXA Packet Memory Map 0x00 to 0xFF	Reset	Not reset	Reset

[1] SYSTEM_PD bit in TXA main map.

Table 8. TXB Registers Reset Strategy

TXB Registers	TXB_SOFT_RESET Set High or RESET Pin Set Low	TXB_HPD Pin Set Low	SYSTEM_PD[1] Set High
TXB Main Map 0x00 to 0x93	Reset	Reset	Not reset
TXB Main Map 0x94 to 0x97 (except 0x96[7:6])	Reset	Reset	Reset
TXB Main Map 0x96[7:6]	Reset	Not reset	Not reset
TXB Main Map 0x98 to 0xAE	Reset	Not reset	Not reset
TXB Main Map 0xAF to 0xCC	Not reset	Reset	Reset
TXB Main Map 0xCD to 0xFF	Not reset	Not reset	Not reset
TXB Packet Memory Map 0x00 to 0xFF	Reset	Not reset	Reset

[1] SYSTEM_PD bit in TXB main map.

Further Power Savings in TXA Power-Down Mode

A number of extra options can be taken in TXA power-down mode to reduce further the current consumption of the ADV7630. These options include disabling the Rx sense monitoring and TXA transmitter interrupt sections by setting RX_SENSE_PD to 0. When this bit is set to 0, the TXA interrupts cannot be used and the MSEN_STATE status is not valid. However, the HPD_STATE status is still valid when RX_SENSE_PD is set to 0.

RESET CONTROLS

$\overline{\text{RESET}}$ Pin

The ADV7630 can be reset by a low pulse on the $\overline{\text{RESET}}$ pin for a minimum of 5 ms. It is recommended to wait 5 ms after the low pulse before an I²C write is performed to the ADV7630.

Resetting the ADV7630 via the $\overline{\text{RESET}}$ pin resets all sections of the ADV7630; that is, the receiver section as well as both the TXA and TXB transmitter sections. Table 7 and Table 8 provide lists of transmitter registers that are reset via the $\overline{\text{RESET}}$ pin.

Reset Controls

The receiver and CEC sections can be reset via the MAIN_RESET bit. The transmitter sections TXA and TXB can be reset via the TXA_SOFT_RESET and TXB_SOFT_RESET bits, respectively. Table 7 and Table 8 provide lists of transmitter registers that are reset via the $\overline{\text{RESET}}$ pin.

MAIN_RESET, IO Map, Address 0xFF[7] (Self-Clearing)

Main reset where all I²C registers are reset to their default values.

Function

MAIN_RESET	Description
0 (default)	Normal operation
1	Apply main I²C reset

TXA_SOFT_RESET, IO Map, Address 0x1B[7] (Self-Clearing)

Software reset for HDMI TXA.

Function

TXA_SOFT_RESET	Description
0 (default)	Normal operation
1	Apply reset

TXB_SOFT_RESET, IO Map, Address 0x1B[6] (Self-Clearing)

Software reset for HDMI TXB.

Function

TXB_SOFT_RESET	Description
0 (default)	Normal operation
1	Apply reset

DRIVE STRENGTH SELECTION

It may be desirable to strengthen or weaken the drive strength of the output drivers for Electromagnetic Compatibility (EMC) and crosstalk reasons. DR_STR[1:0] controls the adjustment of the output drivers' main I²C interface of the ADV7630. The drive strength DR_STR[1:0] bits affect output drivers for the following output pins:

- SDA
- SCL

DR_STR[1:0], IO Map, Address 0x14[5:4]

A control to set the drive strength of the data output drivers.

Function

DR_STR[1:0]	Description
00	Reserved
01	Medium low (2×)
10 (default)	Medium high (3×)
11	High (4×)

CLOCK INPUT FREQUENCY OPERATION

The ADV7630 can operate on four different clock input frequencies: 24.000 MHz, 24.576 MHz, 27.000 MHz, and 28.63636 MHz.

CLK_IN_FREQ_SEL[1:0], IO Map, Address 0x04[2:1]

A control to set the CLK_IN frequency to be used.

Function

CLK_IN_FREQ_SEL[1:0]	Description
00 (default)	27 MHz
01	28.63636 MHz
10	24.576 MHz
11	24.000 MHz

HDMI RECEIVER

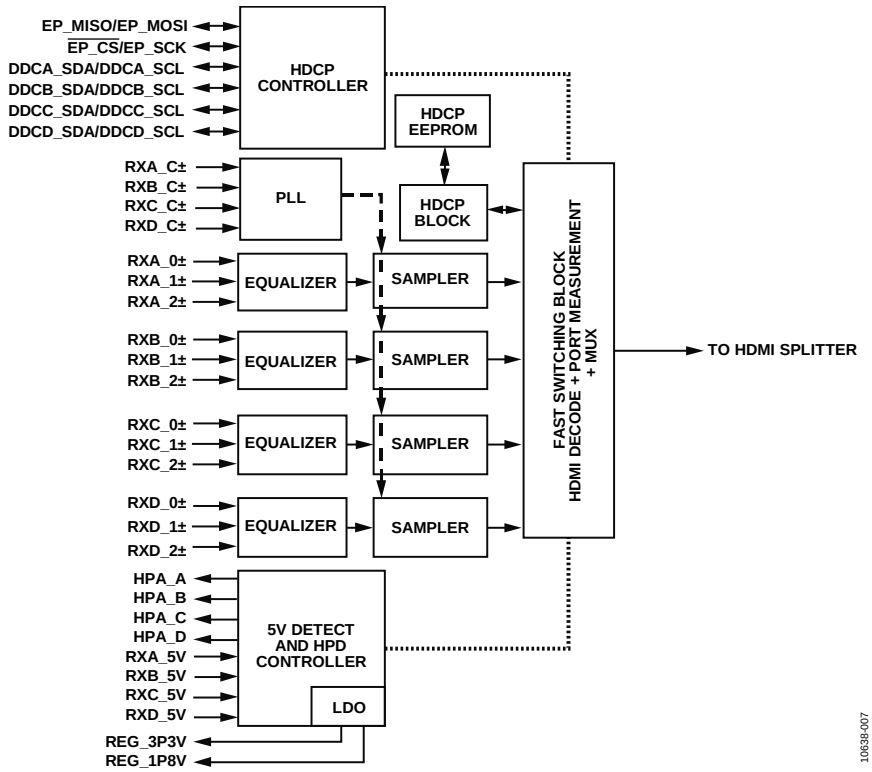


Figure 5. Functional Block Diagram of HDMI Receiver

+5 V CABLE DETECT

The HDMI receiver in the ADV7630 can monitor the level on the +5 V power signal pin of each connected HDMI port. The results of this detection can be read back from the following I²C registers. These readbacks are valid even when the part is not configured for HDMI mode.

CABLE_DET_A_RAW, IO Map, Address 0x6F[3] (Read Only)

Raw status of Port A +5 V cable detection signal.

Function

CABLE_DET_A_RAW	Description
0	No cable detected on Port A
1	Cable detected on Port A (high level on RXA_5V)

CABLE_DET_B_RAW, IO Map, Address 0x6F[2] (Read Only)

Raw status of Port B +5 V cable detection signal.

Function

CABLE_DET_B_RAW	Description
0	No cable detected on Port B
1	Cable detected on Port B (high level on RXB_5V)

CABLE_DET_C_RAW, IO Map, Address 0x6F[1] (Read Only)

Raw status of Port C +5 V cable detection signal.

Function

CABLE_DET_C_RAW	Description
0	No cable detected on Port C
1	Cable detected on Port C (high level on RXC_5V)

CABLE_DET_D_RAW, IO Map, Address 0x6F[0] (Read Only)

Raw status of Port D +5 V cable detection signal.

Function

CABLE_DET_D_RAW	Description
0	No cable detected on Port D
1	Cable detected on Port D (high level on RXD_5V)

The ADV7630 provides a digital glitch filter on the +5 V power signals from the HDMI ports. The output of this filter is used to reset the HDMI block (refer to the HDMI Section Reset Strategy section).

The +5 V power signal must be constantly high for the duration of the timer (controlled by FILT_5V_DET_TIMER); otherwise, the output of the filter is low. The output of the filter returns low as soon as any change in the +5 V power signal is detected.

FILT_5V_DET_DIS, HDMI, Address 0x56[7]

This bit is a control to disable the digital glitch filter on the HDMI 5 V detect signals. The filtered signals are used as interrupt flags and are also used to reset the HDMI section. The filter works from an internal ring oscillator clock and is, therefore, available in power-down mode. The clock frequency of the ring oscillator is 42 MHz ± 10%.

Note: If the 5 V pins are not used and are left unconnected, the 5 V detect circuitry should be disconnected from the HDMI reset signal by setting DIS_CABLE_DET_RST to 1. This avoids holding the HDMI section in reset.

Function

FILT_5V_DET_DIS	Description
0 (default)	Enable
1	Disable

Note: If the 5 V detect pins are not used and are left unconnected, the 5 V detect circuitry should be disconnected from the HDMI reset signal by setting DIS_CABLE_DET_RST to 1. This avoids holding the HDMI section in reset.

FILT_5V_DET_TIMER[6:0], HDMI, Address 0x56[6:0]

This control is used to set the timer for the digital glitch filter on the HDMI 5 V detect inputs. The unit of this parameter is two clock cycles of the ring oscillator (~47 ns). The input must be constantly high for the duration of the timer, otherwise the filter output remains low. The output of the filter returns low as soon as any change in the +5 V power signal is detected.

Function

FILT_5V_DET_TIMER[6:0]	Description
1011000 (default)	Approximately 4.2 µs
xxxxxxx	Time duration of +5 V deglitch filter. The unit of this parameter is two clock cycles of the ring oscillator (~47 ns)

DIS_CABLE_DET_RST, HDMI, Address 0x48[6]

This control disables the reset effects of cable detection. DIS_CABLE_DET_RST should be set to 1 if the 5 V detect pins are unused and left unconnected.

Function

DIS_CABLE_DET_RST	Description
0 (default)	Reset the HDMI section if the 5 V input pin corresponding to the selected HDMI port (for example, RXA_5V for Port A) is inactive
1	Do not use the 5 V input pins as reset signals for the HDMI section

HOT PLUG ASSERT

The ADV7630 features HPA controls for its four HDMI ports. The purpose of these controls and their corresponding output pins is to communicate to an HDMI transmitter that the E-EDID connected to the DDC bus can be accessed.

Note: To comply with the required output characteristics described in Section 4.2.9 "Hot Plug Detect Signal" of the HDMI 1.4a specification, the output resistance on the HPA pins must be 1000 Ω ± 20%. This can be implemented by connecting the HPA line to the Hot Plug Detect line of the HDMI connector through a 680R ± 5% Ω resistor (refer to Figure 6).

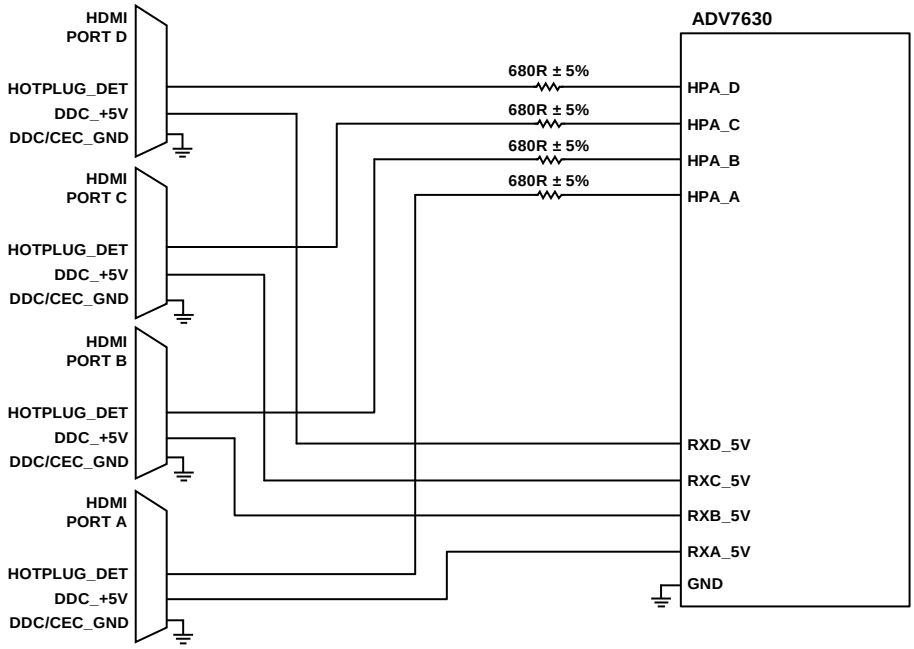


Figure 6. Hot Plug Detect Connection

HPA_MANUAL, HDMI, Address 0x6C[0]

Manual control enable for the HPA output pins. By setting this bit, any automatic control of these pins is disabled. Manual control is determined by HPA_MAN_VALUE_X (where X = A, B, C, or D).

Function

HPA_MANUAL	Description
0	HPA takes its value based on HPA_AUTO_INT_EDID
1 (default)	HPA takes its value from HPA_MAN_VALUE_X

HPA_MAN_VALUE_A, IO Map, Address 0x20[7]

A manual control for the value of HPA on Port A. Only valid if HPA_MANUAL is set to 1.

Function

HPA_MAN_VALUE_A	Description
0 (default)	0 V applied to HPA_A pin
1	High level applied to HPA_A pin

HPA_MAN_VALUE_B, IO Map, Address 0x20[6]

A manual control for the value of HPA on Port B. Only valid if HPA_MANUAL is set to 1.

Function

HPA_MAN_VALUE_B	Description
0 (default)	0 V applied to HPA_B pin
1	High level applied to HPA_B pin

HPA_MAN_VALUE_C, IO Map, Address 0x20[5]

A manual control for the value of HPA on Port C. Only valid if HPA_MANUAL is set to 1.

Function

HPA_MAN_VALUE_C	Description
0 (default)	0 V applied to HPA_C pin
1	High level applied to HPA_C pin

HPA_MAN_VALUE_D, IO Map, Address 0x20[4]

A manual control for the value of HPA on Port D. Only valid if HPA_MANUAL is set to 1.

Function

HPA_MAN_VALUE_D	Description
0 (default)	0 V applied to HPA_D pin
1	High level applied to HPA_D pin

HPA_AUTO_INT_EDID[1:0], HDMI, Address 0x6C[2:1]

Selects the type of automatic control on the HPA output pins. This bit has no effect when HPA_MANUAL is set to 1.

Function

HPA_AUTO_INT_EDID[1:0]	Description
00	The HPA of an HDMI port is asserted high immediately after the internal E-EDID has been activated for that port. The HPA of a specific HDMI port is deasserted low immediately after the internal E-EDID is deactivated for that port.
01 (default)	The HPA of an HDMI port is asserted high following a programmable delay after the part detects an HDMI cable plug on that port. The HPA of an HDMI port is immediately deasserted after the part detects a cable disconnect on that HDMI port.
10	The HPA of an HDMI port is asserted high after the following two conditions have been met: 1. The internal E-EDID is active for that port. 2. The delayed version of the cable detect signal for that port, CABLE_DET_X_RAW, is high. The HPA of an HDMI port is immediately deasserted after either of the following two conditions have been met: 1. The internal E-EDID is deactivated for that port. 2. The cable detect signal for that port, CABLE_DET_X_RAW, is low.
11	The HPA of an HDMI port is asserted high after the following three conditions have been met: 1. The internal E-EDID is active for that port. 2. The delayed version of the cable detect signal for that port, CABLE_DET_X_RAW, is high. 3. The user has set the manual HPA control for that port to 1 via the HPA_MAN_VALUE_X controls. The HPA of an HDMI port is immediately deasserted after any of the following three conditions have been met: 1.The internal E-EDID is deactivated for that port 2.The cable detect signal for that port, CABLE_DET_X_RAW, is low. 3.The user sets the manual HPD control for that port to 0 via the HPA_MAN_VALUE_X controls.

Note: The delay is programmable via HPA_DELAY_SEL[3:0]. Refer to EDID_X_ENABLED for details on enabling the internal E-EDID for an HDMI port. In HPA_MAN_VALUE_X and CABLE_DET_X_RAW, 'X' refers to A, B, C and D.

HPA_DELAY_SEL[3:0], HDMI, Address 0x6C[7:4]

Sets a delay between +5 V detection and HPA on the HPA output pins, in increments of 100 ms per bit.

Function

HPA_DELAY_SEL[3:0]	Description
0000	No delay
0001	100 ms delay
0010	200 ms delay
1010 (default)	1 sec delay
1111	1.5 sec delay

HPA_TRISTATE_A, IO Map, Address 0x20[3]

Tristate HPA output pin for Port A.

Function

HPA_TRISTATE_A	Description
0 (default)	HPA_A pin active
1	Tristate HPA_A pin

HPA_TRISTATE_B, IO Map, Address 0x20[2]

Tristate HPA output pin for Port B.

Function

HPA_TRISTATE_B	Description
0 (default)	HPA_B pin active
1	Tristate HPA_B pin

HPA_TRISTATE_C, IO Map, Address 0x20[1]

Tristate HPA output pin for Port C.

Function

HPA_TRISTATE_C	Description
0 (default)	HPA_C pin active
1	Tristate HPA_C pin

HPA_TRISTATE_D, IO Map, Address 0x20[0]

Tristate HPA output pin for Port D.

Function

HPA_TRISTATE_D	Description
0 (default)	HPA_D pin active.
1	Tristate HPA_D pin

HPA_STATUS_PORT_A, IO Map, Address 0x21[3] (Read Only)

Readback of HPA status for RX Port A.

Function

HPA_STATUS_PORT_A	Description
0	+5 V not applied to HPA_A pin by chip
1	+5 V applied to HPA_A pin by chip

HPA_STATUS_PORT_B, IO Map, Address 0x21[2] (Read Only)

Readback of HPA status for RX Port B.

Function

HPA_STATUS_PORT_B	Description
0	+5 V not applied to HPA_B pin by chip
1	+5 V applied to HPA_B pin by chip

HPA_STATUS_PORT_C, IO Map, Address 0x21[1] (Read Only)

Readback of HPA status for RX Port C.

Function

HPA_STATUS_PORT_C	Description
0	+5 V not applied to HPA_C pin by chip
1	+5 V applied to HPA_C pin by chip

HPA_STATUS_PORT_D, IO Map, Address 0x21[0] (Read Only)

Readback of HPA status for RX Port D.

Function

HPA_STATUS_PORT_D	Description
0	+5 V not applied to HPA_D pin by chip
1	+5 V applied to HPA_D pin by chip

HPA_OVR_TERM, HDMI, Address 0x6C[3]

A control to set termination control to be overridden by the HPA setting. When this bit is set, termination on a specific port will be set according to the HPA status of that port.

Function

HPA_OVR_TERM	Description
0 (default)	Automatic or manual I²C control of port termination
1	Termination controls disabled and overridden by HPA controls

E-EDID/REPEATER CONTROLLER

The HDMI section incorporates an E-EDID/repeater controller, which performs the following tasks:

- Computes the E-EDID checksums for the four ports
- Updates the SPA value after the E-EDID image is loaded from the SPI EEPROM into the internal E-EDID RAM
- Performs the repeater routines described in the Repeater Actions Required by External Controller section

The E-EDID/repeater controller is powered from the DVDD supply and clocked by an internal ring oscillator. The controller and the internal DDC bus arbiter are kept active when the part is in cable supply mode, that is, it is powered from the +5 V supply of one or more HDMI sources (refer to the EDID Available in Rx Power-Off Mode section), which allows the internal Enhanced-Extended Display Identification (E-EDID) to be functional and accessible through the DDC port even when the part is powered down. In the cable supply mode, all the power needed by the ADV7630 can be provided by one or more HDMI sources connected to the HDMI ports. These HDMI sources or transmitters can then read the capabilities of the powered-down application integrating the ADV7630 by accessing its internal E-EDID through the DDC ports.

The E-EDID/repeater controller is reset when the DVDD supplies go low or when HDCP_REPT_EDID_RESET is set to 1. When the E-EDID/repeater controller reboots, it performs the following tasks:

- Clears the internal E-EDID and KSV RAM (refer to the E-EDID/Repeater Controller section and the HDCP Registers Available in Repeater Map section)
- Computes a total of seven checksums for all four ports
- Updates the SPA registers (refer to the SPA Configuration section)

HDCP_REPT_EDID_RESET, HDMI, Address 0x5A[3] (Self-Clearing)

A reset control for the E-EDID/Repeater controller. When asserted it resets the E-EDID/Repeater controller.

Function

HDCP_REPT_EDID_RESET	Description
0 (default)	Normal operation
1	Resets the E-EDID/repeater controller

E-EDID DATA CONFIGURATION

The ADV7630 features an SRAM memory that can store an E-EDID. This internal E-EDID feature can be used for the four HDMI ports: A, B, C, and D. It is also possible to use an external device storage for the E-EDID data on each port, or a combination of internal E-EDID for some port(s) and external storage for the other port(s).

The following controls are provided to enable the internal E-EDID for each of the four HDMI ports.

MAN_EDID_A_ENABLE, Repeater Map, Address 0x74[0]

Manual enable for I²C access to internal E-EDID RAM from DDC Port A, when the operations LOAD_EDID and CKSUM_CALC are finished.

Function

MAN_EDID_A_ENABLE	Description
0 (default)	Manual enable not active for E-EDID on Port A
1	Manual enable active for E-EDID on Port A

MAN_EDID_B_ENABLE, Repeater Map, Address 0x74[1]

Manual enable for I²C access to internal E-EDID RAM from DDC Port B, when the operations LOAD_EDID and CKSUM_CALC are finished.

Function

MAN_EDID_B_ENABLE	Description
0 (default)	Manual enable not active for E-EDID on Port B
1	Manual enable active for E-EDID on Port B

MAN_EDID_C_ENABLE, Repeater Map, Address 0x74[2]

Manual enable for I²C access to internal E-EDID RAM from DDC Port C, when the operations LOAD_EDID and CKSUM_CALC are finished.

Function

MAN_EDID_C_ENABLE	Description
0 (default)	Manual enable not active for E-EDID on Port C
1	Manual enable active for E-EDID on Port C

MAN_EDID_D_ENABLE, Repeater Map, Address 0x74[3]

Manual enable for I²C access to internal E-EDID RAM from DDC Port D, when the operations LOAD_EDID and CKSUM_CALC are finished.

Function

MAN_EDID_D_ENABLE	Description
0 (default)	Manual enable not active for E-EDID on Port D
1	Manual enable active for E-EDID on Port D

When the internal E-EDID is enabled on any of the four ports (for example, Port A by setting MAN_EDID_A_ENABLE to 1), the ADV7630 must first calculate the E-EDID checksums for that port before the E-EDID is actually enabled.

The following read only flags can be utilized to determine if the E-EDID is actually enabled on any of the four HDMI ports.

EDID_A_ENABLED, Repeater Map, Address 0x76[0] (Read Only)

Resulting I²C enable readback for E-EDID access on Port A, after a combination of manual and automatic functions.

Function

EDID_A_ENABLED	Description
0	Disabled
1	Enabled

EDID_B_ENABLED, Repeater Map, Address 0x76[1] (Read Only)

Resulting I²C enable readback for E-EDID access on Port B, after a combination of manual and automatic functions.

Function

EDID_B_ENABLED	Description
0	Disabled
1	Enabled

EDID_C_ENABLED, Repeater Map, Address 0x76[2] (Read Only)

Resulting I²C enable readback for E-EDID access on Port C, after a combination of manual and automatic functions.

Function

EDID_C_ENABLED	Description
0	Disabled
1	Enabled

EDID_D_ENABLED, Repeater Map, Address 0x76[3] (Read Only)

Resulting I²C enable readback for E-EDID access on Port D, after a combination of manual and automatic functions.

Function

EDID_D_ENABLED	Description
0	Disabled
1	Enabled

Notes:

- When the internal E-EDID is enabled on more than one port (for example, Port A and Port B), the corresponding enable controls (for example, MAN_EDID_A_ENABLE and MAN_EDID_B_ENABLE) should be set high in one single I²C write. This ensures the fastest calculation of the checksums.
- If the internal E-EDID RAM is enabled for one specific port (for example, Port A), an external E-EDID storage device should not be connected on the DDC bus of that port.
- The internal E-EDID can be read by the Current Address Read sequences on the DDC ports.
- The ADV7630 supports the segment pointer, which is set at Device Address 0x60 through the DDC bus and used in combination with the internal E-EDID address (0xA0) to access the internal E-EDID.

E-EDID Support for Power-Down Mode

The ADV7630 can support internal E-EDID access when no system power is present by using the +5 V supply available on the HDMI cable, if present (refer to the EDID Available in Rx Power-Off Mode section). Using this feature, an application that integrates the ADV7630 can make its E-EDID available to an HDMI source. This provides compatibility with HDMI transmitters that require the E-EDID to be available when the system is powered down.

In cable supply mode, the part operates in a very low power state with only the minimum of internal circuitry enabled for the internal E-EDID. This allows the E-EDID/repeater controller to load the E-EDID image from an external SPI EEPROM into the internal E-EDID RAM. The E-EDID/repeater controller also updates the SPA of each port (refer to the Main I2C Port section), computes the required E-EDID checksums, and enables the internal E-EDID.

+5 V SUPPLY

The ADV7630 can receive power from the +5 V power signal line of an HDMI cable(s). The ADV7630 has a internal +3.3 V and +1.8 V regulators. The output of the +3.3 V regulator supplies power to the E-EDID/repeater controller, internal ring oscillator, and internal E EDID RAM. It also supplies a 3.3 V external output onto the REG_3P3V pin, which can be used to power an external SPI EEPROM. This allows a system containing the ADV7630 to present an E-EDID image to the HDMI source, even if no system power is available.

When this cable supply mode is initiated, the internal E-EDID is automatically configured and the part loads its internal E-EDID with the information in the SPI EEPROM, and internal E-EDID is enabled on all ports.

Note: The external SPI EEPROM used in a system should consume no more than 5 mA of current. This is required to ensure that no more than 10 mA in total is drawn from the +5 V HDMI cable supply.

TRANSITIONING FROM CABLE SUPPLY MODE

If the part starts in cable supply mode and then transitions into normal operation mode (that is, full system power available), the information in the internal E-EDID is not overwritten. The internal E-EDID remains active on the HDMI port(s) for which the E-EDID was accessed. This prevents disturbing E-EDID read requests from HDMI sources connected to the ADV7630.

It is possible to disable the automatic enable of internal E-EDID on the HDMI ports when the part comes out of cable supply mode, by setting DISABLE_AUTO_EDID.

DISABLE_AUTO_EDID, Repeater Map, Address 0x7A[3]

Disables all automatic enables for internal E-EDID.

Function

DISABLE_AUTO_EDID	Description
0 (default)	Automatic enable of internal E-EDID on HDMI ports when the part comes out of power-down mode. Only the ports accessed during cable-supply mode become enabled.
1	Disable automatic enable of internal E-EDID on HDMI ports when the part comes out of power-down mode.

SPI INTERFACE

The ADV7630 has a 4-pin SPI interface to load the E-EDID information from the SPI EEPROM into the internal E-EDID RAM.

- EP_MOSI
- $\overline{\text{EP\_CS}}$
- EP_MISO
- EP_SCK

The SPI interface offers the user controls to tristate the SPI pins, load the E-EDID data image from the SPI EEPROM into the internal E-EDID RAM, or store the E-EDID data image from the internal E-EDID RAM into the SPI EEPROM.

EXT_EEPROM_TRI, Repeater Map, Address 0x72[6]

Tristates the output pins to the external SPI EEPROM.

Function

EXT_EEPROM_TRI	Description
0 (default)	SPI interface outputs enabled
1	SPI interface outputs tristated

LOAD_EDID, Repeater Map, Address 0x77[1] (Self-Clearing)

Trigger to force loading internal E-EDID RAM with external SPI EEPROM contents. This automatically triggers a CKSUM_CALC event.

Function

LOAD_EDID	Description
0 (default)	No effect
1	Load internal E-EDID with SPI EEPROM contents

STORE_EDID, Repeater Map, Address 0x77[0] (Self-Clearing)

Trigger to write contents of internal E-EDID RAM to external SPI EEPROM.

Function

STORE_EDID	Description
0 (default)	No effect
1	Write contents of internal E-EDID to SPI EEPROM

SPI EEPROM Data Structure

The ADV7630 requires data in the SPI EEPROM to be stored as shown in Figure 7.

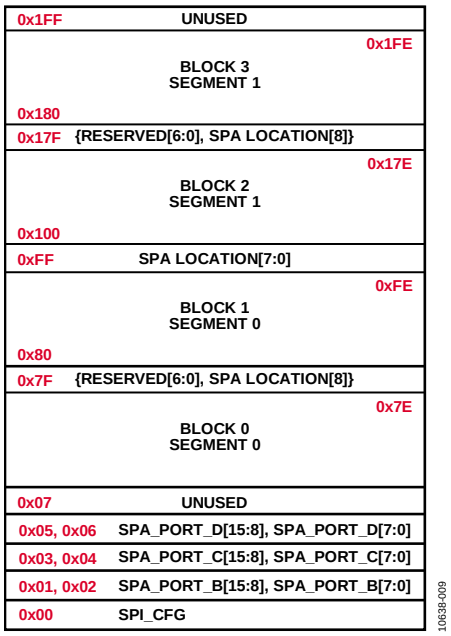


Figure 7. SPI EEPROM Data Image Structure

The SPA location is stored in lieu of the checksums; the part recalculates the checksums after the E-EDID data is read.

SPI_CFG is a 6-bit configuration field located in a first byte of SPI memory (Bits [5:0] at 0x00). It allows the seting of parameters such as number of blocks stored in external EEPROM and HPA behavior in power-off mode. SPI_CFG consists of bits listed in the following table.

On power-up and when the LOAD_EDID command is issued, the SPI_CFG register located in KSV Map Register 0x7C[5:0] can be loaded with the value from an external SPI memory. The register is loaded after the part is powered up or after releasing the previously asserted reset signal (via the RESET pin). In addition, the SPI_CFS register can have its value loaded after issuing the I^2C LOAD_EDID command.

Table 9. SPI_CFG Bit Descriptions

SPI_CFG Bits	Description
SPI_CFG[5]	Reserved bit. It must be set to 1.
SPI_CFG[4]	Reserved bit. It must be set to 0.
SPI_CFG[3]	Unused.
SPI_CFG[2]	Clear HPA in power-off. This bit sets behavior of HPA when HDMI cable with +5 V is plugged into the powered-down ADV7630. When this bit is set to 1, HPA is asserted low when HDMI +5 V is available on the port and the ADV7630 is powered down. When this bit is set to 0, HPA is set low on the port when HDMI +5 V signal is available on the input port and the ADV7630 is powered down.
SPI_CFG[1:0]	Number of 256 byte blocks present in EEPROM. This bit should be set to 1, 2 or 3.

Notes:

- 4 Kb SPI EEPROM must be used to store a 3-block to 4-block E-EDID image.
- 2 Kb or 4 Kb SPI EEPROM must be used to store a 2-block E-EDID image.

Using the ADV7630 Without External SPI Memory

It is possible to use the ADV7630 without external memory attached. In this case, the SPI_MOSI, SPI_SCK, SPI_CS lines should be left floating. Depending on the desired HPA lines (HPA_A, HPA_B, HPA_C, HPA_D) behavior, the SPI_MISO line should be connected to either REG_3P3V or ground

- SPI_MISO tied to REG_3P3V. Causes HPA to be low when cable is plugged into chassis-powered-down ADV7630
- SPI_MISO left floating or tied to ground. Causes HPA to be high when cable is plugged into chassis-powered-down ADV7630

STRUCTURE OF INTERNAL E-EDID MEMORY

The ADV7630 has 512 bytes of internal memory divided into two 256-byte segments (Segment 0 and Segment 1). Internal memory after power-up or after EDID/HDCP reset (HDCP_REPT_EDID_RESET) has all its bytes set to 0 by the EDID/Repeater controller. This operation takes less than 1 ms, and it is recommended to wait at least 1 ms before initializing EDID Map with an E-EDID image.

Internal memory can be fully accessed via the EDID I²C Map. To do so, the EDID I²C map address must be assigned (using EDID_MAP_SLAVE located in the IO Map, Register 0xFA (refer to Table 39); and one 256-byte segment must be chosen using the HDMI_EDID_SEGMENT_SEL register.

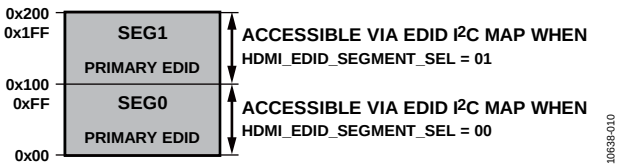


Figure 8. Internal E-EDID Memory Structure

HDMI_EDID_SEGMENT_SEL, Repeater Map, Address 0x7A[2:0]

Selects one of the two SRAM memory banks for HDMI EDID segments to be accessed via the EDID I²C Map.

Function

HDMI_EDID_SEGMENT_SEL[1:0]	Description
00 (default)	Main I²C EDID access for HDMI EDID Segment 0
01	Main I²C EDID access for HDMI EDID Segment 1

The internal E-EDID can be independently enabled on any Port X (where X = A, B, C, D) of the HDMI RX ports by setting MAN_EDID_X_ENABLE (MAN_EDID_A_ENABLE, … MAN_EDID_D_ENABLE) to 1. Once enabled, Port X can provide content of primary EDID or secondary EDID. When an internal E-EDID is enabled on Port X = A, B, C, D, the Hot Plug on that port should not be asserted until the EDID Map is completely initialized with E-EDID.

When EDID is enabled on Port X = A, B, C, D, the EDID content can be read through the DDC lines of Port X. The DDC lines use I²C protocol with Device Address 0xA0. Table 10 shows content presented to HDMI source once E-EDID is enabled.

Table 10. E-EDID Content Presented to HDMI Source

Considered HDMI Input	Orignal Source of data	Bytes Modified from Original Source of Data
Port A	Segment 0 and Segment 1 Bytes[0:511]	SPA_BYTES: not modified. Checksums: checksum bytes located at 0x7F, 0xFF, 0x17F, 0x1FF are replaced with newly recalculated[1] checksums. Rest of data remains as it is in original source of data.
Port B	Segment 0 and Segment 1 Bytes[0:511]	SPA_BYTES: bytes located at offset indicated by SPA_LOCATION[2] and SPA_LOCATION + 1 are replaced with values SPA_PORT_B[15:8] and SPA_PORT_B[7:0]. Checksums: checksum bytes located at 0x7F, 0xFF, 0x17F, 0x1FF are replaced with newly recalculated[1] checksums. Rest of data remains as it is in original source of data.
Port C	Segment 0 and Segment 1 Bytes[0:511]	SPA_BYTES: bytes located at offset indicated by SPA_LOCATION[2] and SPA_LOCATION + 1 are replaced with values SPA_PORT_C[15:8] and SPA_PORT_C[7:0]. Checksums: checksum bytes located at 0x7F, 0xFF, 0x17F, 0x1FF are replaced with newly calculated[1] checksums. Rest of data remains as it is in original source of data.
Port D	Segment 0 and Segment 1 Bytes[0:511]	SPA_BYTES: bytes located at offset indicated by SPA_LOCATION[2] and SPA_LOCATION + 1 are replaced with values SPA_PORT_D[15:8] and SPA_PORT_D[7:0]. Checksums: checksum bytes located at 0x7F, 0xFF, 0x17F, 0x1FF are replaced with newly calculated[1] checksums. Rest of data remains as it is in original source of data.

[1] Recalculation of EDID checksums is done by EEDID/Repeater controller. Checksums are calculated once EDID is enabled on Port X = A, B, C, D by MAN_EDID_X_ENABLE.
[2] SPA_LOCATION must be programmed with a value greater than (between Bytes 0x80 andByte 0xFE) because SPA is always located in CEA extension blocks.

Note: The SPA_PORT_B[15:0], SPA_PORT_C, SPA_PORT_D registers do not have to be programmed with an actual SPA value. They can be programmed with any value that must be read from the location SPA_LOCATION[7:0] when the internal E-EDID is accessed from the DDC lines of Port B, C, D. This allows support for non CEA-861-compliant E-EDIDs .

The SPA of Port X = B, C, D is the address of Port X in the CEC interface. The SPA comprises of four components: A, B, C, and D as defined in the HDMI specification. They are programmed as follows:

- SPA_PORT_B[15:12] = A
- SPA_PORT_B[11:8] = B
- SPA_PORT_B[7:4] = C
- SPA_PORT_B[3:0] = D

SPA_PORT_B[15:0], Repeater Map, *Address 0x52[7:0]; Address 0x53[7:0]*

Source physical address for Port B. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID.

Function

SPA_PORT_B[15:0]	Description
0000000000000000 (default)	Default value
xxxxxxxxxxxxxxxx	Source physical address of Port B

SPA_LOCATION[7:0], Repeater Map, *Address 0x70[7:0]*

This is the location in the E-EDID record where the SPA is located.

Function

SPA_LOCATION[7:0]	Description
11000000 (default)	Default value
xxxxxxxx	Location of source physical address in internal E-EDID of Ports B, C and D

PORT_B_CHECKSUM[7:0], Repeater Map, *Address 0x61[7:0]*

This is the checksum for the second half of the Port B E-EDID. This is calculated automatically.

Function

PORT_B_CHECKSUM[7:0]	Description
00000000 (default)	Default value
xxxxxxxx	Checksum for E-EDID block containing SPA for Port B

SPA_PORT_C[15:0], Repeater Map, *Address 0x54[7:0]; Address 0x55[7:0]*

Source physical address for Port C. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID.

Function

SPA_PORT_C[15:0]	Description
0000000000000000 (default)	Default value
xxxxxxxxxxxxxxxx	Source physical address of Port C

PORT_C_CHECKSUM[7:0], Repeater Map, *Address 0x62[7:0]*

This is the checksum for the second half of the Port C E-EDID. This is calculated automatically.

Function

PORT_C_CHECKSUM[7:0]	Description
00000000 (default)	Default value
xxxxxxxx	Checksum for E-EDID block containing SPA for Port C

SPA_PORT_D[15:0], Repeater Map, *Address 0x56[7:0]; Address 0x57[7:0]*

Source physical address for Port D. This is used for CEC and is located in the HDMI Vendor Specific data block in the E-EDID.

Function

SPA_PORT_D[15:0]	Description
0000000000000000 (default)	Default value
xxxxxxxxxxxxxxxx	Source physical address of Port D

PORT_D_CHECKSUM[7:0], Repeater Map, *Address 0x63[7:0]*

This is the checksum for the second half of the Port D E-EDID. This is calculated automatically.

Function

PORT_D_CHECKSUM[7:0]	Description
00000000 (default)	Default value
xxxxxxxx	Checksum for E-EDID block containing SPA for Port D

SPA CONFIGURATION

When the E-EDID/repeater controller configures the internal E-EDID in cable supply mode (see the Transitioning From Cable Supply Mode section), it also updates the SPA registers for each port according to the SPA read from the external SPI EEPROM. The 2-byte SPA is located at the address specified by SPA_LOCATION in Address 0x7F and Address 0xFF of the SPI EEPROM. The SPA of each port is set as follows:

- SPA for Port A, located in E-EDID RAM, is set to A.B.C.D
- SPA for Port B, **SPA_PORT_B[15:0]**, is set to A+1.B.C.D
- SPA for Port C, **SPA_PORT_C[15:0]**, is set to A+2.B.C.D
- SPA for Port D, **SPA_PORT_D[15:0]**, is set to A+3.B.C.D

where A.B.C.D is the 2-byte SPA read from the SPI EEPROM. The format A.B.C.D is described in the HDMI specification.

EXTERNAL E-EDID

The ADV7630 powers up the internal E-EDID from an HDMI +5 V signal. In this case, it provides E-EDID functionality via DDC lines without any addditional I^2C writes. This could lead to a conflict of two devices having same addresses: E-EDID attached to DDC lines and internal E-EDID visible on DDC lines. To avoid this situation, it is recommended not to use external E-EDID on DDC lines.

TMDS EQUALIZATION

The ADV7630 incorporates active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at long lengths and higher frequencies. The ADV7630 is capable of equalizing for cable lengths up to 30 meters.

The ADV7630 has programmed equalizer settings for three frequency bandwidth ranges. The internally measured TMDS frequency is compared against these limits. The ADV7630 then applies the corresponding equalizer settings according to the detected range.

Note: The Transition Minimized Differential Signaling (TMDS) equalization frequency of the active HDMI port can be read back in the TMDSFREQ[8:0] and TMDSFREQ_FRAC[6:0] registers.

Port Selection

HDMI_PORT_SELECT_TX_A[2:0] and HDMI_PORT_SELECT_TX_B[2:0] allow for the selection of the active HDMI port that is passed to the TXA and TXB outputs, respectively. HDMI_PORT_SELECT_TX_A and HDMI_PORT_SELECT_TX_B must be set to the same input port.

HDMI_PORT_SELECT_TX_A[2:0], HDMI, Address 0x00[2:0]

This 3-bit control is used to select the HDMI port for the primary path (that is, for TxA).

Function

HDMI_PORT_SELECT_TX_A[2:0]	Description
000 (default)	Port A
001	Port B
010	Port C
011	Port D

HDMI_PORT_SELECT_TX_B[2:0], HDMI, Address 0x0D[6:4]

This 3-bit control is used to select the HDMI port for the secondary path (that is, for TXB).

Function

HDMI_PORT_SELECT_TX_B[2:0]	Description
000 (default)	Port A
001	Port B
010	Port C
011	Port D

FAST SWITCHING AND BACKGROUND PORT SELECTION

The ADV7630 incorporates a fast switching feature. This feature allows the user of a system containing the ADV7630 to switch seamlessly between HDCP encrypted sources. There is no delay in achieving video output previously caused by HDCP authentication. The time required to switch between HDMI sources with HDCP encryption is reduced to a fraction of a second.

Asserting EN_BG_PORT_X (where X is A, B, C, or D) allows this unselected port to be enabled in background mode. Once a port is in background mode, the ADV7630 establishes an HDCP link with its source even if it is not selected. This background authentication allows for fast switching of the HDMI ports.

Note: EN_BG_PORT_X has no effect if the port is already selected.

EN_BG_PORT_A, HDMI, Address 0x02[0]

Background mode enable for Port A. Sets Port A in background mode to establish an HDCP link with its source even if the port is not selected.

Function

EN_BG_PORT_A	Description
0 (default)	Port A disabled, unless selected with HDMI_PORT_SELECT_TX_A or HDMI_PORT_SELECT_TX_B
1	Port A enabled in background mode

EN_BG_PORT_B, HDMI, Address 0x02[1]

Background mode enable for Port B. Sets the Port B in background mode to establish an HDCP link with its source even if the port is not selected.

Function

EN_BG_PORT_B	Description
0 (default)	Port B disabled, unless selected with HDMI_PORT_SELECT_TX_A or HDMI_PORT_SELECT_TX_B
1	Port B enabled in background mode

EN_BG_PORT_C, HDMI, Address 0x02[2]

Background mode enable for Port C. Sets Port C in background mode to establish an HDCP link with its source, even if the port is not selected.

Function

EN_BG_PORT_C	Description
0 (default)	Port C disabled, unless selected with HDMI_PORT_SELECT_TX_A or HDMI_PORT_SELECT_TX_B
1	Port C enabled in background mode

EN_BG_PORT_D, HDMI, Address 0x02[3]

Background mode enable for Port C. Sets Port C in background mode to establish an HDCP link with its source, even if the port is not selected.

Function

EN_BG_PORT_D	Description
0 (default)	Port D disabled, unless selected with HDMI_PORT_SELECT_TX_A or HDMI_PORT_SELECT_TX_B
1	Port D enabled in background mode

The ADV7630 can also perform HDMI parameter measurements on one background port. The following information can then be read from the background measurement and parameter registers:

- BG_TMDSFREQ[8:0]
- BG_TMDSFREQ_FRAC[6:0]
- BG_PIX_REP[3:0]
- BG_PARAM_LOCK
- BG_TOTAL_LINE_WIDTH[13:0]
- BG_LINE_WIDTH[12:0]
- BG_TOTAL_FIELD_HEIGHT[12:0]
- BG_FIELD_HEIGHT[12:0]
- BG_HDMI_INTERLACED
- BG_HDMI_MODE
- BG_AUDIO_DETECTED[3:0]
- BG_AUDIO_LAYOUT
- BG_DST_DOUBLE
- BG_HEADER_REQUESTED[7:0]
- BG_HEADER_BYTE1[7:0]
- BG_PACKET_BYTE2[7:0]
- BG_VALID_PACKET

BG_MEAS_PORT_SEL[2:0], HDMI, Address 0x00[5:3]

BG_MEAS_PORT_SEL[2:0] selects a background port on which HDMI measurements are to be made and provided in the background measurement registers. For this setting to be effective, the port in question must be set as a background port. There is no conflict if this matches the port selected by HDMI_PORT_SELECT.

Function

BG_MEAS_PORT_SEL[2:0]	Description
000 (default)	Port A
001	Port B
010	Port C
011	Port D

BG_MEAS_REQ, HDMI, Address 0x5A[5] (Self-Clearing)

This bit must be set to get the correct measurements of the selected background port. Setting this control sends a request to update the synchronization parameter measurements of the currently selected background port. The port on which the measurement are made is selected by BG_MEAS_PORT_SEL[2:0]**.**

Function

BG_MEAS_REQ	Description
0 (default)	No request to update selected background port synchronization parameter measurements
1	Requests an update of the selected background port synchronization parameter measurements

Note: After setting the self clearing BG_MEAS_REQ bit, the measurements of the TMDS frequency and video parameters of the background ports are valid when BG_MEAS_DONE_RAW goes high.

BG_MEAS_DONE_RAW, IO Map, Address 0x8D[1] (Read Only)

Status of background port measurement completed interrupt signal. When set to 1, it indicates that measurement of TMDS frequency and video parameters on the selected background port have been completed. Once set, this bit remains high until it is cleared via BG_MEAS_DONE_CLR.

Function

BG_MEAS_DONE_RAW	Description
0	Measurements of TMDS frequency and video parameters of background port not finished or not requested
1	Measurements of TMDS frequency and video parameters of background port are ready

BG_HDMI_MODE, HDMI, Address 0xEB[0] (Read Only)

This readback provides the HDMI/DVI mode status of the background port determined by BG_MEAS_PORT_SEL[1:0] and is updated continuously.

Function

BG_HDMI_MODE	Description
0	DVI Mode detected on selected BG port
1	HDMI Mode detected on selected BG port

BG_AUDIO_DETECTED[3:0], HDMI Map, Address 0xEE[3:0] (Read Only)

Flags if audio samples were received on the background port and, if so, their type.

Function

BG_AUDIO_DETECTED[3:0]	Description
0000 (default)	No audio samples detected|
0001	Audio sample detected
0010	DSD audio detected
0100	DST audio detected
1000	HBR audio detected

BG_AUDIO_LAYOUT, HDMI Map, Address 0xEE[5] (Read Only)

Flags layout of audio channels in background port selected with BG_MEAS_PORT_SEL. Valid only when BG_AUDIO_DETECTED_BG flags audio sample packets or DSD audio packets have been detected.

Function

BG_AUDIO_LAYOUT	Description
0 (default)	Layout 0
1	Layout 1

BG_DST_DOUBLE, HDMI Map, Address 0xEE[4] (Read Only)

Flags whether DST audio is sampled at single or double transfer rate in the background port with BG_MEAS_PORT_SEL. Valid Only when BG_AUDIO_DETECTED flags DST packets have been received.

Function

BG_DST_DOUBLE	Description
0 (default)	DST sample rate equals transfer rate
1	DST sample rate doubles transfer rate

BG_HEADER_REQUESTED[7:0], HDMI Map, Address 0xEF[7:0]

Selects the type of InfoFrame/packet to be provided for readback in the background port header and packet registers (0xF0 to 0xF5). The value set in this register is compared against the detected InfoFrame/packet header byte 0. If they match, header byte 1 and data bytes 1 to 5 are stored. Default value of 0x82 is the InfoFrame type of AVI InfoFrame.

Function

BG_HEADER_REQUESTED[7:0]	Description
xxxxxxxx	Header value requested. This is compared with detected packet headers. If a match is found, data is stored in Registers 0xF0 to Register 0xF5.

BG_HEADER_BYTE1[7:0], HDMI Map, Address 0xF0[7:0] (Read Only)

Byte 1 of header for the InfoFrame/Packet selected to be read in background port.

Function

BG_HEADER_BYTE1[7:0]	Description
xxxxxxxx	Header Byte 1 data . Valid only if BG_VALID_PACKET is high.

BG_PACKET_BYTE2[7:0], HDMI Map, Address 0xF2[7:0] (Read Only)

Byte 2 of packet for the InfoFrame/Packet selected to be read in background port.

Function

BG_PACKET_BYTE2[7:0]	Description
xxxxxxxx	Packet Byte 2 data . Valid only if BG_VALID_PACKET is high.

BG_VALID_PACKET, HDMI Map, Address 0xF6[0] (Read Only)

Readbacks of packets in BG port are valid only if this signal is high.

Function

BG_VALID_PACKET	Description
0 (default)	BG header and packet readbacks not valid
1	BG header and packet readbacks are valid

TMDS_CLK_A_RAW, IO Map, Address 0x6A[3] (Read Only)

Raw status of Port A TMDS clock detection signal.

Function

TMDS_CLK_A_RAW	Description
0	No TMDS clock detected on Port A
1	TMDS clock detected on Port A

TMDS_CLK_B_RAW, IO Map, Address 0x6A[2] (Read Only)

Raw status of Port B TMDS clock detection signal.

Function

TMDS_CLK_B_RAW	Description
0	No TMDS clock detected on Port B
1	TMDS clock detected on Port B

TMDS_CLK_C_RAW, IO Map, Address 0x6A[1] (Read Only)

Raw status of Port C TMDS clock detection signal.

Function

TMDS_CLK_C_RAW	Description
0	No TMDS clock detected on Port C
1	TMDS clock detected on Port C

TMDS_CLK_D_RAW, IO Map, Address 0x6A[0] (Read Only)

Raw status of Port D TMDS clock detection signal.

Function

TMDS_CLK_D_RAW	Description
0	No TMDS clock detected on Port D
1	TMDS clock detected on Port D

CLOCK AND DATA TERMINATION CONTROL

The ADV7630 provides controls for the TMDS clock and data termination on all HDMI ports. The ADV7630 also offers automatic or manual termination closure of the selected port, and individual manual control over the four ports.

Note: The clock termination of selected port must always be enabled.

TERM_AUTO, HDMI, Address 0x01[0]

This bit allows the user to select automatic or manual control of clock termination. If automatic mode termination is enabled, then the termination on the port selected is enabled. The termination is disabled on all other ports.

Function

TERM_AUTO	Description
0 (default)	Disable automatic control of the TMDS terminations
1	Enable automatic control of the TMDS terminations

Note: To enable the fast switching feature, the termination should be set manually for each port.

When manual mode is enabled, the termination for each port is set individually by the CLOCK_TERMX_DISABLE control bits (where X = A, B, C, or D).

CLOCK_TERMA_DISABLE, HDMI, Address 0x83[0]

Disable clock termination on Port A. Can be used when TERM_AUTO is set to 0.

Function

CLOCK_TERMA_DISABLE	Description
0	Enable termination on Port A
1 (Default)	Disable termination on Port A

CLOCK_TERMB_DISABLE, HDMI, Address 0x83[1]

Disable clock termination on Port B. Can be used when TERM_AUTO is set to 0.

Function

CLOCK_TERMB_DISABLE	Description
0	Enable termination on Port B
1 (Default)	Disable termination on Port B

CLOCK_TERMC_DISABLE, HDMI, Address 0x83[2]

Disable clock termination on Port C. Can be used when TERM_AUTO is set to 0.

Function

CLOCK_TERMC_DISABLE	Description
0	Enable termination on Port C
1 (Default)	Disable termination on Port C

CLOCK_TERMD_DISABLE, HDMI, Address 0x83[3]

Disable clock termination on Port D. Can be used when TERM_AUTO is set to 0.

Function

CLOCK_TERMD_DISABLE	Description
0	Enable termination on Port D
1 (Default)	Disable termination on Port D

TMDS MEASUREMENT

The ADV7630 contains logic that measures the frequency of the TMDS clock transmitted on the TMDS clock channel. The TMDS frequency can be read back via the TMDSFREQ[8:0] and TMDSFREQ_FRAC[6:0] registers.

TMDS Measurement After TMDS PLL

The TMDSFREQ measurement is provided by a clock measurement circuit located after the TMDS PLL. The TMDS PLL must, therefore, be locked to the incoming TMDS clock in order for the TMDSFREQ and TMDSFREQ_FRAC registers to return a valid measurement. The TMDS frequency can be obtained using Equation 1.

$$F_{TMDS} = TMDSFREQ + \frac{TMDSFREQ\_FRAC}{128}$$

Equation 1. TMDS Frequency in MHz (Measured After TMDS PLL)

Notes:

- TMDS PLL lock status can be monitored via TMDS_PLL_LOCKED.
- Figure 9 shows the algorithm that can be implemented on an external controller to monitor the TMDS clock frequency.
- TMDS_PLL_LOCKED flag should be considered valid if a TMDS clock is input on the HDMI port selected via HDMI_PORT_SELECT_TX_A[2:0].
- NEW_TMDS_FRQ_RAW flag can be used to monitor if the TMDS frequency on the selected primary HDMI port (HDMI_PORT_SELECT_TX_A[2:0]) changes by a programmable threshold.
- TMDS frequency on the selected secondary HDMI port (HDMI_PORT_SELECT_TX_B[2:0]) can be read back using background measurements. To read back, BG_MEAS_PORT_SEL[2:0] should be set to the desired HDMI input. Then BG_MEAS_REQ should be set high. Once BG_MEAS_DONE_RAW is high, BG_TMDSFREQ[8:0] contains valid data that can be read back.
- The ADV7630 can be configured to trigger an interrupt when the bit NEW_TMDS_FRQ_RAW changes from 0 to 1. In that configuration, the interrupt status NEW_TMDS_FRQ_ST indicates that the NEW_TMDS_FRQ_RAW bit has changed from 0 to 1. Refer to the Interrupt Architecture Overview section for additional information on the configuration of interrupts.

TMDSFREQ[8:0], HDMI, Address 0x51[7:0]; Address 0x52[7] (Read Only)

This register provides a full precision integer TMDS frequency measurement. This register refers to a primary HDMI port selected.

Function	
TMDSFREQ[8:0]	**Description**
000000000	Outputs 9-bit TMDS frequency measurement in MHz
xxxxxxxxx	Outputs 9-bit TMDS frequency measurement in MHz

TMDSFREQ_FRAC[6:0], HDMI, Address 0x52[6:0] (Read Only)

A readback to indicate the fractional bits of measured frequency of PLL recovered TMDS clock. The unit is 1/128 MHz. This register refers to a primary HDMI port selected.

Function	
TMDSFREQ_FRAC[6:0]	**Description**
0000000	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz
xxxxxxx	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz

BG_TMDSFREQ[8:0], HDMI, Address 0xE0[7:0]; Address 0xE1[7] (Read Only)

This register provides a precision integer TMDS frequency measurement on the background port selected by BG_MEAS_PORT_SEL. The value provided is the result of a single measurement of the TMDS PLL frequency in MHz. This value is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is valid only when BG_PARAM_LOCK is set to 1.

Function	
BG_TMDSFREQ[8:0]	**Description**
000000000	Outputs 9-bit TMDS frequency measurement in MHz
xxxxxxxxx	Outputs 9-bit TMDS frequency measurement in MHz

BG_TMDSFREQ_FRAC[6:0], HDMI, Address 0xE1[6:0] (Read Only)

This register provides a precision fractional measurement of the TMDS frequency on the background port selected by BG_MEAS_PORT_SEL. The unit is 1/128 MHz and the value is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is valid only when BG_PARAM_LOCK is set to 1.

Function

BG_TMDSFREQ_FRAC[6:0]	**Description**
0000000	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz
xxxxxxx	Outputs 7-bit TMDS fractional frequency measurement in 1/128 MHz

TMDS_PLL_LOCKED, HDMI, Address 0x04[1] (Read Only)

A readback to indicate if the TMDS PLL is locked to the TMDS clock input of the selected HDMI port.

Function

TMDS_PLL_LOCKED	**Description**
0	TMDS PLL is not locked
1	TMDS PLL is locked to the TMDS clock input of the selected HDMI port

TMDSPLL_LCK_A_RAW, IO Map, Address 0x6A[7] (Read Only)

A readback to indicate the raw status of the Port A TMDS PLL lock signal.

Function

TMDSPLL_LCK_A_RAW	**Description**
0	TMDS PLL on Port A is not locked
1	TMDS PLL on Port A is locked to the incoming clock

TMDSPLL_LCK_B_RAW, IO Map, Address 0x6A[6] (Read Only)

A readback to indicate the raw status of the Port B TMDS PLL lock signal.

Function

TMDSPLL_LCK_B_RAW	**Description**
0	TMDS PLL on Port B is not locked
1	TMDS PLL on Port B is locked to the incoming clock

TMDSPLL_LCK_C_RAW, IO Map, Address 0x6A[5] (Read Only)

A readback to indicate the raw status of the Port C TMDS PLL lock signal.

Function

TMDSPLL_LCK_C_RAW	Description
0	TMDS PLL on Port C is not locked
1	TMDS PLL on Port C is locked to the incoming clock

TMDSPLL_LCK_D_RAW, IO Map, Address 0x6A[4] (Read Only)

A readback to indicate the raw status of the Port D TMDS PLL lock signal.

Function

TMDSPLL_LCK_D_RAW	Description
0	TMDS PLL on Port D is not locked
1	TMDS PLL on Port D is locked to the incoming clock

NEW_TMDS_FRQ_RAW, IO Map, Address 0x83[1] (Read Only)

Status of New TMDS Frequency interrupt signal. When set to 1 it indicates the TMDS frequency has changed by more than the tolerance set in FREQTOLERANCE[3:0]. Once set, this bit remains high until it is cleared via NEW_TMDS_FREQ_CLR.

Function

NEW_TMDS_FRQ_RAW	Description
0	TMDS frequency has not changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI Map
1	TMDS frequency has changed by more than tolerance set in FREQTOLERANCE[3:0] in the HDMI Map

FREQTOLERANCE[3:0], HDMI, Address 0x0D[3:0]

Sets the tolerance in MHz for new TMDS frequency detection. This tolerance is used for the audio mute mask MT_MSK_VCLK_CHNG and the HDMI status bit NEW_TMDS_FRQ_RAW.

Function

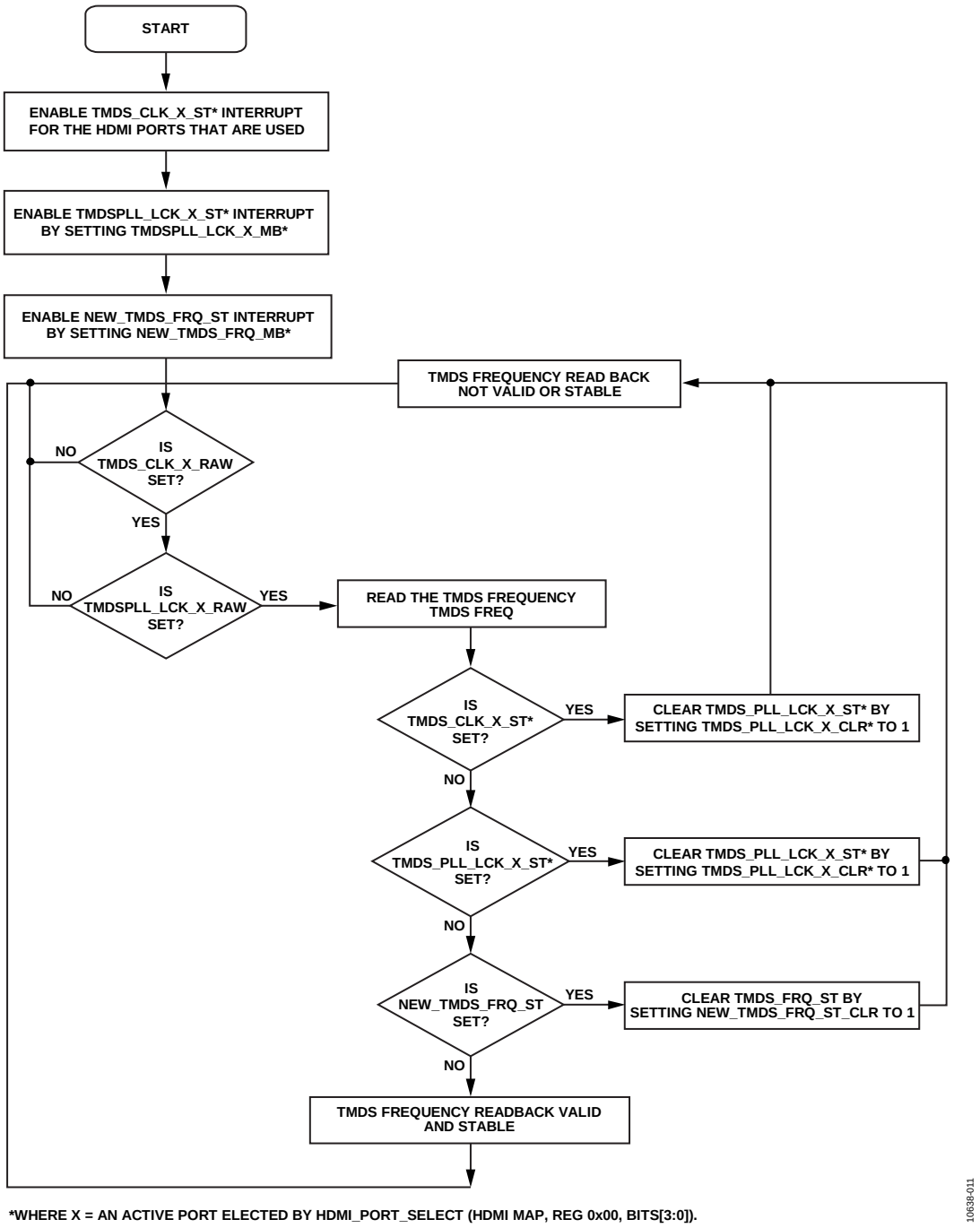
FREQTOLERANCE[3:0]	Description
0100 (default)	Default tolerance in MHz for new TMDS frequency detection
xxxx	Tolerance in MHz for new TMDS frequency detection

VCLK_CHNG_RAW, IO Map, Address 0x83[6] (Read Only)

Status of video clock changed interrupt signal. When set to 1, it indicates that irregular or missing pulses are detected in the TMDS clock. Once set, this bit remains high until it is cleared via VCLK_CHNG_CLR.

Function

VCLK_CHNG_RAW	Description
0 (default)	No irregular or missing pulse detected in TMDS clock
1	Irregular or missing pulses detected in TMDS clock triggered this interrupt



*WHERE X = AN ACTIVE PORT ELECTED BY HDMI_PORT_SELECT (HDMI MAP, REG 0x00, BITS[3:0]).

Figure 9. Monitoring TMDS Clock Frequency on Primary Port Selected by HDMI_PORT_SELECT_TX_A

PIXEL REPETITION

BG_PIX_REP[3:0], HDMI, Address 0xEA[7:4] (Read Only)

Background port pixel repetition status for the background HDMI port determined by BG_MEAS_PORT_SEL[1:0]. The readback provides the pixel repetition value in AVI InfoFrame and is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is valid only when BG_PARAM_LOCK is set to 1.

Function

BG_PIX_REP[3:0]	Description
0000	1x
0001	2x
0010	3x
0011	4x
0100	5x
0101	6x
0110	7x
0111	8x
1000	9x
1001	10x
1010 – 1111	Reserved

HDCP SUPPORT

HDCP Decryption Engine

The HDCP decryption engine allows for the reception and decryption of HDCP content-protected video and audio data. In the HDCP authentication protocol, the transmitter authenticates the receiver by accessing the HDCP registers of the ADV7630 over the DDC bus. Once the authentication is initiated, the HDCP decryption integrated in the ADV7630 computes and updates a decryption mask for every video frame. This mask is applied to the incoming data at every clock cycle to yield decrypted video and audio data.

HDMI_CONTENT_ENCRYPTED, HDMI, Address 0x05[6] (Read Only)

A readback to indicate if the input stream processed by the HDMI core is HDCP encrypted or not. This register refers to a primary HDMI port selected.

Function

HDMI_CONTENT_ENCRYPTED	Description
0	Input stream processed by the HDMI core is not HDCP encrypted
1	Input stream processed by the HDMI core is HDCP encrypted

HDMI_ENCRPT_X_RAW (where X = A, B, C or D) reports the encryption status of the data present on each individual HDMI port.

Note: These bits are reset to 0 if an HDMI packet detection reset occurs.

HDMI_ENCRPT_A_RAW, IO Map, Address 0x6F[7] (Read Only)

Raw status of Port A encryption detection signal.

Function

HDMI_ENCRPT_A_RAW	Description
0	Current frame in Port A is not encrypted
1	Current frame in Port A is encrypted

HDMI_ENCRPT_B_RAW, IO Map, Address 0x6F[6] (Read Only)

Raw status of Port B encryption detection signal.

Function

HDMI_ENCRPT_B_RAW	Description
0	Current frame in Port B is not encrypted
1	Current frame in Port B is encrypted

HDMI_ENCRPT_C_RAW, IO Map, Address 0x6F[5] (Read Only)

Raw status of Port C encryption detection signal.

Function

HDMI_ENCRPT_C_RAW	Description
0	Current frame in Port C is not encrypted
1	Current frame in Port C is encrypted

HDMI_ENCRPT_D_RAW, IO Map, Address 0x6F[4] (Read Only)

Raw status of Port D encryption detection signal.

Function

HDMI_ENCRPT_D_RAW	Description
0	Current frame in Port D is not encrypted
1	Current frame in Port D is encrypted

Notes:

- The ADV7630 supports the 1.1_FEATURES, FAST_REAUTHENTICATION, and FAST_I2C speed HDCP features. The BCAPS register must be initialized appropriately if these features are to be supported by the application integrating the ADV7630. For example, Bit 0 of BCAPS[7:0] is set to 1 to support FAST_REAUTHENTICATION.
- It is recommended that Bit 7 of BCAPS[7:0] be set to 1 if the ADV7630 is used as the front end of an HDMI receiver. This bit should be set to 0 for DVI applications.

Internal HDCP Key OTP ROM

The ADV7630 features an on-chip nonvolatile memory that is preprogrammed with a set of HDCP keys.

HDCP Keys Access Flags

The ADV7630 accesses the internal HDCP key OTP ROM (also referred to as HDCP ROM) on two different occasions:

- After a power-up, the ADV7630 reads the KSV from the internal HDCP ROM (refer to Figure 10).
- After a KSV update from an HDCP transmitter, the ADV7630 reads the KSV and all keys in order to carry out the link verification response (refer to Figure 11).

The host processor can read the HDCP_KEYS_READ and HDCP_KEY_ERROR flags to check that the ADV7630 successfully accessed the HDCP ROM.

HDCP_KEYS_READ, HDMI, Address 0x04[5] (Read Only)

A readback to indicate a successful read of the HDCP keys and/or KSV from the internal HDCP key OTP ROM. A logic high is returned when the read is successful.

Function

HDCP_KEYS_READ	Description
0	HDCP keys and/or KSV not yet read
1	HDCP keys and/or KSV HDCP keys read

HDCP_KEY_ERROR, HDMI, Address 0x04[4] (Read Only)

A readback to indicate if a checksum error occurred while reading the HDCP and/or KSV from the HDCP key ROM. Returns high when HDCP key master encounters an error while reading the HDCP key OTP ROM. This register refers to a primary HDMI port selected.

Function

HDCP_KEY_ERROR	Description
0	No error occurred while reading HDCP keys
1	HDCP keys read error

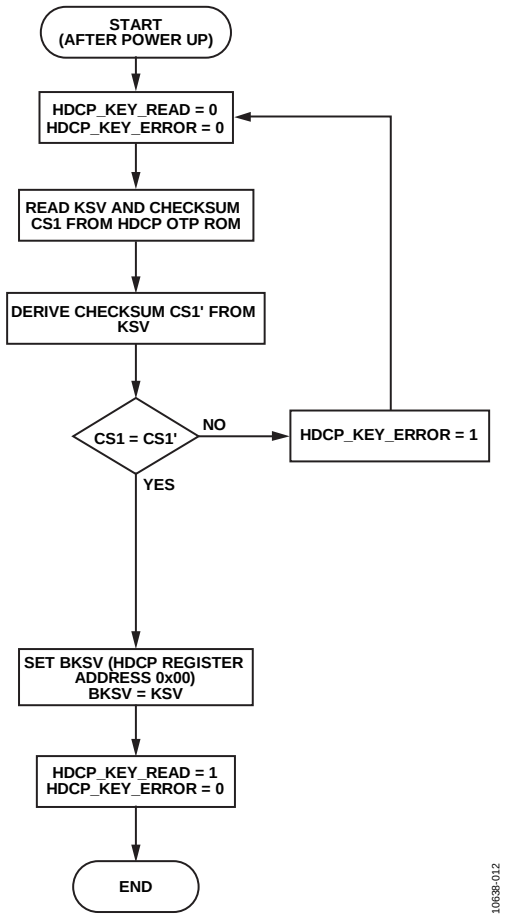


Figure 10. HDCP ROM Access After Power-Up

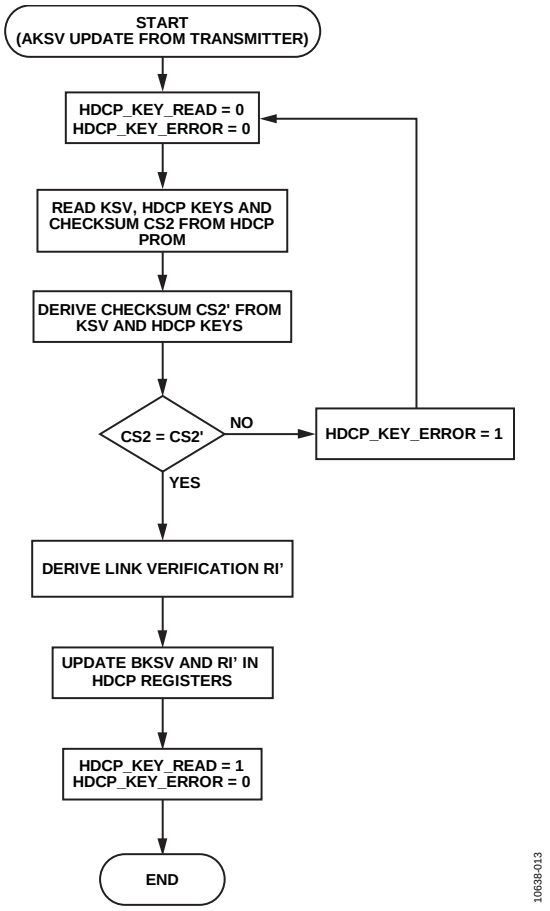


Figure 11. HDCP ROM Access After KSV Update From Transmitter

Notes:

- After the part has powered up, it is recommended to wait for 1 ms before checking the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits. This ensures that the ADV7630 had sufficient time to access the internal HDCP ROM and set the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits.
- After an AKSV update from the transmitter, it is recommended to wait for 2 ms before checking the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits. This ensures that the ADV7630 had sufficient time to access the internal HDCP ROM, and set the HDCP_KEYS_READ and HDCP_KEY_ERROR flag bits.
- When the ADV7630 successfully retrieves the HDCP keys and/or KSV from the internal HDCP ROM, the HDCP_KEYS_READ flag bit is set to 1 and the HDCP_KEY_ERROR flag bit is set to 0.
- The I^2C controllers for the main I^2C lines and the HDCP lines are independent of each other. It is, therefore, possible to access the internal registers of the ADV7630 while it reads the HDCP keys and/or the KSV from the internal HDCP ROM.
- A hardware reset (that is, reset via the $\overline{\text{RESET}}$ pin) does not lead the ADV7630 to read the KSV or the keys from the HDCP ROM.
- The ADV7630 takes 1.8 ms to read the keys from the HDCP ROM.

BACKGROUND PORT HORIZONTAL FILTER MEASUREMENTS

The HDMI horizontal filter performs the measurements described in this section on the HDMI port selected by BG_MEAS_PORT_SEL[2:0].

Note: BG_PARAM_LOCK must be high for background horizontal and vertical measurements to be valid.

BG_PARAM_LOCK, HDMI, Address 0xEA[1] (Read Only)

A flag to indicate that vertical and horizontal parameters were locked during a background measurement.

Function

BG_PARAM_LOCK	Description
0	Horizontal and vertical were not locked when measurement for selected background HDMI port was taken
1	Horizontal and vertical were locked when measurement for selected background HDMI port was taken

BG_TOTAL_LINE_WIDTH[13:0], HDMI, Address 0xE4[5:0]; Address 0xE5[7:0] (Read Only)

Background port total line width, a horizontal synchronization measurement for the background HDMI port that is determined by BG_MEAS_PORT_SEL[1:0]. The value represents the total number of pixels in a line and is updated when an update request is made via the BG_MEAS_REQ control bit. This measurement is valid only when BG_PARAM_LOCK is set to 1.

Function

BG_TOTAL_LINE_WIDTH[13:0]	Description
xxxxxxxxxxxxx	Total number of pixels per line on the background measurement port

BG_LINE_WIDTH[12:0], HDMI, Address 0xE2[4:0]; Address 0xE3[7:0] (Read Only)

A horizontal synchronization measurement for the background HDMI port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the number of active pixels in a line and is updated when an update request is made via the BG_MEAS_REQ control bit.

Function

BG_LINE_WIDTH[12:0]	Description
0000000000000	Number of active pixels per line on the background measurement port
xxxxxxxxxxxxx	Number of active pixels per line on the background measurement port

BACKGROUND PORT VERTICAL FILTER MEASUREMENTS

The HDMI vertical filter performs the measurements described in this section on the HDMI port selected by BG_MEAS_PORT_SEL[2:0].

Note: BG_PARAM_LOCK must be high for background horizontal and vertical measurements to be valid.

BG_TOTAL_FIELD_HEIGHT[12:0], HDMI, Address 0xE8[4:0]; Address 0xE9[7:0] (Read Only)

A vertical synchronization measurement for the background HDMI port determined by BG_MEAS_PORT_SEL[1:0]. The value represents the total number of lines in a field and is updated when an update request is made via the BG_MEAS_REQ control bit.

Function

BG_TOTAL_FIELD_HEIGHT[12:0]	Description
0000000000000	Total number of lines in a field on the background measurement port
xxxxxxxxxxxxx	Total number of lines in a field on the background measurement port

BG_FIELD_HEIGHT[12:0], HDMI, Address 0xE6[4:0]; Address 0xE7[7:0] (Read Only)

Background port field height is a vertical synchronization measurement for a background HDMI port that is determined by BG_MEAS_PORT_SEL[1:0]. The value represents the number of active lines in a field and is updated when a update request is made via the BG_MEAS_REQ control bit.

Function

BG_FIELD_HEIGHT[12:0]	Description
0000000000000	Number of active lines in a field on the background measurement port
xxxxxxxxxxxxx	Number of active lines in a field on the background measurement port

BG_HDMI_INTERLACED, HDMI, Address 0xEA[0] (Read Only)

Background port HDMI input interlace status is a vertical filter measurement for a background HDMI port that is determined by BG_MEAS_PORT_SEL[1:0]. The status readback is updated when a update request is made via the BG_MEAS_REQ control bit. This measurement is valid only when BG_PARAM_LOCK is set to 1.

Function

BG_HDMI_INTERLACED	Description
0	Progressive video format
1	Interlaced video format

Low Frequency Formats

To process the low frame rate video formats such as 720p24, 720p25, 720p30, 1080p23, 1080p24, 1080p30, the NEW_VS_PARAM bit should be set. Refer to Figure 12.

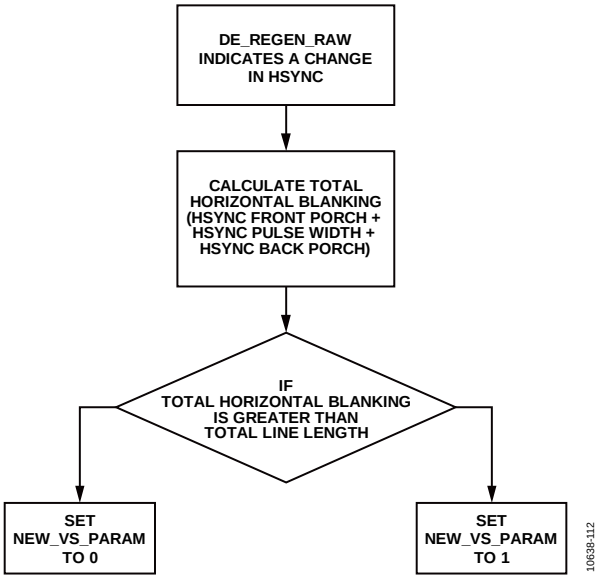


Figure 12. Low Frame Rate Algorithm

NEW_VS_PARAM, HDMI, Address 0x4C[2]

Enables a new version of vertical parameter extraction for evaluation purposes. That is the version in the background port measurement blocks.

Function

NEW_VS_PARAM	Description
0	NEW_VS_PARAM disabled
1	NEW_VS_PARAM enabled

AUDIO MUTING

AV Mute Status

AV_MUTE, HDMI, Address 0x04[6] (Read Only)

Readback of AVMUTE status in the last General Control packet received.

Function

AV_MUTE	Description
0	AVMUTE not set
1	AVMUTE set

PACKETS AND INFOFRAME REGISTERS

In HDMI, auxiliary data is carried across the digital link using a series of packets. The ADV7630 automatically detects and stores the following HDMI packets:

- InfoFrames
- Audio content protection (ACP)
- International Standard Recording Code (ISRC)
- Gamut metadata

When the ADV7630 receives one of these packets, it computes the packet checksum and compares it with the checksum available in the packet. If these checksums are the same, the packets are stored in the corresponding registers. If the checksums are not the same, the packets are discarded. Refer to the EIA/CEA-861D specifications for more information on the packets fields.

InfoFrame Registers

The ADV7630 can store the following InfoFrames:

- Auxiliary video information (AVI) InfoFrame
- Source production descriptor (SPD) InfoFrame
- Audio InfoFrame
- Moving Picture Experts Group (MPEG) Source InfoFrame

InfoFrame Collection Mode

The ADV7630 has two modes for storing the InfoFrame packet sent from the source into the internal memory. By default, the ADV7630 only stores the InfoFrame packets received if the checksum is correct for each InfoFrame.

The ADV7630 also provides a mode to store every InfoFrame sent from the source, regardless of an InfoFrame packet checksum error.

ALWAYS_STORE_INF, HDMI, Address 0x47[0]

A control to force InfoFrames with checksum errors to be stored.

Function

ALWAYS_STORE_INF	Description
0 (default)	Store data from received InfoFrames only if their checksum is correct
1	Always store the data from received InfoFrame regardless of their checksum

AVI_INF_CKS_ERR_RAW, IO Map, Address 0x88[4] (Read Only)

Status of AVI InfoFrame checksum error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an AVI InfoFrame. Once set, this bit remains high until it is cleared via AVI_INF_CKS_ERR_CLR.

Function

AVI_INF_CKS_ERR_RAW	Description
0 (default)	No AVI InfoFrame checksum error has occurred
1	An AVI InfoFrame checksum error has occurred

AUD_INF_CKS_ERR_RAW, IO Map, Address 0x88[5] (Read Only)

Status of Audio InfoFrame checksum error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an Audio InfoFrame. Once set, this bit remains high until it is cleared via AUDIO_INF_CKS_ERR_CLR.

Function

AUD_INF_CKS_ERR_RAW	Description
0 (default)	No Audio InfoFrame checksum error has occurred
1	An Audio InfoFrame checksum error has occurred

SPD_INF_CKS_ERR_RAW, IO Map, Address 0x88[6] (Read Only)

Status of SPD InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for an SPD InfoFrame. Once set, this bit remains high until it is cleared via ASPD_INF_CKS_ERR_CLR.

Function

SPD_INF_CKS_ERR_RAW	Description
0 (default)	No SPD InfoFrame checksum error has occurred
1	An SPD InfoFrame checksum error has occurred

MS_INF_CKS_ERR_RAW, IO Map, Address 0x88[7] (Read Only)

Status of MPEG Source InfoFrame checksum error interrupt signal. When set to 1 it indicates that a checksum error has been detected for an MPEG Source InfoFrame. Once set, this bit remains high until it is cleared via MS_INF_CKS_ERR_CLR.

Function

MS_INF_CKS_ERR_RAW	Description
0 (default)	No MPEG source InfoFrame checksum error has occurred
1	An MPEG source InfoFrame checksum error has occurred

VS_INF_CKS_ERR_RAW, IO Map, Address 0x8D[0] (Read Only)

Status of vendor-specific InfoFrame checksum error interrupt signal. When set to 1, it indicates that a checksum error has been detected for a vendor-specific InfoFrame. Once set, this bit remains high until it is cleared via VS_INF_CKS_ERR_CLR.

Function

VS_INF_CKS_ERR_RAW	Description
0 (default)	No VS InfoFrame checksum error has occurred
1	A VS InfoFrame checksum error has occurred

AVI InfoFrame Registers

Table 11 provides a list of readback registers for the AVI InfoFrame data. Refer to the EIA/CEA-861D specifications for a detailed explanation of the AVI InfoFrame fields.

Table 11. AVI InfoFrame Registers

InfoFrame Map Address	Access Type	Register Name	Byte Name[1]
0xE0	R/W	AVI_PACKET_ID[7:0]	Packet type value
0xE1	R	AVI_INF_VER	InfoFrame version number
0xE2	R	AVI_INF_LEN	InfoFrame length
0x00	R	AVI_INF_PB_0_1	Checksum
0x01	R	AVI_INF_PB_0_2	Data Byte 1
0x02	R	AVI_INF_PB_0_3	Data Byte 2
0x03	R	AVI_INF_PB_0_4	Data Byte 3
0x04	R	AVI_INF_PB_0_5	Data Byte 4
0x05	R	AVI_INF_PB_0_6	Data Byte 5
0x06	R	AVI_INF_PB_0_7	Data Byte 6
0x07	R	AVI_INF_PB_0_8	Data Byte 7
0x08	R	AVI_INF_PB_0_9	Data Byte 8
0x09	R	AVI_INF_PB_0_10	Data Byte 9
0x0A	R	AVI_INF_PB_0_11	Data Byte 10
0x0B	R	AVI_INF_PB_0_12	Data Byte 11
0x0C	R	AVI_INF_PB_0_13	Data Byte 12
0x0D	R	AVI_INF_PB_0_14	Data Byte 13
0x0E	R	AVI_INF_PB_0_15	Data Byte 14
0x0F	R	AVI_INF_PB_0_16	Data Byte 15
0x10	R	AVI_INF_PB_0_17	Data Byte 16
0x11	R	AVI_INF_PB_0_18	Data Byte 17
0x12	R	AVI_INF_PB_0_19	Data Byte 18
0x13	R	AVI_INF_PB_0_20	Data Byte 19
0x14	R	AVI_INF_PB_0_21	Data Byte 20
0x15	R	AVI_INF_PB_0_22	Data Byte 21
0x16	R	AVI_INF_PB_0_23	Data Byte 22
0x17	R	AVI_INF_PB_0_24	Data Byte 23
0x18	R	AVI_INF_PB_0_25	Data Byte 24
0x19	R	AVI_INF_PB_0_26	Data Byte 25
0x1A	R	AVI_INF_PB_0_27	Data Byte 26
0x1B	R	AVI_INF_PB_0_28	Data Byte 27

[1] As defined by the EIA/CEA-861D specifications.

AVI InfoFrame registers are considered valid if AVI_INFO_RAW is set to 1 and AVI_INF_CKS_ERR_RAW is set to 0.

AVI_INFO_RAW, IO Map, Address 0x60[0] (Read Only)

Raw status of AVI InfoFrame detected signal. This bit is set to 1 when an AVI InfoFrame is received and is reset to 0 if no AVI InfoFrame is received for more than seven VSyncs (on the eighth VSync leading edge following the last received AVI InfoFrame), after an HDMI packet detection reset or upon writing to AVI_PACKET_ID.

Function

AVI_INFO_RAW	Description
0 (default)	No AVI InfoFrame has been received within the last seven VSyncs or since the last HDMI packet detection reset
1	An AVI InfoFrame has been received within the last seven VSyncs

Audio InfoFrame Registers

Table 12 provides a list of readback registers available for the Audio InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the Audio InfoFrame fields.

Table 12. Audio InfoFrame Registers

InfoFrame Map Address	Access Type	Register Name	Byte Name[1]
0xE3	R/W	AUD_PACKET_ID[7:0]	Packet Type Value
0xE4	R	AUD_INF_VERS	InfoFrame version number
0xE5	R	AUD_INF_LEN	InfoFrame length
0x1C	R	AUD_INF_PB_0_1	Checksum
0x1D	R	AUD_INF_PB_0_2	Data Byte 1
0x1E	R	AUD_INF_PB_0_3	Data Byte 2
0x1F	R	AUD_INF_PB_0_4	Data Byte 3
0x20	R	AUD_INF_PB_0_5	Data Byte 4
0x21	R	AUD_INF_PB_0_6	Data Byte 5
0x22	R	AUD_INF_PB_0_7	Data Byte 6
0x23	R	AUD_INF_PB_0_8	Data Byte 7
0x24	R	AUD_INF_PB_0_9	Data Byte 8
0x25	R	AUD_INF_PB_0_10	Data Byte 9
0x26	R	AUD_INF_PB_0_11	Data Byte 10
0x27	R	AUD_INF_PB_0_12	Data Byte 11
0x28	R	AUD_INF_PB_0_13	Data Byte 12
0x29	R	AUD_INF_PB_0_14	Data Byte 13

[1] As defined by the EIA/CEA-861D specifications.

Audio InfoFrame registers are considered valid if AUDIO_INFO_RAW is set to 1 and AUD_INF_CKS_ERR_RAW is set to 0.

AUDIO_INFO_RAW, IO Map, Address 0x60[1] (Read Only)

Raw status of Audio InfoFrame detected signal.

Function

AUDIO_INFO_RAW	Description
0 (default)	No AVI InfoFrame has been received within the last three VSyncs or since the last HDMI packet detection reset.
1	An Audio InfoFrame has been received within the last three VSyncs. This bit resets to zero on the fourth VSync leading edge following an Audio InfoFrame, after an HDMI packet detection reset or upon writing to AUD_PACKET_ID.

SPD InfoFrame Registers

Table 13 provides a list of readback registers available for the SPD InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the SPD InfoFrame fields.

Table 13. SPD InfoFrame Registers

InfoFrame Map Address	Access Type	Register Name	Byte Name[1]
0xE6	R/W	SPD_PACKET_ID[7:0]	Packet Type Value
0xE7	R	SPD_INF_VER	InfoFrame version number
0xE8	R	SPD_INF_LEN	InfoFrame length
0x2A	R	SPD_INF_PB_0_1	Checksum
0x2B	R	SPD_INF_PB_0_2	Data Byte 1
0x2C	R	SPD_INF_PB_0_3	Data Byte 2
0x2D	R	SPD_INF_PB_0_4	Data Byte 3
0x2E	R	SPD_INF_PB_0_5	Data Byte 4
0x2F	R	SPD_INF_PB_0_6	Data Byte 5
0x30	R	SPD_INF_PB_0_7	Data Byte 6
0x31	R	SPD_INF_PB_0_8	Data Byte 7
0x32	R	SPD_INF_PB_0_9	Data Byte 8
0x33	R	SPD_INF_PB_0_10	Data Byte 9
0x34	R	SPD_INF_PB_0_11	Data Byte 10
0x35	R	SPD_INF_PB_0_12	Data Byte 11
0x36	R	SPD_INF_PB_0_13	Data Byte 12
0x37	R	SPD_INF_PB_0_14	Data Byte 13
0x38	R	SPD_INF_PB_0_15	Data Byte 14
0x39	R	SPD_INF_PB_0_16	Data Byte 15
0x3A	R	SPD_INF_PB_0_17	Data Byte 16
0x3B	R	SPD_INF_PB_0_18	Data Byte 17
0x3C	R	SPD_INF_PB_0_19	Data Byte 18
0x3D	R	SPD_INF_PB_0_20	Data Byte 19
0x3E	R	SPD_INF_PB_0_21	Data Byte 20
0x3F	R	SPD_INF_PB_0_22	Data Byte 21
0x40	R	SPD_INF_PB_0_23	Data Byte 22
0x41	R	SPD_INF_PB_0_24	Data Byte 23
0x42	R	SPD_INF_PB_0_25	Data Byte 24
0x43	R	SPD_INF_PB_0_26	Data Byte 25
0x44	R	SPD_INF_PB_0_27	Data Byte 26
0x45	R	SPD_INF_PB_0_28	Data Byte 27

[1] As defined by the EIA/CEA-861D specifications.

The Source Product Descriptor InfoFrame registers are considered valid if the following two conditions are met:

- SPD_INFO_RAW is 1.
- SPD_INF_CKS_ERR_RAW is 0. This condition applies only if ALWAYS_STORE_INF is set to 1.

SPD_INFO_RAW, IO Map, Address 0x60[2] (Read Only)

Raw status of SPD InfoFrame detected signal.

Function

SPD_INFO_RAW	Description
0 (default)	No source product description InfoFrame received since the last HDMI packet detection reset.
1	Source product description InfoFrame received. This bit resets to zero after an HDMI packet detection reset or upon writing to SPD_PACKET_ID.

MPEG Source InfoFrame Registers

Table 14 provides a list of readback registers available for the MPEG InfoFrame. Refer to the EIA/CEA-861D specifications for a detailed explanation of the MPEG InfoFrame fields.

Table 14. MPEG InfoFrame Registers

InfoFrame Map Address	Access Type	Register Name	Byte Name[1]
0xE9	R/W	MS_PACKET_ID[7:0]	Packet Type Value
0xEA	R	MS_INF_VERS	InfoFrame version number
0xEB	R	MS_INF_LEN	InfoFrame length
0x46	R	MS_INF_PB_0_1	Checksum
0x47	R	MS_INF_PB_0_2	Data Byte 1
0x48	R	MS_INF_PB_0_3	Data Byte 2
0x49	R	MS_INF_PB_0_4	Data Byte 3
0x4A	R	MS_INF_PB_0_5	Data Byte 4
0x4B	R	MS_INF_PB_0_6	Data Byte 5
0x4C	R	MS_INF_PB_0_7	Data Byte 6
0x4D	R	MS_INF_PB_0_8	Data Byte 7
0x4E	R	MS_INF_PB_0_9	Data Byte 8
0x4F	R	MS_INF_PB_0_10	Data Byte 9
0x50	R	MS_INF_PB_0_11	Data Byte 10
0x51	R	MS_INF_PB_0_12	Data Byte 11
0x52	R	MS_INF_PB_0_13	Data Byte 12
0x53	R	MS_INF_PB_0_14	Data Byte 13

[1] As defined by the EIA/CEA-861D specifications.

The MPEG InfoFrame registers are considered valid if the following two conditions are met:

- MS_INFO_RAW is 1.
- MS_INF_CKS_ERR_RAW is 0. This condition applies only if ALWAYS_STORE_INF is set to 1.

MS_INFO_RAW, IO Map, Address 0x60[3] (Read Only)

Raw status signal of MPEG Source InfoFrame detection signal.

Function

MS_INFO_RAW	Description
0 (default)	No source product description InfoFrame received within the last three VSyncs or since the last HDMI packet detection reset.
1	MPEG Source InfoFrame received. This bit resets to 0 after an HDMI packet detection reset or upon writing to MS_PACKET_ID.

Vendor Specific InfoFrame Registers

Table 15 provides a list of readback registers available for the Vendor Specific InfoFrame.

Table 15. VS InfoFrame Registers

InfoFrame Map Address	R/W	Register Name	Byte Name
0xEC	R	VS_PACKET_ID[7:0]	Packet Type Value
0xED	R	VS_INF_VERS	InfoFrame version number
0xEE	R	VS_INF_LEN	InfoFrame length
0x54	R	VS_INF_PB_0_1	Checksum
0x55	R	VS_INF_PB_0_2	Data Byte 1
0x56	R	VS_INF_PB_0_3	Data Byte 2
0x57	R	VS_INF_PB_0_4	Data Byte 3
0x58	R	VS_INF_PB_0_5	Data Byte 4
0x59	R	VS_INF_PB_0_6	Data Byte 5
0x5A	R	VS_INF_PB_0_7	Data Byte 6
0x5B	R	VS_INF_PB_0_8	Data Byte 7
0x5C	R	VS_INF_PB_0_9	Data Byte 8
0x5D	R	VS_INF_PB_0_10	Data Byte 9
0x5E	R	VS_INF_PB_0_11	Data Byte 10
0x5F	R	VS_INF_PB_0_12	Data Byte 11
0x60	R	VS_INF_PB_0_13	Data Byte 12
0x61	R	VS_INF_PB_0_14	Data Byte 13
0x62	R	VS_INF_PB_0_15	Data Byte 14
0x63	R	VS_INF_PB_0_16	Data Byte 15
0x64	R	VS_INF_PB_0_17	Data Byte 16
0x65	R	VS_INF_PB_0_18	Data Byte 17
0x66	R	VS_INF_PB_0_19	Data Byte 18
0x67	R	VS_INF_PB_0_20	Data Byte 19
0x68	R	VS_INF_PB_0_21	Data Byte 20
0x69	R	VS_INF_PB_0_22	Data Byte 21
0x6A	R	VS_INF_PB_0_23	Data Byte 22
0x6B	R	VS_INF_PB_0_24	Data Byte 23
0x6C	R	VS_INF_PB_0_25	Data Byte 24
0x6D	R	VS_INF_PB_0_26	Data Byte 25
0x6E	R	VS_INF_PB_0_27	Data Byte 26
0x6F	R	VS_INF_PB_0_28	Data Byte 27

The Vendor Specific InfoFrame registers are considered valid if the following two conditions are met:

- VS_INFO_RAW is 1.
- VS_INF_CKS_ERR_RAW is 0. This condition applies only if ALWAYS_STORE_INF is set to 1.

VS_INFO_RAW, IO Map, Address 0x60[4] (Read Only)

Raw status signal of Vendor specific InfoFrame detection signal.

Function

VS_INFO_RAW	Description
0 (default)	No new VS InfoFrame has been received since the last HDMI packet detection reset.
1	A new VS InfoFrame has been received. This bit resets to zero after an HDMI packet detection reset or upon writing to VS_PACKET_ID.

PACKET REGISTERS

ACP Packet Registers

Table 16 provides the list of readback registers available for the ACP packets. Refer to the HDMI 1.4 specifications for a detailed explanation of the ACP packet fields.

Table 16. ACP Packet Registers

InfoFrame Map Address	R/W	Register Name	Packet Byte No.[1]
0xEF	R/W	ACP_PACKET_ID[7:0]	Packet Type Value
0xF0	R	ACP_TYPE	HB1
0xF1	R	ACP_HEADER2	HB2
0x70	R	ACP_PB_0_1	PB0
0x71	R	ACP_PB_0_2	PB1
0x72	R	ACP_PB_0_3	PB2
0x73	R	ACP_PB_0_4	PB3
0x74	R	ACP_PB_0_5	PB4
0x75	R	ACP_PB_0_6	PB5
0x76	R	ACP_PB_0_7	PB6
0x77	R	ACP_PB_0_8	PB7
0x78	R	ACP_PB_0_9	PB8
0x79	R	ACP_PB_0_10	PB9
0x7A	R	ACP_PB_0_11	PB10
0x7B	R	ACP_PB_0_12	PB11
0x7C	R	ACP_PB_0_13	PB12
0x7D	R	ACP_PB_0_14	PB13
0x7E	R	ACP_PB_0_15	PB14
0x7F	R	ACP_PB_0_16	PB15
0x80	R	ACP_PB_0_17	PB16
0x81	R	ACP_PB_0_18	PB17
0x82	R	ACP_PB_0_19	PB18
0x83	R	ACP_PB_0_20	PB19
0x84	R	ACP_PB_0_21	PB20
0x85	R	ACP_PB_0_22	PB21
0x86	R	ACP_PB_0_23	PB22
0x87	R	ACP_PB_0_24	PB23
0x88	R	ACP_PB_0_25	PB24
0x89	R	ACP_PB_0_26	PB25
0x8A	R	ACP_PB_0_27	PB26
0x8B	R	ACP_PB_0_28	PB27

[1] As defined by the HDMI 1.4 specifications.

The ACP InfoFrame registers are considered valid if ACP_PCKT_RAW is set to 1.

ACP_PCKT_RAW, IO Map, Address 0x60[5] (Read Only)

Raw status signal of audio content protection packet detection signal.

Function

ACP_PCKT_RAW	Description
0 (default)	No ACP packet received within the last 600 ms or since the last HDMI packet detection reset.
1	ACP packets have been received within the last 600 ms. This bit resets to 0 after an HDMI packet detection reset or upon writing to ACP_PACKET_ID.

ISRC Packet Registers

Table 17 and Table 18 provide lists of readback registers available for the ISRC packets. Refer to the HDMI 1.4 specifications for a detailed explanation of the ISRC packet fields.

Table 17. ISRC1 Packet Registers

InfoFrame Map Address	R/W	Register Name	Packet Byte No.[1]
0xF2	R/W	ISRC1_PACKET_ID[7:0]	Packet Type Value
0xF3	R	ISRC1_HEADER1	HB1
0xF4	R	ISRC1_HEADER2	HB2
0x8C	R	ISRC1_PB_0_1	PB0
0x8D	R	ISRC1_PB_0_2	PB1
0x8E	R	ISRC1_PB_0_3	PB2
0x8F	R	ISRC1_PB_0_4	PB3
0x90	R	ISRC1_PB_0_5	PB4
0x91	R	ISRC1_PB_0_6	PB5
0x92	R	ISRC1_PB_0_7	PB6
0x93	R	ISRC1_PB_0_8	PB7
0x94	R	ISRC1_PB_0_9	PB8
0x95	R	ISRC1_PB_0_10	PB9
0x96	R	ISRC1_PB_0_11	PB10
0x97	R	ISRC1_PB_0_12	PB11
0x98	R	ISRC1_PB_0_13	PB12
0x99	R	ISRC1_PB_0_14	PB13
0x9A	R	ISRC1_PB_0_15	PB14
0x9B	R	ISRC1_PB_0_16	PB15
0x9C	R	ISRC1_PB_0_17	PB16
0x9D	R	ISRC1_PB_0_18	PB17
0x9E	R	ISRC1_PB_0_19	PB18
0x9F	R	ISRC1_PB_0_20	PB19
0xA0	R	ISRC1_PB_0_21	PB20
0xA1	R	ISRC1_PB_0_22	PB21
0xA2	R	ISRC1_PB_0_23	PB22
0xA3	R	ISRC1_PB_0_24	PB23
0xA4	R	ISRC1_PB_0_25	PB24
0xA5	R	ISRC1_PB_0_26	PB25
0xA6	R	ISRC1_PB_0_27	PB26
0xA7	R	ISRC1_PB_0_28	PB27

[1] As defined by the HDMI 1.4 specifications.

The ISRC1 packet registers are considered valid if ISRC1_PCKT_RAW is set to 1.

ISRC1_PCKT_RAW, IO Map, Address 0x60[6] (Read Only)

Raw status signal of International Standard Recording Code 1 (ISRC1) Packet detection signal.

Function

ISRC1_PCKT_RAW	Description
0 (default)	No ISRC1 packets received since the last HDMI packet detection reset.
1	ISRC1 packets have been received. This bit resets to 0 after an HDMI packet detection reset or upon writing to ISRC1_PACKET_ID.

Table 18. ISRC2 Packet Registers

InfoFrame Map Address	R/W	Register Name	Packet Byte No.[1]
0xF5	R/W	ISRC2_PACKET_ID[7:0]	Packet Type Value
0xF6	R	ISRC2_HEADER1	HB1
0xF7	R	ISRC2_HEADER2	HB2
0xA8	R	ISRC2_PB_0_1	PB0
0xA9	R	ISRC2_PB_0_2	PB1
0xAA	R	ISRC2_PB_0_3	PB2
0xAB	R	ISRC2_PB_0_4	PB3
0xAC	R	ISRC2_PB_0_5	PB4
0xAD	R	ISRC2_PB_0_6	PB5
0xAE	R	ISRC2_PB_0_7	PB6
0xAF	R	ISRC2_PB_0_8	PB7
0xB0	R	ISRC2_PB_0_9	PB8
0xB1	R	ISRC2_PB_0_10	PB9
0xB2	R	ISRC2_PB_0_11	PB10
0xB3	R	ISRC2_PB_0_12	PB11
0xB4	R	ISRC2_PB_0_13	PB12
0xB5	R	ISRC2_PB_0_14	PB13
0xB6	R	ISRC2_PB_0_15	PB14
0xB7	R	ISRC2_PB_0_16	PB15
0xB8	R	ISRC2_PB_0_17	PB16
0xB9	R	ISRC2_PB_0_18	PB17
0xBA	R	ISRC2_PB_0_19	PB18
0xBB	R	ISRC2_PB_0_20	PB19
0xBC	R	ISRC2_PB_0_21	PB20
0xBD	R	ISRC2_PB_0_22	PB21
0xBE	R	ISRC2_PB_0_23	PB22
0xBF	R	ISRC2_PB_0_24	PB23
0xC0	R	ISRC2_PB_0_25	PB24
0xC1	R	ISRC2_PB_0_26	PB25
0xC2	R	ISRC2_PB_0_27	PB26
0xC3	R	ISRC2_PB_0_28	PB27

[1] As defined by the HDMI 1.4 specifications.

The ISRC2 packet registers are considered valid if, and only if, ISRC2_PCKT_RAW is set to 1.

ISRC2_PCKT_RAW, IO Map, Address 0x60[7] (Read Only)

Raw status signal of International Standard Recording Code 2 (ISRC2) Packet detection signal.

Function

ISRC2_PCKT_RAW	Description
0 (default)	No ISRC2 packets received since the last HDMI packet detection reset.
1	ISRC2 packets have been received. This bit resets to 0 after an HDMI packet detection reset or upon writing to ISRC2_PACKET_ID.

Gamut Metadata Packets

Refer to the HDMI 1.4 specifications for a detailed explanation of the Gamut Metadata packet fields.

Table 19. Gamut Metadata Packet Registers

HDMI Map Address	R/W	Register Name	Packet Byte No.[1]
0xF8	R/W	GAMUT_PACKET_ID[7:0]	Packet Type Value
0xF9	R	GAMUT_HEADER1	HB1
0xFA	R	GAMUT_HEADER2	HB2
0xC4	R	GAMUT_MDATA_PB_0_1	PB0
0xC5	R	GAMUT_MDATA_PB_0_2	PB1
0xC6	R	GAMUT_MDATA_PB_0_3	PB2
0xC7	R	GAMUT_MDATA_PB_0_4	PB3
0xC8	R	GAMUT_MDATA_PB_0_5	PB4
0xC9	R	GAMUT_MDATA_PB_0_6	PB5
0xCA	R	GAMUT_MDATA_PB_0_7	PB6
0xCB	R	GAMUT_MDATA_PB_0_8	PB7
0xCC	R	GAMUT_MDATA_PB_0_9	PB8
0xCD	R	GAMUT_MDATA_PB_0_10	PB9
0xCE	R	GAMUT_MDATA_PB_0_11	PB10
0xCF	R	GAMUT_MDATA_PB_0_12	PB11
0xD0	R	GAMUT_MDATA_PB_0_13	PB12
0xD1	R	GAMUT_MDATA_PB_0_14	PB13
0xD2	R	GAMUT_MDATA_PB_0_15	PB14
0xD3	R	GAMUT_MDATA_PB_0_16	PB15
0xD4	R	GAMUT_MDATA_PB_0_17	PB16
0xD5	R	GAMUT_MDATA_PB_0_18	PB17
0xD6	R	GAMUT_MDATA_PB_0_19	PB18
0xD7	R	GAMUT_MDATA_PB_0_20	PB19
0xD8	R	GAMUT_MDATA_PB_0_21	PB20
0xD9	R	GAMUT_MDATA_PB_0_22	PB21
0xDA	R	GAMUT_MDATA_PB_0_23	PB22
0xDB	R	GAMUT_MDATA_PB_0_24	PB23
0xDC	R	GAMUT_MDATA_PB_0_25	PB24
0xDD	R	GAMUT_MDATA_PB_0_26	PB25
0xDE	R	GAMUT_MDATA_PB_0_27	PB26
0xDF	R	GAMUT_MDATA_PB_0_28	PB27

[1] As defined by the HDMI 1.4 specifications.

The Gamut Metadata packet registers are considered valid if GAMUT_MDATA_RAW is set to 1.

GAMUT_MDATA_RAW, IO Map, Address 0x65[0] (Read Only)

Raw status signal of Gamut Metadata Packet detection signal.

Function

GAMUT_MDATA_RAW	Description
0 (default)	No Gamut Metadata packet has been received in the last video frame or since the last HDMI packet detection reset.
1	A Gamut Metadata packet has been received in the last video frame. This bit resets to 0 after an HDMI packet detection reset or upon writing to GAMUT_PACKET_ID.

GAMUT_IRQ_NEXT_FIELD, HDMI Map, Address 0x50[4]

A control set the NEW_GAMUT_MDATA_RAW interrupt to detect when the new contents are applicable to next field or to indicate that the Gamut packet is new. This is done using header information of the gamut packet.

Function

GAMUT_IRQ_NEXT_FIELD	Description
0 (default)	Interrupt flag indicates that Gamut packet is new
1	Interrupt flag indicates that Gamut packet is to be applied next field

CUSTOMIZING PACKET/INFOFRAME STORAGE REGISTERS

The packet type value of each set of packet and InfoFrame registers in the InfoFrame map is programmable. This allows the user to configure the ADV7630 to store the payload data of any packet and InfoFrames sent by the transmitter connected on the selected HDMI port.

Note: Writing to any of the nine following packet ID registers also clears the corresponding raw InfoFrame /packet detection bit. For example, writing 0x82 (or any other value) to AVI_PACKET_ID[7:0] clears AVI_INFO_RAW.

AVI_PACKET_ID[7:0], InfoFrame, Address 0xE0[7:0]

AVI InfoFrame packet type value.

Function

AVI_PACKET_ID[7:0]	Description
0xxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x00 to 0x1B
1xxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x00 to 0x1B

AUD_PACKET_ID[7:0], InfoFrame, Address 0xE3[7:0]

Audio InfoFrame packet type value.

Function

AUD_PACKET_ID[7:0]	Description
xxxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x1C to 0x29

SPD_PACKET_ID[7:0], InfoFrame, Address 0xE6[7:0]

Source Product Descriptor InfoFrame packet type value.

Function

SPD_PACKET_ID[7:0]	Description
xxxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x2A to 0x45

MS_PACKET_ID[7:0], InfoFrame, Address 0xE9[7:0]

MPEG Source InfoFrame ID packet type value.

Function

MS_PACKET_ID[7:0]	Description
xxxxxxxx	Packet type value of InfoFrame stored in InfoFrame map, Address 0x46 to 0x53

VS_PACKET_ID[7:0], InfoFrame, Address 0xEC[7:0]

Vendor Specific InfoFrame ID packet type value.

Function

VS_PACKET_ID[7:0]	Description
xxxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x54 to 0x6F

ACP_PACKET_ID[7:0], InfoFrame, Address 0xEF[7:0]

ACP Packet ID packet type value.

Function

ACP_PACKET_ID[7:0]	Description
xxxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x70 to 0x8B

ISRC1_PACKET_ID[7:0], InfoFrame, Address 0xF2[7:0]

ISRC1 Packet ID packet type value.

Function

ISRC1_PACKET_ID[7:0]	Description
xxxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0x8C to 0xA7

ISRC2_PACKET_ID[7:0], InfoFrame, Address 0xF5[7:0]

ISRC2 Packet ID packet type value.

Function

ISRC2_PACKET_ID[7:0]	Description
xxxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0xA8 to 0xC3

GAMUT_PACKET_ID[7:0], InfoFrame, Address 0xF8[7:0]

Gamut Metadata Packet ID packet type value.

Function

GAMUT_PACKET_ID[7:0]	Description
xxxxxxxx	Packet type value of packet stored in InfoFrame map, Address 0xC4 to 0xDF

Note: The packet type values and corresponding packets should not be programmed in the packet type values registers. The following packets are always processed internally and cannot be stored in the packet/InfoFrame registers in the InfoFrame map:

- 0x01: Audio Clock Regeneration Packet
- 0x02: Audio Sample Packet
- 0x03: General Control Packet
- 0x07: DSD Audio Sample Packet
- 0x08: DST Audio Packet
- 0x09: HBR Audio Stream Packet

REPEATER SUPPORT

The ADV7630 incorporates a E-EDID/repeater controller that provides all the features required for a receiver front end of a fully HDCP 1.4 compliant repeater system. The ADV7630 has a RAM that can store up to 127 KSVs, which allows it to handle up to 127 downstream devices in repeater mode (refer to Table 20).

The ADV7630 features a set of HDCP registers, defined in the HDCP specifications, which are accessible through the DDC bus of the selected port (refer to the HDMI Receiver DDC Ports section). A subset of the HDCP registers (defined in the following subsections) are also available in the repeater map and are accessible through the main I^2C port (refer to the Main I2C Port section).

Repeater Routines Performed by Repeater Controller

Power-Up

A power-on RESET circuitry on the DVDD supply is used to reset the repeater controller when the ADV7630 is powered up. When the E-EDID/repeater controller reboots after reset, it resets all the KSV registers listed in Table 20 to 0x00 for all maps.

AKSV Update

The repeater controller automatically resets BCAPS[5] to 0 when an HDCP transmitter writes its AKSV into the ADV7630 HDCP registers through the DDC bus of the selected HDMI port.

Note: Writing a value in AKSV[39:32] triggers an AKSV update and an AKSV_UPDATE_ST interrupt if AKSV_UPDATE_MB1 or AKSV_UPDATE_MB2 is set to 1 This triggers the repeater controller to reset the BCAPS[5] bit back to 0.

KSV List Ready

The KSV_LIST_READY bit is set by an external controller driving the ADV7630. This notifies the ADV7630 on-chip repeater controller that the KSV list registers were updated with the KSVs of the attached and active downstream HDCP devices.

When KSV_LIST_READY is set to 1, the repeater controller computes the SHA-1 hash value V', updates the corresponding V' registers (refer to Table 21), and sets the READY bit (that is, Bit 5 of BCAPS[7:0]) to 1. This indicates to the transmitter attached to the ADV7630 that the KSV FIFO and SHA-1 hash value V' are ready to be read.

KSV_LIST_READY, Repeater Map, Address 0x71[7]

The system sets this bit in order to indicate that the KSV list has been read from the Tx IC(s) and written into the repeater map. The system must also set bits [11:0] of Bstatus before setting this bit.

Function

KSV_LIST_READY	Description
0 (default)	KSV list not ready
1	KSV list ready

Notes:

- The SHA-1 hash value is computed if the KSV_LIST_READY bit is set after the part has received an AKSV update from the upstream source. The external controller should, therefore, set KSV_LIST_READY to 1 only after the part has received an AKSV update from the upstream source.
- The ADV7630 does not automatically clear KSV_LIST_READY to 0, after it has finished computing the SHA-1 hash value. Therefore, the external controller needs to clear KSV_LIST_READY.

HDMI Mode

The BSTATUS[15:0] bit is updated automatically by the ADV7630 and follows the HDMI mode status of the HDMI/DVI stream input on the active HDMI port. BSTATUS[15:0] is set to 1 if the ADV7630 receives an HDMI stream, and set to 0 if the ADV7630 receives a DVI stream.

HDMI_MODE, HDMI, Address 0x05[7] (Read Only)

A readback to indicate if the stream processed by the HDMI core is a DVI or an HDMI stream. This register refers to a primary HDMI port selected.

Function

HDMI_MODE	Description
0	DVI mode detected
1	HDMI mode detected

BG_HDMI_MODE, HDMI Map, Address 0xEB[0] (Read Only)

This readback provides the HDMI/DVI mode status of the background port determined by BG_MEAS_PORT_SEL[1:0] and is updated continuously.

Function

BG_HDMI_MODE	Description
0	DVI mode detected on selected BG port
1	HDMI mode detected on selected BG port

Repeater Actions Required by External Controller

The external controller must set the BCAPS register and notify the ADV7630 when the KSV list is updated, as described in the Repeater Bit, KSV FIFO Read from HDCP Registers, First AKSV Update, and Second and Subsequent AKSV Updates sections.

Note: Many more routines must be implemented into the external controller driving the ADV7630 to implement a full repeater. Such routines are described in the HDCP and HDMI specifications (for example, copying InfoFrame and packet data images from the HDMI receiver into the HDMI transmitter, disabling the clock termination on a change of downstream topology, and so on).

Repeater Bit

The repeater bit (that is, Bit 6 of BCAPS[7:0]) must be set to 1 by the external controller in the routine that initializes the ADV7630. The repeater bit must be left as such as long as the ADV7630 is configured as the front end of a repeater system.

Note: The registers in the KSV list (refer to Table 20) should always be set to 0x0 if the repeater bit is set to 0. The firmware running on the external controller, therefore, always sets the registers in the KSV list to 0x0 if the repeater bit is changed from 1 to 0.

KSV FIFO Read from HDCP Registers

The KSV FIFO read at address 0x43 through the HDCP port of the selected HDMI port is dependent on the value of the repeater bit (that is, Bit 6 of BCAPS[7:0]):

- When the repeater bit is set to 0, the KSV FIFO read from the HDCP port always returns 0x0
- When the repeater bit is set to 1, the KSV FIFO read from the HDCP port matches the KSV list which is set in the repeater map at Address 0x80 to Address 0xF7 (refer to Table 20)

First AKSV Update

When the upstream transmitter writes its AKSV for the first time into the ADV7630 HDCP registers, the external controller driving the ADV7630 should perform the following tasks:

- Update BSTATUS[15:0] according to the topology of the downstream device attached to the repeater.
- Update the KSV list (refer to Table 20) with the KSV from the transmitter on the back end of the repeater as well as the KSV from all the downstream devices connected to the repeater.
- Set KSV_LIST_READY to 1.
- The external controller can monitor the AKSV_UPDATE_X_RAW bits (where X = A, B, C or D) to be notified when the transmitter writes its AKSV into the HDCP registers of the ADV7630.

AKSV_UPDATE_A_RAW, IO Map, Address 0x88[3] (Read Only)

Status of Port A AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port A. Once set, this bit remains high until it is cleared via AKSV_UPDATE_A_CLR.

Function

AKSV_UPDATE_A_RAW	Description
0	No AKSV updates on Port A
1	Detected a write access to the AKSV register on Port A

AKSV_UPDATE_B_RAW, IO Map, Address 0x88[2] (Read Only)

Status of Port B AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port B. Once set, this bit remains high until it is cleared via AKSV_UPDATE_B_CLR.

Function

AKSV_UPDATE_B_RAW	Description
0	No AKSV updates on Port B
1	Detected a write access to the AKSV register on Port B

AKSV_UPDATE_C_RAW, IO Map, Address 0x88[1] (Read Only)

Status of Port C AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port C. Once set, this bit remains high until it is cleared via AKSV_UPDATE_C_CLR.

Function

AKSV_UPDATE_C_RAW	Description
0	No AKSV updates on Port C
1	Detected a write access to the AKSV register on Port C

AKSV_UPDATE_D_RAW, IO Map, Address 0x88[0] (Read Only)

Status of Port D AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port D. Once set, this bit remains high until it is cleared via AKSV_UPDATE_D_CLR.

Function

AKSV_UPDATE_D_RAW	Description
0	No AKSV updates on Port D
1	Detected a write access to the AKSV register on Port D

Second and Subsequent AKSV Updates

When the upstream transmitter writes its AKSV for the second time or more into the ADV7630 HDCP registers, the external controller driving the ADV7630 should set KSV_LIST_READY to 1.

HDCP Registers Available in Repeater Map

In order to enable fast switching of the HDCP encrypted HDMI ports, the registers 0x00 to 0x42 in the Repeater Map are replicated for each port. AUTO_HDCP_MAP_ENABLE and HDCP_MAP_SELECT[2:0] determine which port is currently visible to the user.

AUTO_HDCP_MAP_ENABLE, Repeater Map, Address 0x79[3]

Selects which port is accessed for HDCP addresses: the HDMI active port (selected by HDMI_PORT_SELECT, HDMI Map) or the one selected in HDCP_MAP_SELECT.

Function

AUTO_HDCP_MAP_ENABLE	Description
0	HDCP data read from port given by HDCP_MAP_SELECT
1 (Default)	HDCP data read from the active HDMI port

HDCP_MAP_SELECT[2:0], Repeater Map, Address 0x79[2:0]

Selects which port is accessed for HDCP addresses (Address 0x00 to Address 0x42 in repeater map). This takes effect only when AUTO_HDCP_MAN_ENABLE is 0.

Function

HDCP_MAP_SELECT[2:0]	Description
000 (Default)	Select Port A
001	Select Port B
010	Select Port C
011	Select Port D

BKSV[39:0], Repeater Map, Address 0x04[7:0]; Address 0x03[7:0]; Address 0x02[7:0]; Address 0x01[7:0]; Address 0x00[7:0] (Read Only)

The HDMI receiver Key Selection Vector (BKSV) can be read back once the part has successfully accessed the HDCP ROM. The following registers contain the BKSV read from the EEPROM: 0x00[7:0] = BKSV[7:0], 0x01[7:0] = BKSV[15:8], 0x02[7:0] = BKSV[23:16], 0x03[7:0] = BKSV[31:24] and 0x04[7:0] = BKSV[39:32].

Function

BKSV[39:0]	Description
0x00	BKSV[7:0]
0x01	BKSV[15:8]
0x02	BKSV[23:16]
0x03	BKSV[31:24]
0x04	BKSV[39:32]

AKSV[39:0], Repeater Map, Address 0x14[7:0]; Address 0x13[7:0]; Address 0x12[7:0]; Address 0x11[7:0]; Address 0x10[7:0]

The AKSV of the transmitter attached to the active HDMI port can be read back after an AKSV update. The following registers contain the AKSV written by the Tx: 0x10[7:0] = AKSV[7:0], 0x11[7:0] = AKSV[15:8], 0x12[7:0] = AKSV[23:16], 0x13[7:0] = AKSV[31:24] and 0x14[7:0] = AKSV[39:32]. Default value for this register is 0.

Function

AKSV[39:0]	Description
0x10	AKSV[7:0]
0x11	AKSV[15:8]
0x12	AKSV[23:16]
0x13	AKSV[31:24]
0x14	AKSV[39:32]

BCAPS[7:0], Repeater Map, Address 0x40[7:0]

This is the BCAPS register that is presented to the Tx attached to the active HDMI port.

Function

BCAPS[7:0]	Description
10000011 (Default)	Default BCAPS register value presented to Tx
xxxxxxxx	BCAPS register value presented to Tx

BSTATUS[15:0], Repeater Map, Address 0x42[7:0]; Address 0x41[7:0]

These registers contain the BSTATUS information presented to the Tx attached to the active HDMI port. Bits [11:0] must be set by the system software acting as a repeater. 0x41[7:0] = BSTATUS[7:0], 0x42[7:0] = BSTATUS[15:8]

Function

BSTATUS[15:0]	Description
xxxxxxxxxxxxxxxx	BSTATUS register presented to Tx
0000000000000000 (Default)	Reset value. BSTATUS register is reset only after power-up.

KSV registers are stored consecutively in RAM, which is split into maps of 5 × 128 bytes. Each map can be accessed through KSV_BYTE_0…KSV_BYTE_127. The proper segment can be selected via the KSV_MAP_SELECT[2:0] register (see Figure 13).

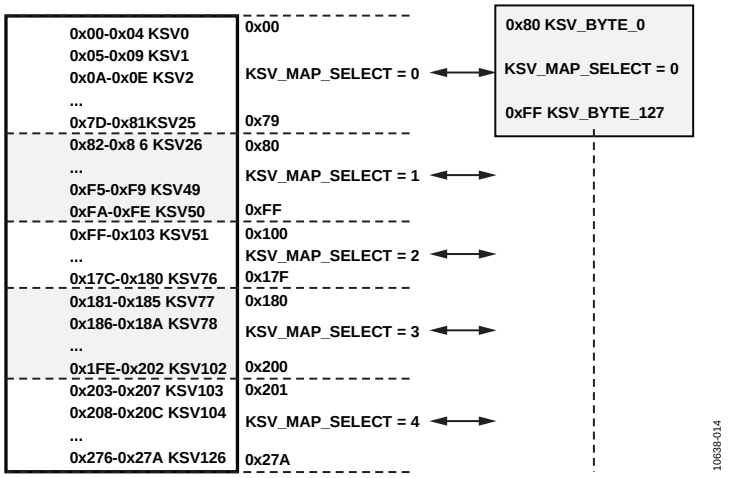


Figure 13. Addressing by Using KSV_MAP_SELECT and Register KSV_BYTE_0 to Register KSV_BYTE_127

KSV_MAP_SELECT[2:0], Repeater Map, Address 0x79[6:4]

Selects which 128 bytes of KSV list are accessed when reading or writing to Address 0x80 to Address 0xFF in this map. Values from 5 and upwards are not valid.

Table 20. KSV Byte Registers Location

KSV Byte Number	Register Name	Register Address
0	KSV_BYTE_0[7:0]	0x80[7:0]
1	KSV_BYTE_1[7:0]	0x81[7:0]
2	KSV_BYTE_2[7:0]	0x82[7:0]
3	KSV_BYTE_3[7:0]	0x83[7:0]
4	KSV_BYTE_4[7:0]	0x84[7:0]
5	KSV_BYTE_5[7:0]	0x85[7:0]
6	KSV_BYTE_6[7:0]	0x86[7:0]
7	KSV_BYTE_7[7:0]	0x87[7:0]
8	KSV_BYTE_8[7:0]	0x88[7:0]
9	KSV_BYTE_9[7:0]	0x89[7:0]
10	KSV_BYTE_10[7:0]	0x8A[7:0]
11	KSV_BYTE_11[7:0]	0x8B[7:0]
12	KSV_BYTE_12[7:0]	0x8C[7:0]
13	KSV_BYTE_13[7:0]	0x8D[7:0]
14	KSV_BYTE_14[7:0]	0x8E[7:0]
15	KSV_BYTE_15[7:0]	0x8F[7:0]
16	KSV_BYTE_16[7:0]	0x90[7:0]
17	KSV_BYTE_17[7:0]	0x91[7:0]
18	KSV_BYTE_18[7:0]	0x92[7:0]
19	KSV_BYTE_19[7:0]	0x93[7:0]
20	KSV_BYTE_20[7:0]	0x94[7:0]
21	KSV_BYTE_21[7:0]	0x95[7:0]
22	KSV_BYTE_22[7:0]	0x96[7:0]
23	KSV_BYTE_23[7:0]	0x97[7:0]
24	KSV_BYTE_24[7:0]	0x98[7:0]
25	KSV_BYTE_25[7:0]	0x99[7:0]
26	KSV_BYTE_26[7:0]	0x9A[7:0]
27	KSV_BYTE_27[7:0]	0x9B[7:0]
28	KSV_BYTE_28[7:0]	0x9C[7:0]
29	KSV_BYTE_29[7:0]	0x9D[7:0]
30	KSV_BYTE_30[7:0]	0x9E[7:0]
31	KSV_BYTE_31[7:0]	0x9F[7:0]
32	KSV_BYTE_32[7:0]	0xA0[7:0]
33	KSV_BYTE_33[7:0]	0xA1[7:0]
34	KSV_BYTE_34[7:0]	0xA2[7:0]
35	KSV_BYTE_35[7:0]	0xA3[7:0]

KSV Byte Number	Register Name	Register Address
36	KSV_BYTE_36[7:0]	0xA4[7:0]
37	KSV_BYTE_37[7:0]	0xA5[7:0]
38	KSV_BYTE_38[7:0]	0xA6[7:0]
39	KSV_BYTE_39[7:0]	0xA7[7:0]
40	KSV_BYTE_40[7:0]	0xA8[7:0]
41	KSV_BYTE_41[7:0]	0xA9[7:0]
42	KSV_BYTE_42[7:0]	0xAA[7:0]
43	KSV_BYTE_43[7:0]	0xAB[7:0]
44	KSV_BYTE_44[7:0]	0xAC[7:0]
45	KSV_BYTE_45[7:0]	0xAD[7:0]
46	KSV_BYTE_46[7:0]	0xAE[7:0]
47	KSV_BYTE_47[7:0]	0xAF[7:0]
48	KSV_BYTE_48[7:0]	0xB0[7:0]
49	KSV_BYTE_49[7:0]	0xB1[7:0]
50	KSV_BYTE_50[7:0]	0xB2[7:0]
51	KSV_BYTE_51[7:0]	0xB3[7:0]
52	KSV_BYTE_52[7:0]	0xB4[7:0]
53	KSV_BYTE_53[7:0]	0xB5[7:0]
54	KSV_BYTE_54[7:0]	0xB6[7:0]
55	KSV_BYTE_55[7:0]	0xB7[7:0]
56	KSV_BYTE_56[7:0]	0xB8[7:0]
57	KSV_BYTE_57[7:0]	0xB9[7:0]
58	KSV_BYTE_58[7:0]	0xBA[7:0]
59	KSV_BYTE_59[7:0]	0xBB[7:0]
60	KSV_BYTE_60[7:0]	0xBC[7:0]
61	KSV_BYTE_61[7:0]	0xBD[7:0]
62	KSV_BYTE_62[7:0]	0xBE[7:0]
63	KSV_BYTE_63[7:0]	0xBF[7:0]
64	KSV_BYTE_64[7:0]	0xC0[7:0]
65	KSV_BYTE_65[7:0]	0xC1[7:0]
66	KSV_BYTE_66[7:0]	0xC2[7:0]
67	KSV_BYTE_67[7:0]	0xC3[7:0]
68	KSV_BYTE_68[7:0]	0xC4[7:0]
69	KSV_BYTE_69[7:0]	0xC5[7:0]
70	KSV_BYTE_70[7:0]	0xC6[7:0]
71	KSV_BYTE_71[7:0]	0xC7[7:0]
72	KSV_BYTE_72[7:0]	0xC8[7:0]
73	KSV_BYTE_73[7:0]	0xC9[7:0]
74	KSV_BYTE_74[7:0]	0xCA[7:0]
75	KSV_BYTE_75[7:0]	0xCB[7:0]
76	KSV_BYTE_76[7:0]	0xCC[7:0]
77	KSV_BYTE_77[7:0]	0xCD[7:0]
78	KSV_BYTE_78[7:0]	0xCE[7:0]
79	KSV_BYTE_79[7:0]	0xCF[7:0]
80	KSV_BYTE_80[7:0]	0xD0[7:0]
81	KSV_BYTE_81[7:0]	0xD1[7:0]
82	KSV_BYTE_82[7:0]	0xD2[7:0]
83	KSV_BYTE_83[7:0]	0xD3[7:0]
84	KSV_BYTE_84[7:0]	0xD4[7:0]
85	KSV_BYTE_85[7:0]	0xD5[7:0]
86	KSV_BYTE_86[7:0]	0xD6[7:0]
87	KSV_BYTE_87[7:0]	0xD7[7:0]
88	KSV_BYTE_88[7:0]	0xD8[7:0]
89	KSV_BYTE_89[7:0]	0xD9[7:0]
90	KSV_BYTE_90[7:0]	0xDA[7:0]
91	KSV_BYTE_91[7:0]	0xDB[7:0]
92	KSV_BYTE_92[7:0]	0xDC[7:0]
93	KSV_BYTE_93[7:0]	0xDD[7:0]
94	KSV_BYTE_94[7:0]	0xDE[7:0]
95	KSV_BYTE_95[7:0]	0xDF[7:0]
96	KSV_BYTE_96[7:0]	0xE0[7:0]
97	KSV_BYTE_97[7:0]	0xE1[7:0]
98	KSV_BYTE_98[7:0]	0xE2[7:0]
99	KSV_BYTE_99[7:0]	0xE3[7:0]

KSV Byte Number	Register Name	Register Address
100	KSV_BYTE_100[7:0]	0xE4[7:0]
101	KSV_BYTE_101[7:0]	0xE5[7:0]
102	KSV_BYTE_102[7:0]	0xE6[7:0]
103	KSV_BYTE_103[7:0]	0xE7[7:0]
104	KSV_BYTE_104[7:0]	0xE8[7:0]
105	KSV_BYTE_105[7:0]	0xE9[7:0]
106	KSV_BYTE_106[7:0]	0xEA[7:0]
107	KSV_BYTE_107[7:0]	0xEB[7:0]
108	KSV_BYTE_108[7:0]	0xEC[7:0]
109	KSV_BYTE_109[7:0]	0xED[7:0]
110	KSV_BYTE_110[7:0]	0xEE[7:0]
111	KSV_BYTE_111[7:0]	0xEF[7:0]
112	KSV_BYTE_112[7:0]	0xF0[7:0]
113	KSV_BYTE_113[7:0]	0xF1[7:0]
114	KSV_BYTE_114[7:0]	0xF2[7:0]
115	KSV_BYTE_115[7:0]	0xF3[7:0]
116	KSV_BYTE_116[7:0]	0xF4[7:0]
117	KSV_BYTE_117[7:0]	0xF5[7:0]
118	KSV_BYTE_118[7:0]	0xF6[7:0]
119	KSV_BYTE_119[7:0]	0xF7[7:0]
120	KSV_BYTE_120[7:0]	0xF8[7:0]
121	KSV_BYTE_121[7:0]	0xF9[7:0]
122	KSV_BYTE_122[7:0]	0xFA[7:0]
123	KSV_BYTE_123[7:0]	0xFB[7:0]
124	KSV_BYTE_124[7:0]	0xFC[7:0]
125	KSV_BYTE_125[7:0]	0xFD[7:0]
126	KSV_BYTE_126[7:0]	0xFE[7:0]
127	KSV_BYTE_127[7:0]	0xFF[7:0]

Table 21. Registers Location for SHA-1 Hash Value V'

Register Name	Address Location[1]	Function[2]
SHA_A[31:0]	0x20[7:0]: SHA_A[7:0] 0x21[7:0]: SHA_A[15:8] 0x22[7:0]: SHA_A[23:16] 0x23[7:0]: SHA_A[31:24]	H0 part of SHA-1 hash value V'. Register also called (V'.H1).
SHA_B[31:0]	0x24[7:0]: SHA_B[7:0] 0x25[7:0]: SHA_B[15:8] 0x26[7:0]: SHA_B[23:16] 0x27[7:0]: SHA_B[31:24]	H1 part of SHA-1 hash value V'. Register also called (V'.H1).
SHA_C[31:0]	0x28[7:0]: SHA_C[7:0] 0x29[7:0]: SHA_C[15:8] 0x2A[7:0]: SHA_C[23:16] 0x2B[7:0]: SHA_C[31:24]	H2 part of SHA-1 hash value V'. Register also called (V'.H2).
SHA_D[31:0]	0x2C[7:0]: SHA_D[7:0] 0x2D[7:0]: SHA_D[15:8] 0x2E[7:0]: SHA_D[23:16] 0x2F[7:0]: SHA_D[31:24]	H3 part of SHA-1 hash value V'. Register also called (V'.H3).
SHA_E[31:0]	0x30[7:0]: SHA_E[7:0] 0x31[7:0]: SHA_E[15:8] 0x32[7:0]: SHA_E[23:16] 0x33[7:0]: SHA_E[31:24]	H4 part of SHA-1 hash value V'. Register also called (V'.H4).

[1] All registers specified in Table 21 are located in the repeater map.
[2] Refer to HDCP Protection System Standards.

COLOR SPACE INFORMATION

Color space information is available via the HDMI_COLORSPACE[3:0] register.

HDMI_COLORSPACE[3:0], HDMI, Address 0x53[3:0] (Read Only)

A readback of the HDMI input color space decoded from the AVI InfoFrame. This register refers to a primary HDMI port selected.

Function

HDMI_COLORSPACE[3:0]	Description
0000	RGB_LIMITED
0001	RGB_FULL
0010	YUV_601
0011	YUV_709
0100	XVYCC_601
0101	XVYCC_709
0110	YUV_601_FULL
0111	YUV_709_FULL
1000	sYCC 601
1001	Adobe YCC 601
1010	Adobe RGB

STATUS REGISTERS

Many status bit are available throughout the IO map and HDMI map. These status bits are listed in Table 22, Table 23, and Table 24.

Table 22. HDMI Flags in IO Map Register 0x6A

Bit Name	Bit Position	Description
TMDS_CLK_D_RAW	0 (LSB)	Description available on Page 37
TMDS_CLK_C_RAW	1	Description available on Page 37
TMDS_CLK_B_RAW	2	Description available on Page 37
TMDS_CLK_A_RAW	3	Description available on Page 37
TMDSPLL_LCK_D_RAW	4	Description available on Page 40
TMDSPLL_LCK_C_RAW	5	Description available on Page 40
TMDSPLL_LCK_B_RAW	6	Description available on Page 39
TMDSPLL_LCK_A_RAW	7 (MSB)	Description available on Page 39

Table 23. HDMI Flags in IO Map Register 0x6F

Bit Name	Bit Position	Description
CABLE_DET_D_RAW	0 (MSB)	Description available on Page 22
CABLE_DET_C_RAW	1	Description available on Page 21
CABLE_DET_B_RAW	2	Description available on Page 21
CABLE_DET_A_RAW	3	Description available on Page 21
HDMI_ENCRPT_D_RAW	4	Description available on Page 43
HDMI_ENCRPT_C_RAW	5	Description available on Page 43
HDMI_ENCRPT_B_RAW	6	Description available on Page 42
HDMI_ENCRPT_A_RAW	7 (MSB)	Description available on Page 42

Table 24. AKSV Update Flags in IO Map Register 0x88

Bit Name	Bit Position	Description
AKSV_UPDATE_D_RAW	0 (LSB)	When set to 1, it indicates that transmitter has written its AKSV into HDCP registers for Port D. Once set, this bit remains high until the interrupt is cleared via AKSV_UPDATE_D_CLR (IO Map 0x8A[0])
AKSV_UPDATE_C_RAW	1	When set to 1, it indicates that transmitter has written its AKSV into HDCP registers for Port C. Once set, this bit remains high until the interrupt is cleared via AKSV_UPDATE_C_CLR (IO Map 0x8A[1])
AKSV_UPDATE_B_RAW	2	When set to 1, it indicates that transmitter has written its AKSV into HDCP registers for Port B. Once set, this bit remains high until the interrupt is cleared via AKSV_UPDATE_B_CLR (IO Map 0x8A[2])
AKSV_UPDATE_A_RAW	3	When set to 1, it indicates that transmitter has written its AKSV into HDCP registers for Port A. Once set, this bit remains high until the interrupt is cleared via AKSV_UPDATE_A_CLR (IO Map 0x8A[3])

HDMI SECTION RESET STRATEGY

The reset strategy implemented for the HDMI section is as follows:

- **Global Chip Reset**
  A global chip reset is triggered by asserting the $\overline{\text{RESET}}$ pin to a low level. The HDMI section, excluding the repeater controller, is reset when a global reset is triggered.
- **Loss of TMDS Clock or 5 V Signal Reset**
  A loss of TMDS clock or 5 V signal on the HDMI port selected resets the HDMI section except for the EDID/repeater controller and the audio section. The loss of a 5 V signal condition is discarded if DIS_CABLE_DET_RST is set high. Authenticated background port is not affected.
- **DVI Mode Reset**
  The packet processing block, including InfoFrame memory, is held in reset when the HDMI section processes a DVI stream.
- **E-EDID/Repeater Controller Reset**
  The EDID/repeater controller is reset when its supply is low or when HDCP_REPT_EDID_RESET is set high. The E-EDID/repeater controller can be powered either from DVDD or from an HDMI cable. Refer to the +5 V Supply section.

HDMI PACKET DETECTION FLAG RESET

A packet detection flag reset is triggered when any of the following events occurs:

- ADV7630 is powered up.
- ADV7630 is reset.
- TMDS clock is detected, after a period of no clock activity, on the selected HDMI port
- Selected HDMI port is changed.
- Signal from the 5 V input pin of the HDMI port selected through HDMI_PORT_SELECT_TX_A[2:0] transitions to a high; this condition is discarded if DIS_CABLE_DET_RST is set high.

HDMI TRANSMITTERS

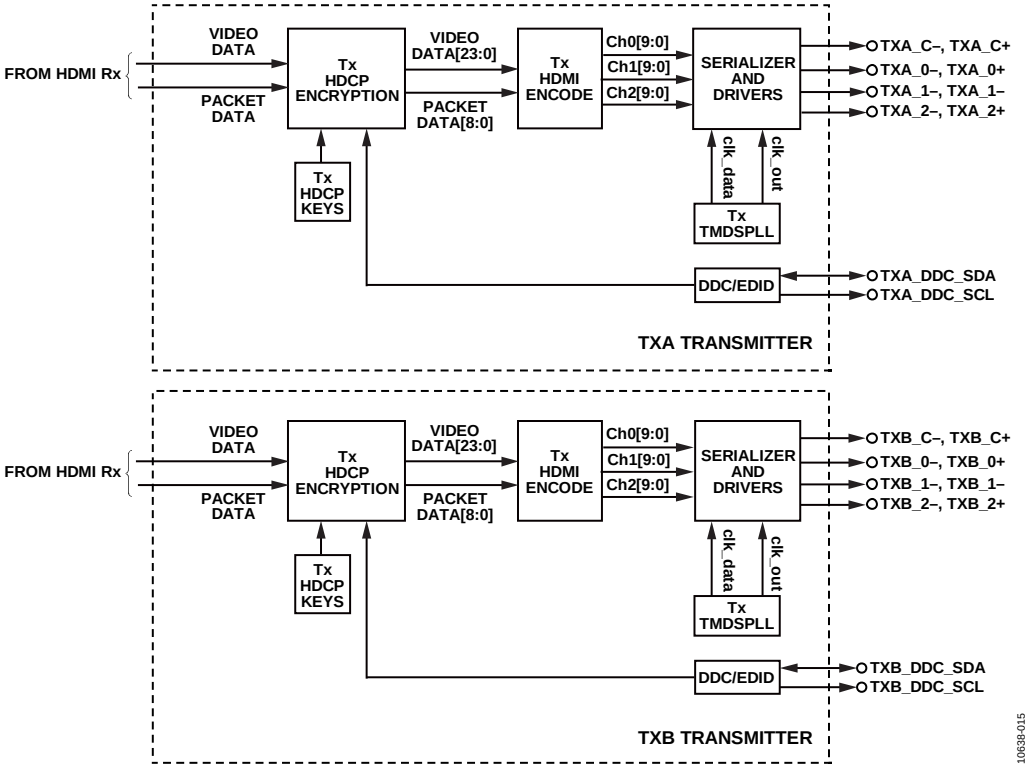


Figure 14. Functional Block Diagram of TXA and TXB Transmitter Sections

The ADV7630 contains two HDMI transmitters, TXA and TXB. Because these two transmitters can be configured independently, there are separate register maps for both the HDMI TXA and HDMI TXB. The I²C slave address for each of maps can be programmed using slave address registers separately using appropriate register listed in Table 25.

Table 25. HDMI Transmitter Maps

Register Map	Map Type	Slave address register location
TXA Register Maps	Main TXA Map	IO Map, Register 0xEE
	EDID TXA Map	IO Map, Register 0xF0
	Test TXA Map	IO Map, Register 0xF1
TXB Register Maps	Main TXB Map	IO Map, Register 0xEA
	EDID TXB Map	IO Map, Register 0xEC
	Test TXB Map	IO Map, Register 0xED

It should be noted that, although most of this section about the HDMI TXA and TXB transmitters refers to TXA, it also applies to TXB. Unless otherwise stated, the same register bits and controls listed in Table 25 apply for both transmitters and should be treated accordingly.

INTERFACE WITH HDMI RECEIVER SECTION

The HDMI_PORT_SELECT_TX_A[2:0] control sets the HDMI input port from which the ADV7630 decodes the primary digital stream containing video pixel, packet and control data. When the TXA is configured in mux mode, the TXA section is fed with the primary stream which it re-encodes into a TMDS stream.

The HDMI_PORT_SELECT_TX_B[2:0] control sets the HDMI input port from which the ADV7630 decodes the secondary digital stream. The secondary stream is fed into the TXB transmitter section. Note that the TXB section supports only mux mode, which consists of routing the secondary digital stream from the receive section into TXB.

HDMI_PORT_SELECT_TX_A and HDMI_PORT_SELECT_TX_B must be set to the same port at all times.

The secondary digital stream that is fed into the TXB section is never HDCP encrypted. The TXB transmitter may optionally encrypt the stream it receives before re-encoding the resulting stream into TMDS stream output via the HDMI TXB output port.

GENERAL CONTROLS

To operate the TXA transmitter section, it is necessary to monitor the HPD signal from the downstream sink and power up the TXA transmitter section after HPD becomes high, meaning that the TXA is attached to an HDMI sink with an available E-EDID. To power up the TXA section, the SYSTEM_PD bit must be written to 0 when the TXA_HPD pin is high. The status of the TXA_HPD pin is provided via the HPD_STATE bit.

When the signal on the TXA_HPD input pin is low, some registers cannot be written to because they are held in reset. When the level on the TXA_HPD pin goes from high to low, some registers are reset to their default value. Refer to Table 7 for a list of registers that are reset when the HPD signal from the downstream sink goes low.

If there is a need to power up the TXA while the HPD signal of the downstream sink is low, the level on the TXA_HPD input pin can be overridden by setting the HPD_DISABLE[1:0] register to 0b11.

Using the interrupt system is the best method to determine when the level of the signal on the TXA_HPD pin is high. An interrupt can be enabled to notify a level change on the TXA_HPD pin (refer to the System Monitoring section).

The TXA section also features the MSEN_STATE status bit, which can be used to detect the presence of TMDS clock terminations from the downstream sink connected to TXA. If the TXA transmitter detects a voltage level that is higher than 1.8 V on the clock lines of its TMDS output port, the MSEN_STATE bit is set to 1.

The detection of TMDS clock terminations from the downstream sink is useful to delay powering up the TXA section until the downstream sink is actually ready to receive signals. A typical implementation for a sink is to tie the transmitter 5 V power signal to HPD through a series resistor. In this case, the ADV7630 detects a high level on its TXA_HPD input pin regardless of whether or not the downstream sink is powered on and ready to receive a TMDS stream. For this reason, it is best to wait for both MSEN_STATE and HPD_STATE to be high before powering up the TXA section when trying to achieve minimum power consumption.

Important: When HPD_DISABLE[1:0] is set to 3, the HPD_STATE bit always reports the value as 1, irrespective of the level of the signal on the TXA_HPD input pin.

HPD_STATE, TXA Main Map, Address 0x42[6] (Read Only)

Hot Plug detect input status.

Function

HPD_STATE	Description
0	Hot Plug detect state is low
1	Hot Plug detect state is high

MSEN_STATE, TXA Main Map, Address 0x42[5] (Read Only)

TMDS clock termination detection status.

Function

MSEN_STATE	Description
0	HDMI clock termination not detected
1	HDMI clock termination detected

HPD_DISABLE[1:0], TXA Main Map, Address 0x9F[5:4]

Hot Plug detect override control.

Function

HPD_DISABLE[1:0]	Description
00 (Default)	HPD pin and CDC HPD
01	CDC HPD
10	HPD pin
11	Logic 1

TMDS Clock Inversion

The TMDS clock can be inverted by setting TMDS_CLK_INV_I2C to 1. This can be useful when using test equipment that has a dependency on the relationship between the TMDS clock and the data.

TMDS_CLK_INV_I2C, TXA Main Map, Address 0xEA[1]

TMDS clock inversion control.

Function

TMDS_CLK_INV_I2C	Description
0 (Default)	Normal TMDS clock
1	Inverted TMDS clock

TMDS Output Driver Disable

The TMDS data lines can be disabled setting TRANSDRVENABLE_I2C[2:0] to 0. TMDS clock signal cannot be disabled.

TRANSDRVENABLE _I2C[2:0], TXA Main Map, Address 0xEA[7:5]

TMDS clock inversion control.

Function

TMDS_CLK_INV_I2C[2:0]	Description
000	All TMDS data line drivers disabled
111 (Default)	All TMDS data line drivers enabled

System Monitoring

General Status and Interrupts

The ADV7630 provides interrupts and status bits to notify the state of internal operations in the TXA section. These interrupts and status bits are listed in Table 26 and Table 27. Refer to the TX Section section for details on the use of TXA interrupts.

Table 26. HDMI TXA Interrupt Bits in Main Map, Register 0x96

Bit Name	Bit Position	Description
RI_RDY_ST	0	TBD
HDCP_AUTH_ST	1	When set to 1, it indicates that the HDCP/EDID state machine has transitioned from State 3 to State 4. Once this bit is set, it remains high until it is cleared by setting it to 1.
EDID_RDY_ST	2	When set to 1, it indicates that the E-EDID was read from the receiver and is available in the packet map. Once this bit is set, it remains high until it is cleared by setting it to 1.
MSEN_ST	6	When set to 1, it indicates that the TMDS clock lines voltage has crossed 1.8 V from high to low or low to high. Once this bit is set, it remains high until it is cleared by setting it to 1.
HPD_ST	7	When set to 1, it indicates that a transition for high to low or low to high was detected on the input HPD signal. Once this bit is set, it remains high until it is cleared by setting it to 1.

Table 27. HDMI TXA Interrupt Bits in Main Map, Register 0x97

Bit Name	Bit Position	Description
BKSV_FLAG_ST	6	When set to 1, it indicates that the KSVs from the downstream sink were read and are available in the memory map. Once this bit is set, it remains high until it is cleared by setting it to 1.
HDCP_ERROR_ST	7	When set to 1, it indicates that the HDCP/EDID controller has reported an error. This error is available in HDCP_CONTROLLER_ERROR. Once this bit is set, it remains high until it is cleared by setting it to 1.

Table 28. TXA Status Bits in Main Map, Register 0x42

Bit Name	Bit Position	Description
HPD_STATE	6	Refer to the description on Page 68
MSEN_STATE	5	Refer to the description on Page 68

EDID/HDCP Controller Status

The TXA section features an E-EDID/HDCP controller that handles E-EDID extraction from the downstream sink. This E-EDID/HDCP controller also handles HDCP authentication with the downstream sink. The tasks that the TXA E-EDID/HDCP controller performs are described in the E-EDID Handling and HDCP Handling sections.

The current state of the TXA E-EDID/HDCP controller can be read from the HDCP_CONTROLLER_STATE[3:0] status field.

HDCP_CONTROLLER_STATE[3:0], TXA Main Map, Address 0xC8[3:0] (Read Only)

HDCP controller status.

Function

HDCP_CONTROLLER_STATE[3:0]	Description
0000	In reset (no Hot Plug detected)
0001	Reading E-EDID
0010	IDLE (waiting for HDCP requested)
0011	Initializing HDCP
0100	HDCP enable
0101	Initializing HDCP repeater

EDID/HDCP Controller Error Codes

If an HDCP authentication occurs between the TXA and the downstream sink, the TXA can trigger an interrupt to notify the user or the controlling CPU of this error. The E-EDID/HDCP controller then reports the HDCP error code via the HDCP_CONTROLLER_ERROR[3:0] status field.

The error code is valid only when the HDCP_ERROR_ST interrupt bit is set to 1. The last error code remains in the HDCP/EDID controller error field, even when the interrupt is cleared. Refer to the TX Section section for information about using interrupts.

HDCP_CONTROLLER_ERROR[3:0], TXA Main Map, Address 0xC8[7:4] (Read Only)

HDCP error information readback.

Function

HDCP_CONTROLLER_ERROR[3:0]	Description
0000	No error
0001	Bad receiver BKSV
0010	Ri mismatch
0011	Pj mismatch
0100	I^2C error (usually a no acknowledge)
0101	Time out waiting for downstream repeater DONE
0110	Maximum cascade of repeaters exceeded
0111	SHA-1 hash check of KSV list failed
1000	Too many devices connected to repeater tree

HDCP_ERROR_ST, TXA Main Map, Address 0x97[7]

Interrupt bit from HDCP master.

Function

HDCP_ERROR_ST	Description
0	No interrupt detected
1	Interrupt detected

E-EDID HANDLING

Reading E-EDID

The TXA section of the ADV7630 features an E-EDID/HDCP controller that can read the E-EDID content of the downstream sink through the DDC lines, TXDDC_SCL and TXDDC_SDA. This E-EDID/HDCP controller begins buffering Segment 0 of the downstream sink's E-EDID once the sink's HPD is detected and the TXA section of the ADV7630 is powered up.

The system can request additional segments by programming the E-EDID segment pointer EDID_SEGMENT[7:0]. The EDID_READY_FLAG interrupt bit (see Table 37) indicates that a 256-byte E-EDID read was completed, and the E-EDID content can be read from the EDID map.

EDID_SEGMENT[7:0], TXA Main Map, Address 0xC4[7:0]

Sets the E-DDC segment used by the E-EDID fetch routine.

Function

EDID_SEGMENT[7:0]	Description
0 (Default)	Default value

E-EDID Definitions

E-EDID supports up to 256 segments. A segment is 256 bytes of E-EDID data containing one or two 128-byte E-EDID blocks. A typical HDMI sink has only two E-EDID blocks and, therefore, uses only Segment 0. The first E-EDID block is always a base E-EDID structure, defined in the VESA E-EDID specification; the second E-EDID block is usually the CEA extension, defined in the CEA-861 specification.

The TxA transmitter section has a single memory location used to store E-EDID and HDCP information read from the downstream sink. During HDCP repeater initialization, the E-EDID data read from the sink is overwritten with HDCP information, also read from the sink. The E-EDID of the sink is not reread after HDCP initialization.

Additional Segments

The E-EDID Block 0, Byte Number 0x7E, tells how many additional E-EDID blocks are available. If Byte 0x7E is greater than 1, additional E-EDID segments must be read. If there is more than one segment, the second block (that is, Block 1) is required to be an E-EDID extension map. This map should be parsed according to the VESA E-EDID specification to determine where additional E-EDID blocks are stored in the sink's E-EDID storage device (that is, EEPROM, RAM, and so on).

The TxA transmitter is capable of accessing up to 256 segments from E-EDID of the sink, as allowed by the E-EDID specification. By writing the desired segment number to the EDID_SEGMENT[7:0] field, the TXA automatically accesses the correct portion of the sink's E-EDID over the Tx DDC lines and loads the 256 bytes into the E-EDID/HDCP memory. When the action is complete, the TxA triggers the EDID_READY_FLAG interrupt (refer to Table 37). The E-EDID data read from the sink can then be accessed from the Tx EDID map. If the host controller needs access to previously requested E-EDID information, then it can be stored in its own memory.

Figure 15 shows how to implement the software to read E-EDID from the downstream sink that is connected to the TxA transmitter.

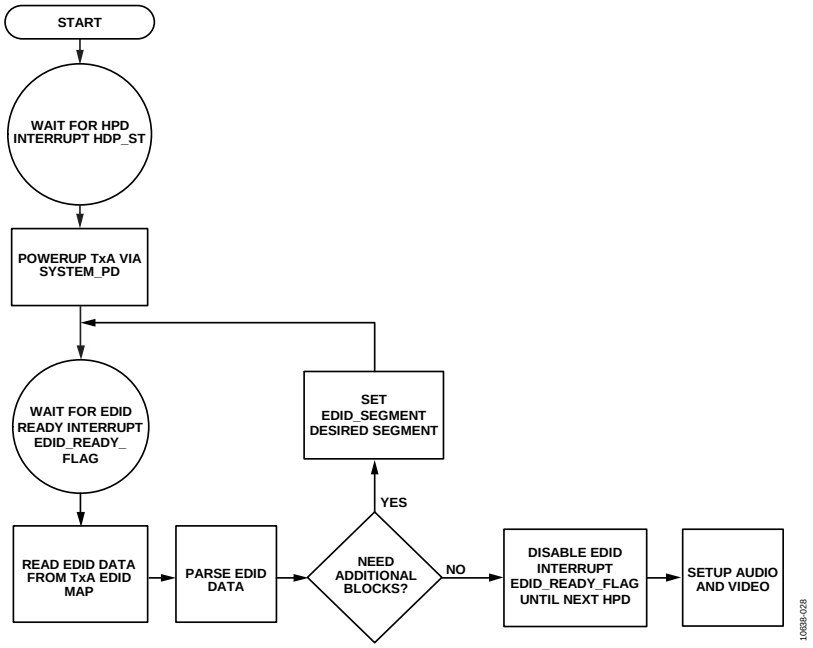


Figure 15. Reading Sink's E-EDID Through TXA Transmitter

EDID_TRIES Control

The EDID_TRIES[3:0] field can be used to set the number of times the Tx E-EDID/HDCP controller tries to read the E-EDID of the sink after a failure. Each time an E-EDID read fails with an I²C no acknowledge (NACK), the EDID_TRIES[3:0] value decrements. When EDID_TRIES[3:0] reaches a value of 0, the Tx E-EDID/HDCP controller does not attempt to read the E-EDID until EDID_TRIES[3:0] is set to a value other than 0.

This could be used if a sink asserts its HPD signal high before the DDC bus is ready, resulting in several NACKs as the TXA transmitter attempts to read the E-EDID.

EDID_TRIES[3:0], TXA Main Map, Address 0xC9[3:0]

Maximum number of times E-EDID read is attempted if unsuccessful. E-EDID reading begins upon setting of this register and on power-up.

Function

EDID_TRIES[3:0]	Description
3 (default)	Default value

If the E-EDID data from the sink is read in and the host determines that the data must be reread, the EDID_TRIES[3:0] bit can be set from 0 to 1, and the current segment set via the EDID_SEGMENT[7:0] field is reread. Rereading the E-EDID of the sink may be useful, for example, if the host finds that one E-EDID checksum read from the sink is invalid.

Note: It is also possible to reread the E-EDID from the sink by toggling the TXA section power-down bit, SYSTEM_PD, from 0 to 1.

HDCP HANDLING

For One Sink and No Upstream Devices

The ADV7630 has a built-in controller, the TXA E-EDID/HDCP controller, that handles HDCP transmitter states, including handling downstream HDCP repeaters. To activate HDCP from a system level, the host controller must set the HDCP_DESIRED bit to 1 and the FRAME_ENC bit to 1. Doing so informs the TXA that the video stream it outputs should be encrypted. The TXA takes control from there and implements all of the remaining tasks defined by the HDCP 1.4 specification.

Before sending audio and video, the BKSV of the downstream sink should be compared with the revocation list compiled by managing System Renewability Messages (SRMs) provided on the source content (for example, DVD, Blue-ray Disc), and the BKSV_FLAG_ST interrupt bit should be cleared.

After the HDCP link is established between the TXA and the downstream sink, the system controller should monitor the status of HDCP by reading the ENC_ON bit every two seconds. The TX E-EDID/HDCP controller error interrupt activates, and the HDCP_ERROR_ST bit is set to 1 if there is an error relating to the controller. The error meaning can be determined by checking the HDCP_CONTROLLER_ERROR[3:0] field.

BKSV_FLAG_ST, TXA Main Map, Address 0x97[6]

This interrupt indicates whether EDID or BKSV is available in the HDMI Tx.

Function

BKSV_FLAG_ST	Description
0 (default)	No interrupt
1	Read BKSV or EDID MEM for revocation list checking

HDCP_DESIRED, TXA Main Map, Address 0xAF[7]

This register indicates if the HDCP function should be enabled.

Function

HDCP_DESIRED	Description
0 (default)	Disable HDCP
1	Enable HDCP

FRAME_ENC, TXA Main Map, Address 0xAF[4]

This register allows for sending unencrypted content without disabling HDCP. This is valid only when HDCP_DESIRED is set to 1.

Function

FRAME_ENC	Description
0 (default)	Current frame is not to be encrypted
1	Current frame is to be encrypted

ENC_ON, TXA Main Map, Address 0xB8[6] (Read only)

This register indicates if the current A/V content is being encrypted.

Function

ENC_ON	Description
0 (default)	Not encrypted
1	Encrypted

BKSV0[7:0], TXA Main Map, Address 0xBF[7:0] (Read Only)

BKSV read from Rx by the HDCP controller.

Function

BKSV0[7:0]	Description
0	Default value

BKSV1[7:0], TXA Main Map, Address 0xC0[7:0] (Read Only)

BKSV read from Rx by the HDCP controller.

Function

BKSV1[7:0]	Description
0	Default value

BKSV2[7:0], TXA Main Map, Address 0xC1[7:0] (Read Only)

BKSV read from Rx by the HDCP controller.

Function

BKSV2[7:0]	Description
0	Default value

BKSV3[7:0], TXA Main Map, Address 0xC2[7:0] (Read Only)

BKSV read from Rx by the HDCP controller.

Function

BKSV3[7:0]	Description
0	Default value

BKSV4[7:0], TXA Main Map, Address 0xC3[7:0] (Read Only)

BKSV read from Rx by the HDCP controller.

Function

BKSV4[7:0]	Description
0	Default value

For Multiple Sinks and No Upstream Devices

When connecting the TXA as source to an HDMI input of a repeater, it is necessary to read all BKSVs from downstream devices. These BKSVs must be checked against a revocation list, which is provided on the source content.

The BKSV_COUNT[6:0] field reads 0 when the first BKSV interrupt occurs with the BKSV_FLAG_ST bit set to 1. After the first BKSV interrupt is cleared, if the sink connected to the TXA is a repeater, a second BKSV interrupt occurs. The TXA transmitter automatically reads up to 13 5-byte BKSVs at a time and stores them in the E-EDID TXA I^2C map.

These BKSVs can be accessed from the EDID map, as shown in Table 29. The number of additional BKSVs available in the EDID map can be obtained from the BKSV_COUNT[6:0] field. If there are more than 13 additional BKSVs to be processed, the TXA collects the next up to 13 BKSVs from the sink. It then generates another BKSV interrupt, with the BKSV_FLAG_ST bit set to 1, when the next set of 13 additional BKSVs is ready to be read from the TXA EDID I^2C Map.

The BKVS interrupt bit, BKSV_FLAG_ST = 1, should be cleared by setting BKSV_FLAG_ST to 1 after each set of BKSVs is read. To check when authentication is complete, the system should monitor the HDCP_CONTROLLER_STATE[3:0] field and wait until this field reaches the value or state = 4. At this time, the last host controller should compare the BKSV list read from the sink with the revocation list. When the host controller has verified that none of the BKSVs read from the sink is revoked, the TXA can be configured to send content down to the sink.

BKSV_COUNT[6:0], TXA Main Map, Address 0xC7[6:0] (Read Only)

BKSVs available in sink's BKSV FIFO.

Function

BKSV_COUNT[6:0]	Description
0	Default value

For Use In Repeater

The ADV7630 can be used as both the front end and the back end of a repeater. This section explains how to use TxA as the back end (that is, the transmitter side) of a repeater. See the Repeater Support section on using the ADV7630 as the front end (i.e., the receiver side) of a repeater.

When the TXA transmitter is used as the back end of a repeater, the system software must pass the KSVs of all downstream devices up to the front end of the repeater (for example, the receiver section of the ADV7630). In addition, the depth of the device tree and the total number of devices must be communicated upstream. This depth and device count information can be found in the BSTATUS information. (DEVICE_COUNT[6:0] is located in the BSTATUS[15:0] register, Bits[6:0]. DEPTH[2:0] is located in the BSTATUS[15:0] register, Bits[10:8]; refer to the HDCP Specification.)

Note: The BSTATUS information is available only when the KSVs are in the E-EDID memory space (BSTATUS[15:8] at 0xFA[7:0] and BSTATUS[7:0] at 0xF9[7:0]) and can, therefore, be read back from the Tx EDID map. The time period during which the KSVs are stored in the E-EDID memory is from the time of a BKSV interrupt (that is, BKSV_FLAG_ST is set to 1) with BKSV_COUNT[6:0] greater than 0 until the BKSV_FLAG_ST interrupt flag is cleared (refer to the For One Sink and No Upstream Devices section). The E-EDID of the downstream sink is not automatically rebuffered.

Table 29. KSV Fields Accessed from E-EDID Map

KSV Number	Field Name	Register Addresses
0	BKSV0_BYTE_0[7:0]	0x00[7:0], Byte 0
	BKSV0_BYTE_1[7:0]	0x01[7:0], Byte 1
	BKSV0_BYTE_2[7:0]	0x02[7:0], Byte 2
	BKSV0_BYTE_3[7:0]	0x03[7:0], Byte 3
	BKSV0_BYTE_4[7:0]	0x04[7:0], Byte 4
1	BKSV1_BYTE_0[7:0]	0x05[7:0], Byte 0
	BKSV1_BYTE_1[7:0]	0x06[7:0], Byte 1
	BKSV1_BYTE_2[7:0]	0x07[7:0], Byte 2
	BKSV1_BYTE_3[7:0]	0x08[7:0], Byte 3
	BKSV1_BYTE_4[7:0]	0x09[7:0], Byte 4

KSV Number	Field Name	Register Addresses
2	BKSV2_BYTE_0[7:0]	0x0A[7:0], Byte 0
	BKSV2_BYTE_1[7:0]	0x0B[7:0], Byte 1
	BKSV2_BYTE_2[7:0]	0x0C[7:0], Byte 2
	BKSV2_BYTE_3[7:0]	0x0D[7:0], Byte 3
	BKSV2_BYTE_4[7:0]	0x0E [7:0], Byte 4
3	BKSV3_BYTE_0[7:0]	0x0F[7:0], Byte 0
	BKSV3_BYTE_1[7:0]	0x10[7:0], Byte 1
	BKSV3_BYTE_2[7:0]	0x11[7:0], Byte 2
	BKSV3_BYTE_3[7:0]	0x12[7:0], Byte 3
	BKSV3_BYTE_4[7:0]	0x13[7:0], Byte 4
4	BKSV4_BYTE_0[7:0]	0x14[7:0], Byte 0
	BKSV4_BYTE_1[7:0]	0x15[7:0], Byte 1
	BKSV4_BYTE_2[7:0]	0x16[7:0], Byte 2
	BKSV4_BYTE_3[7:0]	0x17[7:0], Byte 3
	BKSV4_BYTE_4[7:0]	0x18[7:0], Byte 4
5	BKSV5_BYTE_0[7:0]	0x19[7:0], Byte 0
	BKSV5_BYTE_1[7:0]	0x1A[7:0], Byte 1
	BKSV5_BYTE_2[7:0]	0x1B[7:0], Byte 2
	BKSV5_BYTE_3[7:0]	0x1C[7:0], Byte 3
	BKSV5_BYTE_4[7:0]	0x1D[7:0], Byte 4
6	BKSV6_BYTE_0[7:0]	0x1E[7:0], Byte 0
	BKSV6_BYTE_1[7:0]	0x1F[7:0], Byte 1
	BKSV6_BYTE_2[7:0]	0x20[7:0], Byte 2
	BKSV6_BYTE_3[7:0]	0x21[7:0], Byte 3
	BKSV6_BYTE_4[7:0]	0x22[7:0], Byte 4
7	BKSV7_BYTE_0[7:0]	0x23[7:0], Byte 0
	BKSV7_BYTE_1[7:0]	0x24[7:0], Byte 1
	BKSV7_BYTE_2[7:0]	0x25[7:0], Byte 2
	BKSV7_BYTE_3[7:0]	0x26[7:0], Byte 3
	BKSV7_BYTE_4[7:0]	0x27[7:0], Byte 4
8	BKSV8_BYTE_0[7:0]	0x28[7:0], Byte 0
	BKSV8_BYTE_1[7:0]	0x29[7:0], Byte 1
	BKSV8_BYTE_2[7:0]	0x2A[7:0], Byte 2
	BKSV8_BYTE_3[7:0]	0x2B[7:0], Byte 3
	BKSV8_BYTE_4[7:0]	0x2C[7:0], Byte 4
9	BKSV9_BYTE_0[7:0]	0x2D[7:0], Byte 0
	BKSV9_BYTE_1[7:0	0x2E[7:0], Byte 1
	BKSV9_BYTE_2[7:0]	0x2F[7:0], Byte 2
	BKSV9_BYTE_3[7:0]	0x30[7:0], Byte 3
	BKSV9_BYTE_4[7:0]	0x31[7:0], Byte 4
10	BKSV10_BYTE_0[7:0]	0x32[7:0], Byte 0
	BKSV10_BYTE_1[7:0]	0x33[7:0], Byte 1
	BKSV10_BYTE_2[7:0]	0x34[7:0], Byte 2
	BKSV10_BYTE_3[7:0]	0x35[7:0], Byte 3
	BKSV10_BYTE_4[7:0]	0x36[7:0], Byte 4
11	BKSV11_BYTE_0[7:0]	0x37[7:0], Byte 0
	BKSV11_BYTE_1[7:0]	0x38[7:0], Byte 1
	BKSV11_BYTE_2[7:0]	0x39[7:0], Byte 2
	BKSV11_BYTE_3[7:0]	0x3A[7:0], Byte 3
	BKSV11_BYTE_4[7:0]	0x3B[7:0], Byte 4
12	BKSV12_BYTE_0[7:0]	0x3C[7:0], Byte 0
	BKSV12_BYTE_1[7:0]	0x3D[7:0], Byte 1
	BKSV12_BYTE_2[7:0]	0x3E[7:0], Byte 2
	BKSV12_BYTE_3[7:0]	0x3F[7:0], Byte 3
	BKSV12_BYTE_4[7:0]	0x40[7:0], Byte 4

Software Implementation

Figure 16 provides a block diagram of HDCP software implementation for all cases using the TXA HDCP/EDID controller state machine. The necessary interactions with the TXA registers and E-EDID memory, as well as when these interactions should take place, are shown in the block diagram. Note that there is no need to interact with the DDC bus directly because all the DDC functionality is controlled by the TX HDCP/EDID controller and follows the HDCP Specification 1.4.

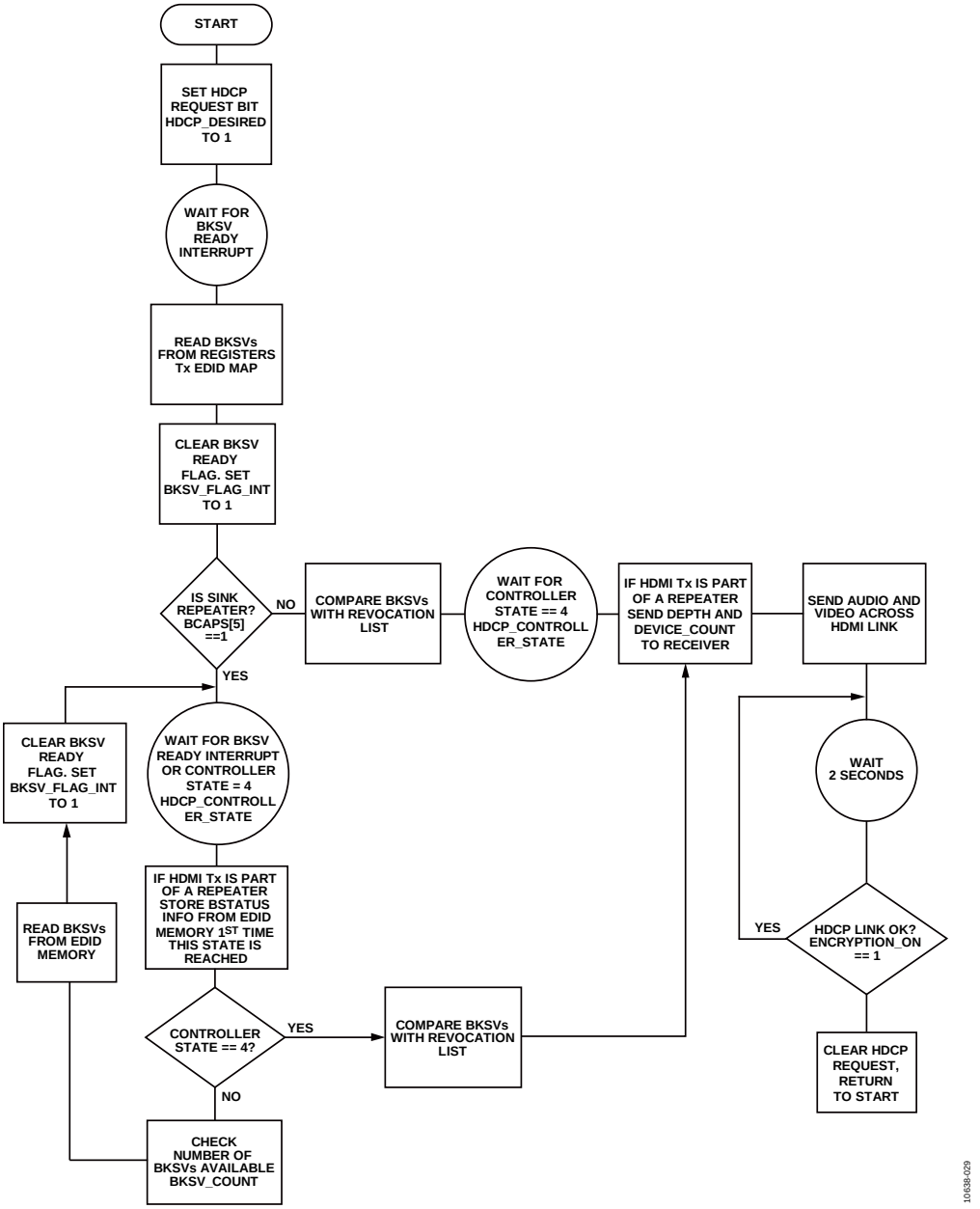


Figure 16. HDCP Software Implementation

DISABLING DRIVERS

To disable drivers, the TransDrvEnable register should be used with the respective TXA or TXB Main Map.

TRANSDRVENABLE[2:0], TXA Main Map, Address 0xEB[7:5]

Enables or disables three TMDS data output currents of the HDMI transmitter.

Function

TRANSDRVENABLE[2:0]	Description
000	Drivers disabled
111 (Default)	Drivers enabled

CONSUMER ELECTRONICS CONTROL

The Consumer Electronics Control (CEC) module features the hardware that is required to behave as an initiator or a follower, as per the specifications for a CEC device. The CEC module contains the following four main sections:

- Transmit section, CEC_TX
- Receive section, CEC_RX
- Clock generator section, CEC_CLK_GEN
- Antiglitch filter section, CEC_ANTI_GLITCH

A block diagram of the CEC module is shown in Figure 17.

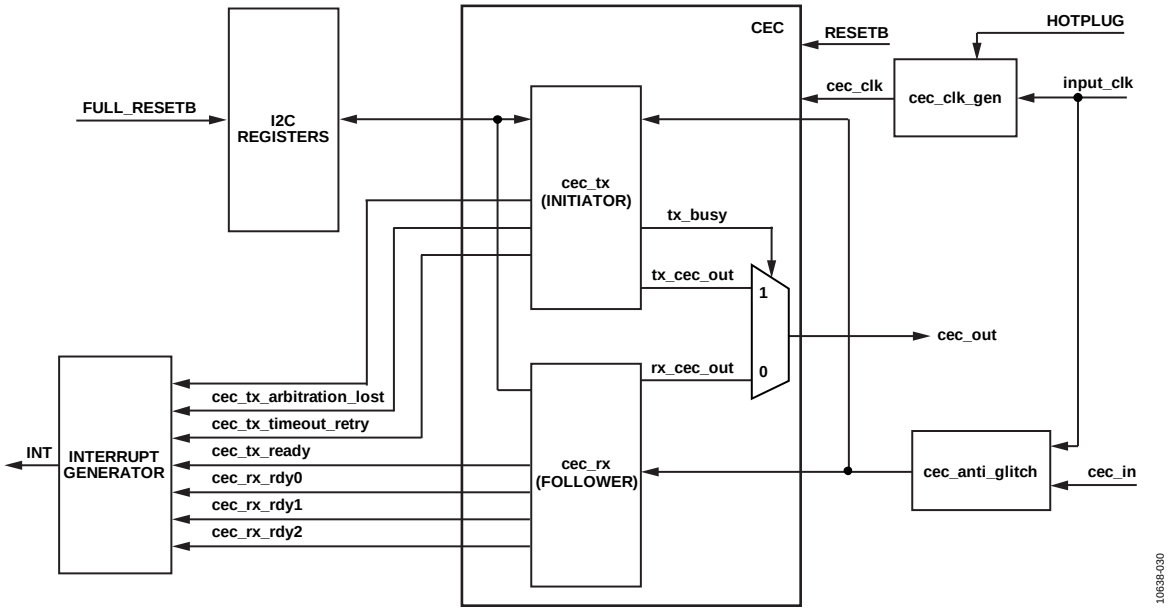


Figure 17. CEC Module Block Diagram

MAIN CONTROLS

This section describes the main controls for the CEC module.

CEC_POWER_UP, Addr 42 (CEC), Address 0x2A[0]

Power mode of CEC module.

Function

CEC_POWER_UP	Description
0 (default)	Power down the CEC module
1	Power up the CEC module

CEC_SOFT_RESET, Addr 42 (CEC), Address 0x2C[0] (Self-Clearing)

CEC module software reset.

Function

CEC_SOFT_RESET	Description
0 (default)	No function
1	Reset the CEC module

CEC TRANSMIT SECTION

The transmit section features the hardware required for the CEC module to act as an initiator. The host utilizes this section to transmit directly addressed messages or broadcast messages on the CEC bus. When the host wants to a send message to other CEC devices, it writes the message to the CEC outgoing message registers (see Table 30) and the message length register, CEC_TX_FRAME_LENGTH[4:0].

The host then enables the transmission process by setting the CEC_TX_ENABLE bit to 1. When the message transmission is complete or an error occurs, the CEC transmitter section generates an interrupt (assuming that the corresponding interrupt mask bits are set accordingly).

CEC_TX_FRAME_LENGTH[4:0], Addr 42 (CEC), Address 0x10[4:0]

Message size of the transmitted frame. This is the number of bytes in the outgoing message, including the header.

Function

CEC_TX_FRAME_LENGTH[4:0]	Description
xxxxx	Total number of bytes (including header byte) to be sent

CEC_TX_ENABLE, CEC Map, Address 0x11[0]

This bit enables the TX section. When set to 1, it initiates the start of transmission of the message in the outgoing message buffer. When the message transmission is complete, this bit is automatically reset to 0. If manually set to 0 during a message transmission, this bit may terminate the transmission, depending on the stage the transmission process has reached. If the message transmission is still in the 'signal free time' stage, the message transmission is terminated. If data transmission has begun, the transmission continues until the message is fully sent or until an error condition occurs.

Function

CEC_TX_ENABLE	Description
0 (default)	Transmission mode disabled
1	Transmission mode enabled, and message transmission started

Table 30. CEC Outgoing Message Buffer Registers

Register Name	CEC Map Address	Description
TX_FRAME_HEADER[7:0]	0x00	Header of next outgoing message
TX_FRAME_DATA0[7:0]	0x01	Byte 0 of next outgoing message
TX_FRAME_DATA1[7:0]	0x02	Byte 1 of next outgoing message
TX_FRAME_DATA2[7:0]	0x03	Byte 2 of next outgoing message
TX_FRAME_DATA3[7:0]	0x04	Byte 3 of next outgoing message
TX_FRAME_DATA4[7:0]	0x05	Byte 4 of next outgoing message
TX_FRAME_DATA5[7:0]	0x06	Byte 5 of next outgoing message
TX_FRAME_DATA6[7:0]	0x07	Byte 6 of next outgoing message
TX_FRAME_DATA7[7:0]	0x08	Byte 7 of next outgoing message
TX_FRAME_DATA8[7:0]	0x09	Byte 8 of next outgoing message
TX_FRAME_DATA9[7:0]	0x0A	Byte 9 of next outgoing message
TX_FRAME_DATA10[7:0]	0x0B	Byte 10 of next outgoing message
TX_FRAME_DATA11[7:0]	0x0C	Byte 11 of next outgoing message
TX_FRAME_DATA12[7:0]	0x0D	Byte 12 of next outgoing message
TX_FRAME_DATA13[7:0]	0x0E	Byte 13 of next outgoing message
TX_FRAME_DATA14[7:0]	0x0F	Byte 14 of next outgoing message

The ADV7630 features three status bits relating to the transmission of CEC messages. The events that set these bits are mutually exclusive; that is, only one of the three events can occur during any given message transmission.

- CEC_TX_READY_ST
- CEC_TX_ARBITRATION_LOST_ST
- CEC_TX_RETRY_TIMEOUT_ST

CEC_TX_READY_ST, IO Map, Address 0x93[0] (Read Only)

Latched status of CEC_TX_READY_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. When the CEC Tx successfully sends the current message this bit is set. Once set, the bit remains high until the interrupt is cleared via CEC_TX_READY_CLR.

Function

CEC_TX_READY_ST	Description
0	No change
1	Message transmitted successfully

CEC_TX_ARBITRATION_LOST_ST, IO Map, Address 0x93[1] (Read Only)

Latched status of CEC_TX_ARBITRATION_LOST_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. If the CEC Tx loses arbitration while trying to send a message, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_TX_ARBITRATION_LOST_CLR.

Function

CEC_TX_ARBITRATION_LOST_ST	Description
0	No change
1	CEC Tx has lost arbitration to another Tx

CEC_TX_RETRY_TIMEOUT_ST, IO Map, Address 0x93[2] (Read Only)

Latched status of CEC_TX_RETRY_TIMEOUT_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. If the CEC Tx fails to send the current message within the number of retry attempts specified by CEC_TX_RETRY this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_TX_RETRY_TIMEOUT_CLR.

Function

CEC_TX_RETRY_TIMEOUT_ST	Description
0	No change
1	CEC Tx tried but failed to resend the current message for the number of times specified by CEC_TX_RETRY

CEC_TX_RETRY[2:0], Addr 42 (CEC), Address 0x12[6:4]

The number of times the CEC Tx should try to retransmit the message if an error condition is encountered. Per the CEC specification, this value should not be set to a value greater than 5.

Function

CEC_TX_RETRY[2:0]	Description
001 (Default)	Try to retransmit the message once if an error occurs
xxx	Try to retransmit the message xxx times if an error occurs

CEC_TX_NACK_COUNTER[3:0], Addr 42 (CEC), Address 0x14[3:0] (Read Only)

The number of times that the NACK error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1.

Function

CEC_TX_NACK_COUNTER[3:0]	Description
0000	No error condition
XXXX	Number of times the NACK error condition was encountered

CEC_TX_LOWDRIVE_COUNTER[3:0], Addr 42 (CEC), Address 0x14[7:4] (Read Only)

The number of times that the LOWDRIVE error condition was encountered while trying to send the current message. This register is reset to 0b0000 when CEC_TX_ENABLE is set to 1.

Function

CEC_TX_LOWDRIVE_COUNTER[3:0]	Description
0000	No error condition
XXXX	Number of times the LOWDRIVE error condition was encountered

CEC RECEIVE SECTION

The receive section features the hardware required for the CEC module to act as a follower. When the CEC module is powered up via the CEC_POWER_UP bit, the CEC Rx section immediately begins monitoring the CEC bus for messages with the correct logical address(es). When the message reception is completed, the CEC receive section generates an interrupt (assuming that the corresponding interrupt mask bits are set accordingly).

The host can disable message reception while keeping the CEC module powered up by using the CEC_FORCE_NACK bit to not acknowledge received messages.

CEC_FORCE_NACK, Addr 42 (CEC), Address 0x27[1]

Setting this bit forces the CEC controller to not acknowledge any received messages.

Function

CEC_FORCE_NACK	Description
0 (Default)	Acknowledge received messages
1	Do not acknowledge received messages

Logical Address Configuration

The host must set the destination logical address(es) to which the CEC receive section responds. Up to three logical addresses can be enabled, allowing support for multifunction devices, such as DVD recorders with TV tuners, which require multiple logical addresses. The logical address(es) are set via the following registers:

- CEC_LOGICAL_ADDRESS2[3:0] if CEC_LOGICAL_ADDRESS_MASK[2] is set to 1
- CEC_LOGICAL_ADDRESS1[3:0] if CEC_LOGICAL_ADDRESS_MASK[1] is set to 1
- CEC_LOGICAL_ADDRESS0[3:0] if CEC_LOGICAL_ADDRESS_MASK[0] is set to 1

CEC_LOGICAL_ADDRESS_MASK[2:0], CEC Map, Address 0x27[6:4]

Logical address mask of the CEC logical devices. Up to three logical devices are supported. When the mask bits are set for a particular logical device, the logical device is enabled and messages whose destination address matches that of the selected logical address.

Function

CEC_LOGICAL_ADDRESS_MASK[2:0]	Description
[4]	Mask bit for Logical Device 0
[5]	Mask bit for Logical Device 1
[6]	Mask bit for Logical Device 2

CEC_LOGICAL_ADDRESS2[3:0], Addr 42 (CEC), Address 0x29[3:0]

Logical Address 2. This address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[2] to 1.

Function

CEC_LOGICAL_ADDRESS2[3:0]	Description
1111 (Default)	Default value
xxxx	User specified logical address

CEC_LOGICAL_ADDRESS1[3:0], Addr 42 (CEC), Address 0x28[7:4]

Logical Address 1. This address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[1] to 1.

Function

CEC_LOGICAL_ADDRESS1[3:0]	Description
1111 (Default)	Default value
xxxx	User specified logical address

CEC_LOGICAL_ADDRESS0[3:0], Addr 42 (CEC), Address 0x28[3:0]

Logical Address 0. This address must be enabled by setting CEC_LOGICAL_ADDRESS_MASK[0] to 1.

Function

CEC_LOGICAL_ADDRESS0[3:0]	Description
1111 (Default)	Default value
xxxx	User specified logical address

Receive Buffers

The ADV7630 features three frame buffers that allow the receiver to receive up to three messages before the host processor must read a message out. When three messages are received, no further message reception is possible until the host reads at least one message.

Note: Only one frame buffer is enabled by default. In this default mode, after a message is received, the host processor must read the message out before any further message reception is possible. The decision to use one or three message buffers is controlled by the CEC_USE_ALL_BUFS bit.

CEC_USE_ALL_BUFS, CEC Map, Address 0x77[0]

Control to enable supplementary receiver frame buffers.

Function

CEC_USE_ALL_BUFS	Description
0 (Default)	Use only Buffer 0 to store CEC frames
1	Use all three buffers to store CEC frames

For each of the frame buffers, there are a corresponding 2-bit time stamp and an interrupt status flag, as follows.

CEC_BUF0_TIMESTAMP[1:0], CEC Map, Address 0x53[1:0] (Read Only)

Time stamp for frame stored in Receiver Frame Buffer 0. This time stamp can be used to determine which frame should be read next from the receiver frame buffers.

Function

CEC_BUF0_TIMESTAMP[1:0]	Description
00	Invalid time stamp; no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered

CEC_BUF1_TIMESTAMP[1:0], CEC Map, Address 0x53[3:2] (Read Only)

Time stamp for frame stored in Receiver Frame Buffer 1. This time stamp can be used to determine which frame should be read next from the receiver frame buffers.

Function

CEC_BUF1_TIMESTAMP[1:0]	Description
00	Invalid time stamp; no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered

CEC_BUF2_TIMESTAMP[1:0], CEC Map, Address 0x53[5:4] (Read Only)

Time stamp for frame stored in Receiver Frame Buffer 2. This time stamp can be used to determine which frame should be read next from the receiver frame buffers.

Function

CEC_BUF2_TIMESTAMP[1:0]	Description
00	Invalid time stamp; no frame is available in this frame buffer
01	Of the frames currently buffered, this frame was the first to be received
10	Of the frames currently buffered, this frame was the second to be received
11	Of the frames currently buffered

CEC_RX_RDY0_ST, IO Map, Address 0x93[3] (Read Only)

Latched status of CEC_RX_RDY0_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. When a message is received into Buffer 0, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY0_CLR.

Function

CEC_RX_RDY0_ST	Description
0	No change
1	New CEC message received in Buffer 0

CEC_RX_RDY1_ST, IO Map, Address 0x93[4] (Read Only)

Latched status of CEC_RX_RDY1_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. When a message is received into Buffer 1, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY1_CLR.

Function

CEC_RX_RDY1_ST	Description
0	No change
1	New CEC message received in Buffer 1

CEC_RX_RDY2_ST, IO Map, Address 0x93[5] (Read Only)

Latched status of CEC_RX_RDY2_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. When a message is received into Buffer 2, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY2_CLR.

Function

CEC_RX_RDY2_ST	Description
0	No change
1	New CEC message received in Buffer 2

CEC_RX_RDY2_CLR, IO Map, Address 0x94[5] (Read Only)

Clear bit for CEC Receiver Buffer 2 ready interrupt.

Function

CEC_RX_RDY2_CLR	Description
0	No change
1	Clears CEC_RX_RDY2_ST

CEC_RX_RDY1_CLR, IO Map, Address 0x94[4] (Read Only)

Clear bit for CEC Receiver Buffer 1 ready interrupt.

Function

CEC_RX_RDY1_CLR	Description
0	No change
1	Clears CEC_RX_RDY1_ST

CEC_RX_RDY0_CLR, IO Map, Address 0x94[3] (Read Only)

Clear bit for CEC Receiver Buffer 0 ready interrupt.

Function

CEC_RX_RDY0_CLR	Description
0	No change
1	Clears CEC_RX_RDY0_ST

CEC_RX_RDY2_MB1, IO Map, Address 0x96[5] (Read Only)

INT1 interrupt mask for CEC Receiver Buffer 2 ready interrupt. When set, the CEC Receiver Buffer 2 Ready interrupt triggers the INT1 interrupt and CEC_RX_RDY2_ST indicates the interrupt status.

Function

CEC_RX_RDY2_MB1	Description
0	Disables CEC Receiver Buffer 2 ready interrupt on INT1
1	Enables CEC Receiver Buffer 2 ready interrupt on INT1

CEC_RX_RDY1_MB1, IO Map, Address 0x96[4] (Read Only)

INT1 interrupt mask for CEC Receiver Buffer 1 ready interrupt. When set, the CEC Receiver Buffer 1 ready interrupt triggers the INT1 interrupt and CEC_RX_RDY1_ST indicates the interrupt status.

Function

CEC_RX_RDY1_MB1	Description
0	Disables CEC Receiver Buffer 1 ready interrupt on INT1
1	Enables CEC Receiver Buffer 1 ready interrupt on INT1

CEC_RX_RDY0_MB1, IO Map, Address 0x96[3] (Read Only)

INT1 interrupt mask for CEC Receiver Buffer 0 Ready interrupt. When set, the CEC Receiver Buffer 0 Ready interrupt triggers the INT1 interrupt and CEC_RX_RDY0_ST indicates the interrupt status.

Function

CEC_RX_RDY0_MB1	Description
0	Disables CEC Receiver Buffer 0 ready interrupt on INT1
1	Enables CEC Receiver Buffer 0 ready interrupt on INT1

When a message (other than a polling message) is received, it is loaded into the first available frame buffer (starting with Buffer 0), and a 2-bit time stamp is generated for that buffer. If the corresponding interrupt mask bit is set, the status bit relating to that buffer is set and an interrupt is generated to alert the host processor that a message was received.

When all three frame buffers are full, the receive module can no longer receive CEC messages and does not acknowledge any new messages (other than polling messages). In the case that only one frame buffer is enabled (the default condition), only one message can be received. In this case, the received message is always available in Buffer 0.

The host can read the receive buffers (see Table 31, Table 32, and Table 33) to get the messages that were addressed to the CEC receiver. The length of each received message is available in the corresponding frame length registers:

- CEC_BUF0_RX_FRAME_LENGTH[4:0]
- CEC_BUF1_RX_FRAME_LENGTH[4:0]
- CEC_BUF2_RX_FRAME_LENGTH[4:0]

CEC_BUF0_RX_FRAME_LENGTH[4:0], Address 42 (CEC), Address 0x25[4:0] (Read Only)

Function

CEC_BUF0_RX_FRAME_LENGTH[4:0]	Description
xxxxx	Total number of bytes (including header byte) that have been received into Buffer 0

CEC_BUF1_RX_FRAME_LENGTH[4:0], Address 42 (CEC), Address 0x64[4:0] (Read Only)

Function

CEC_BUF1_RX_FRAME_LENGTH[4:0]	Description
xxxxx	Total number of bytes (including header byte) that have been received into Buffer 1

CEC_BUF2_RX_FRAME_LENGTH[4:0], Address 42 (CEC), Address 0x75[4:0] (Read Only)

Function

CEC_BUF2_RX_FRAME_LENGTH[4:0]	Description
xxxxx	Total number of bytes (including header byte) that have been received into Buffer 2

Table 31. CEC Incoming Frame Buffer 0 Registers

Register Name	CEC Map Address	Description
CEC_BUF0_RX_FRAME_HEADER[7:0]	0x15	Header of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA0[7:0]	0x16	Byte 0 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA1[7:0]	0x17	Byte 1 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA2[7:0]	0x18	Byte 2 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA3[7:0]	0x19	Byte 3 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA4[7:0]	0x1A	Byte 4 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA5[7:0]	0x1B	Byte 5 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA6[7:0]	0x1C	Byte 6 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA7[7:0]	0x1D	Byte 7 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA8[7:0]	0x1E	Byte 8 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA9[7:0]	0x1F	Byte 9 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA10[7:0]	0x20	Byte 10 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA11[7:0]	0x21	Byte 11 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA12[7:0]	0x22	Byte 12 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA13[7:0]	0x23	Byte 13 of message in Frame Buffer 0
CEC_BUF0_RX_FRAME_DATA14[7:0]	0x24	Byte 14 of message in Frame Buffer 0

Table 32. CEC Incoming Frame Buffer 1 Registers

Register Name	CEC Map Address	Description
CEC_BUF1_RX_FRAME_HEADER[7:0]	0x54	Header of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA0[7:0]	0x55	Byte 0 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA1[7:0]	0x56	Byte 1 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA2[7:0]	0x57	Byte 2 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA3[7:0]	0x58	Byte 3 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA4[7:0]	0x59	Byte 4 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA5[7:0]	0x5A	Byte 5 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA6[7:0]	0x5B	Byte 6 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA7[7:0]	0x5C	Byte 7 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA8[7:0]	0x5D	Byte 8 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA9[7:0]	0x5E	Byte 9 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA10[7:0]	0x5F	Byte 10 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA11[7:0]	0x60	Byte 11 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA12[7:0]	0x61	Byte 12 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA13[7:0]	0x62	Byte 13 of message in Frame Buffer 1
CEC_BUF1_RX_FRAME_DATA14[7:0]	0x63	Byte 14 of message in Frame Buffer 1

Table 33. CEC Incoming Frame Buffer 2 Registers

Register Name	CEC Map Address	Description
CEC_BUF2_RX_FRAME_HEADER[7:0]	0x65	Header of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA0[7:0]	0x66	Byte 0 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA1[7:0]	0x67	Byte 1 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA2[7:0]	0x68	Byte 2 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA3[7:0]	0x69	Byte 3 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA4[7:0]	0x6A	Byte 4 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA5[7:0]	0x6B	Byte 5 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA6[7:0]	0x6C	Byte 6 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA7[7:0]	0x6D	Byte 7 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA8[7:0]	0x6E	Byte 8 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA9[7:0]	0x6F	Byte 9 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA10[7:0]	0x70	Byte 10 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA11[7:0]	0x71	Byte 11 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA12[7:0]	0x72	Byte 12 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA13[7:0]	0x73	Byte 13 of message in Frame Buffer 2
CEC_BUF2_RX_FRAME_DATA14[7:0]	0x74	Byte 14 of message in Frame Buffer 2

CEC Message Reception When Only One Frame Buffer Enabled

This section describes how messages are received and stored when only one frame buffer is enabled (default condition).

Initially, the receive buffer (Buffer 0) is empty. A message is received and stored in Receive Buffer 0, and CEC_BUF0_TIMESTAMP[1:0] is set to 0b01. If the corresponding interrupt mask bit is set, CEC_RX_RDY0_ST goes high and an interrupt is generated to alert the host processor that a message has been received. No more messages can be received until the processor reads out the received message.

The host processor responds to the interrupt (or polls the CEC_BUF0_TIMESTAMP[1:0] register), realizes a message was received, and reads Receive Buffer 0. Once the message is read, the processor sets CEC_RX_RDY0_CLR, which resets the Buffer 0 time stamp to 0b00 and also clears the Buffer 0 status bit (if applicable). The CEC module is now ready to receive the next incoming message.

Example of CEC Message Reception When All Frame Buffers Enabled

This section provides an example of how messages are received and stored, how the time stamps are generated, and what happens when the host reads a received message when all three frame buffers are enabled.

Initially all buffers are empty and all time stamps are 0b00. A message is received and stored in Receive Buffer 0. CEC_BUF0_TIMESTAMP[1:0] is set to 0b01. If the corresponding interrupt mask bit is set (CEC_RX_RDY0_MB1), CEC_RX_RDY0_ST goes high and an interrupt is generated to alert the host processor that a message was received.

Another message is received and stored in Receive Buffer 1, and CEC_BUF0_TIMESTAMP[1:0] is set to 0b10. If the corresponding interrupt mask bit is set, CEC_RX_RDY0_ST[1] goes high and an interrupt is generated to alert the host processor that a message was received.

The host processor responds to the interrupts or polls the time stamps, realizes that messages were received, and reads the three time stamps to determine which receive buffer to read first. The buffer with the earliest time stamp should be read first. Therefore, in this example, the processor should read receive Buffer 0 first. Once the message is read, the processor sets CEC_RX_RDY0_CLR, which resets the Buffer 0 time stamp to 0b00 and also clears the Buffer 0 status bit (if applicable).

Another message is received. The receiver module checks to see which of the three buffers is available, starting with Buffer 0. In this example, Buffer 0 was read out already by the host processor and is available, so the new message is stored in Receive Buffer 0. At this time, the time stamp for Receive Buffer 1 is adjusted to 0b01 to show that it contains the first received message, and a time stamp of 0b10 is assigned to Receive Buffer 0 to show that it contains the second received message. If the corresponding interrupt mask bit is set, the CEC_RX_RDY0_ST[0] bit goes high and an interrupt is generated to alert the host processor that a message was received.

Another message is received. This message is stored in Receive Buffer 2 (Buffer 0 and Buffer 1 are full). Time Stamp 0b11 is assigned to Receive Buffer 2 to show that it contains an unread message that was the third to be received. If the corresponding interrupt mask bit is set, the CEC_RX_RDY0_ST bit goes high and an interrupt is generated to alert the host processor that a message was received. At this time, all receive buffers are full and no more messages can be received until the processor reads at least one message.

The host processor responds to the interrupts or polls the time stamps, realizes that messages were received, and reads the three time stamps. The buffer with the earliest time stamp should be read first. Therefore, Receive Buffer 1 is read first, followed by Receive Buffer 0, and then Receive Buffer 2. Once the messages are read, the processor sets CLR_RX_RDY0, CLR_RX_RDY1, and CLR_RX_RDY2. The time stamps for all three buffers are reset to 0b00.

CEC_RX_RDY0_ST, IO Map, Address 0x93[3] (Read Only)

Latched status of CEC_RX_RDY0_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. When a message is received into Buffer 0, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY0_CLR.

Function

CEC_RX_RDY0_ST	Description
0	No change
1	New CEC message received in Buffer 0

CEC_RX_RDY1_ST, IO Map, Address 0x93[4] (Read Only)

Latched status of CEC_RX_RDY1_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. When a message has been received into Buffer 1, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY1_CLR.

Function

CEC_RX_RDY1_ST	Description
0	No change
1	New CEC message received in Buffer 1

CEC_RX_RDY2_ST, IO Map, Address 0x93[5] (Read Only)

Latched status of CEC_RX_RDY2_RAW signal. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit. When a message is received into Buffer 2, this bit is set. Once set, this bit remains high until the interrupt is cleared via CEC_RX_RDY2_CLR.

Function

CEC_RX_RDY2_ST	Description
0	No change
1	New CEC message received in buffer 2

ANTIGLITCH FILTER MODULE

This module is used to remove any glitches on the CEC bus, making the CEC input signal cleaner before it enters the CEC module. The glitch filter is programmable through the CEC_GLITCH_FILTER_CTRL[5:0] register. The register value specifies the minimum pulse width that is passed through by the module. Any pulses with narrower widths are rejected. There is a CEC_glitch_filter_ctrl + 1 number of clock delays introduced by the antiglitch filter.

CEC_GLITCH_FILTER_CTRL[5:0], CEC Map, Address 0x2B[5:0]

The CEC input signal is sampled by the input clock (XTAL clock). CEC_GLITCH_FILTER_CTRL specifies the minimum pulse width requirement in input clock cycles. Pulses of widths of less than the minimum specified width are considered glitches and are removed.

Function

CEC_GLITCH_FILTER_CTRL[5:0]	Description
000000	Disable the glitch filter
000001	Filter out pulses with widths of less than 1 clock cycle
000010	Filter out pulses with widths of less than 2 clock cycles
	…
000111 (Default)	Filter out pulses with widths of less than 7 clock cycles
	…
111111	Filter out pulses with widths of less than 63 clock cycles

TYPICAL OPERATION FLOW

This section describes the algorithm that should be implemented in the host processor controlling the CEC module.

Initializing CEC Module

Figure 18 shows the flow that can be implemented in the host processor controlling the ADV7630 to initialize the CEC module.

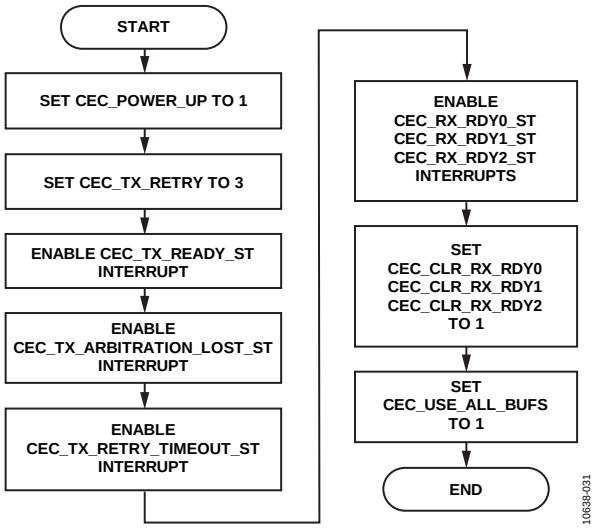


Figure 18. CEC Module Initialization

Using CEC Module as Initiator

Figure 19 shows the algorithm that can be implemented in the host processor controlling the ADV7630 to use the CEC module as an initiator.

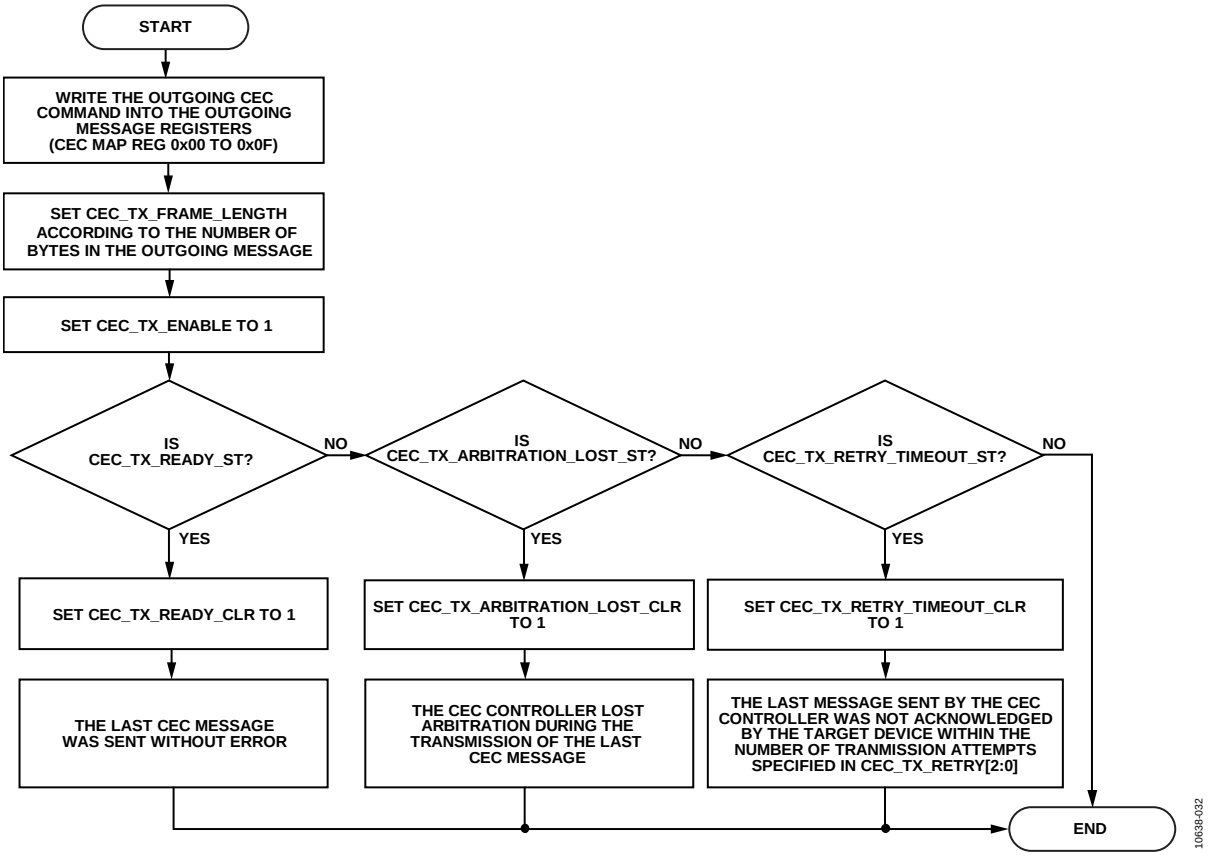


Figure 19. Using CEC Module as Initiator

Using CEC Module as Follower

Figure 20 shows the algorithm that can be implemented in the host processor controlling the ADV7630 to use the CEC module as a follower.

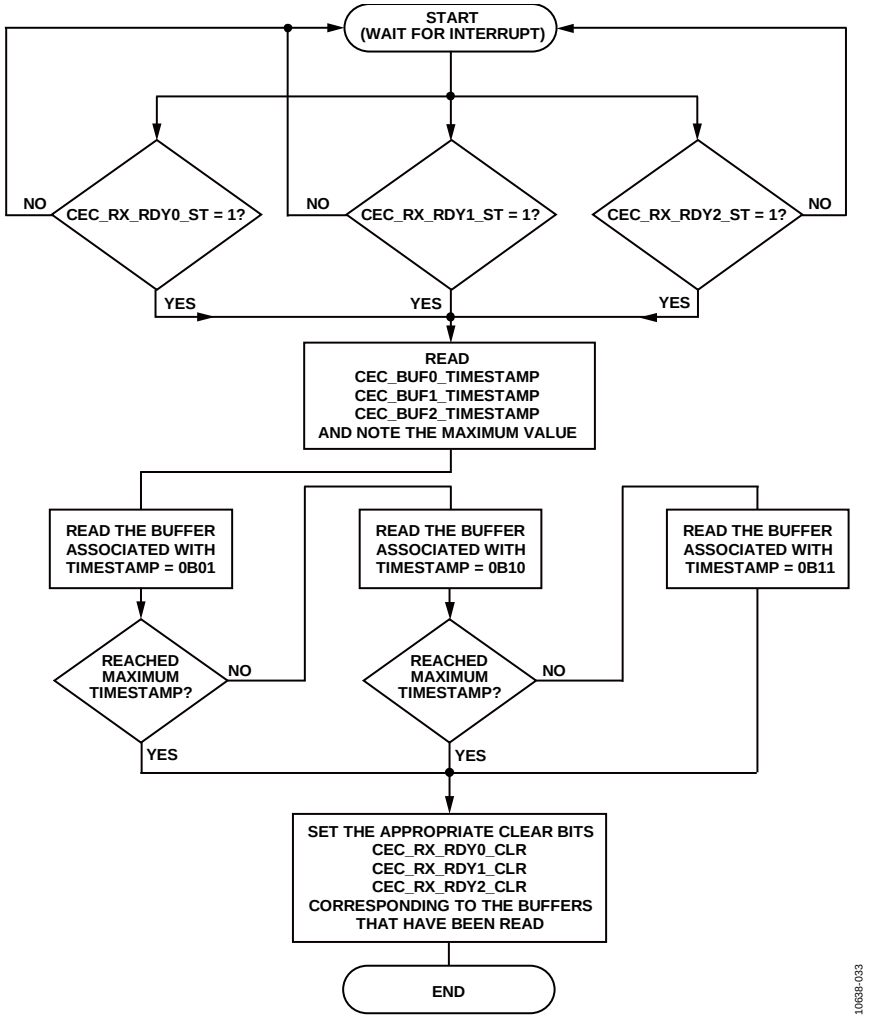


Figure 20. Using CEC Module as Follower

Low Power CEC Message Monitoring

The ADV7630 can be programmed to monitor the CEC line for messages that contain specific user-programmable opcodes. These are referred to as WAKE_OPCODEs because they allow the system to be notified if preprogrammed opcodes of interest are received, without the host processor having to check each received message.

The default values of the WAKE_OPCODE registers are detailed in the following descriptions. All of these registers can be overwritten, as required by the host processor.

For each of the eight WAKE_OPCODE registers, there is a corresponding raw flag, a status bit, and a clear bit. If one of the WAKE_OPCODEs is received, the corresponding raw flag goes high for a brief period of time. If the appropriate interrupt mask bit is set, the interrupt status bit goes high and remains high until the interrupt status is set to 1, and an interrupt is also generated (refer to Table 34).

Table 34. CEC_WAKE_OPCODE and Associated Interrupt Status and Mask Bits

WAKE_OPCODE Register	Associated Interrupt Status	Associated Interrupt Mask
CEC_WAKE_OPCODE0	CEC_CMD_INTR 0]	CEC_CMD_INTR_MASK[0]
CEC_WAKE_OPCODE1	CEC_CMD_INTR[1]	CEC_CMD_INTR_MASK[1]
CEC_WAKE_OPCODE2	CEC_CMD_INTR[2]	CEC_CMD_INTR_MASK[2]
CEC_WAKE_OPCODE3	CEC_CMD_INTR[3]	CEC_CMD_INTR_MASK[3]
CEC_WAKE_OPCODE4	CEC_CMD_INTR[4]	CEC_CMD_INTR_MASK[4]
CEC_WAKE_OPCODE5	CEC_CMD_INTR[5]	CEC_CMD_INTR_MASK[5]
CEC_WAKE_OPCODE6	CEC_CMD_INTR[6]	CEC_CMD_INTR_MASK[6]
CEC_WAKE_OPCODE7	CEC_CMD_INTR[7]	CEC_CMD_INTR_MASK[7]

CEC_CMD_INTR_MASK[7:0], TXB Main Map, Address 0x92[7:0]

This register is used to enable or disable the associated interrupt mask for the CEC_WAKE_OPCODE0 to CEC_WAKE_OPCODE7 registers.

CEC_CMD_INTR_MASK[7:0]	Description
xxxx xxx0	Disable mask for CEC_WAKE_OPCODE0
xxxx xxx1	Enable mask for CEC_WAKE_OPCODE0
xxxx xx0x	Disable mask for CEC_WAKE_OPCODE1
xxxx xx1x	Enable mask for CEC_WAKE_OPCODE1
…	…
0xxx xxxx	Disable mask for CEC_WAKE_OPCODE7
1xxx xxxx	Enable mask for CEC_WAKE_OPCODE7

CEC_CMD_INTR[7:0], TXB Main Map, Address 0x93[7:0]

This register contains the interrupt status for the CEC_WAKE_OPCODE0 to CEC_WAKE_OPCODE7 registers.

CEC_CMD_INTR_MASK	Description
xxxx xxx0	Interrupt not detected for CEC_WAKE_OPCODE0
xxxx xxx1	Interrupt detected for CEC_WAKE_OPCODE0
xxxx xx0x	Interrupt not detected for CEC_WAKE_OPCODE1
xxxx xx1x	Interrupt detected for CEC_WAKE_OPCODE1
…	…
0xxx xxxx	Interrupt not detected for CEC_WAKE_OPCODE7
1xxx xxxx	Interrupt detected for CEC_WAKE_OPCODE7

CEC_WAKE_OPCODE0[7:0], CEC Map, Address 0x78[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE0[7:0]	Description
01101101 (Default)	Reset value set to power on opcode
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE1[7:0], CEC Map, Address 0x79[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE1[7:0]	Description
10001111 (Default)	Reset value set to Give Power Status opcode
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE2[7:0], Addr 42 (CEC), Address 0x7A[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE2[7:0]	Description
10000010 (Default)	Reset value set to Active Source opcode
Xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE3[7:0], Addr 42 (CEC), Address 0x7B[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE3[7:0]	Description
00000100 (Default)	Reset value set to Image View On opcode
xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE4[7:0], Addr 42 (CEC), Address 0x7C[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE4[7:0]	Description
00001101 (Default)	Reset value set to Text View On opcode
Xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE5[7:0], Addr 42 (CEC), Address 0x7D[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE5[7:0]	Description
01110000 (Default)	Reset value set to System Audio Mode Request opcode
Xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE6[7:0], Addr 42 (CEC), Address 0x7E[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE6[7:0]	Description
01000010 (Default)	Reset value set to Deck Control opcode
Xxxxxxxx	User specified opcode to respond to

CEC_WAKE_OPCODE7[7:0], Addr 42 (CEC), Address 0x7F[7:0]

This value can be set to a CEC opcode that requires a response. On receipt of this opcode, the Rx generates an interrupt that can be used to alert the system that a CEC opcode of interest has been received and requires a response.

Function

CEC_WAKE_OPCODE7[7:0]	Description
01000001 (Default)	Reset value set to Play opcode
xxxxxxxx	User specified opcode to respond to

CEC_INTERRUPT_BYTE[7:0], IO Map, Address 0x97[7:0] (Read Only)

One of the eight preprogrammed commands received.

Function

CEC_INTERRUPT_BYTE[7:0]	Description
00	No change
01	Opcode 1 received
02	Opcode 2 received
04	Opcode 3 received
08	Opcode 4 received
10	Opcode 5 received
20	Opcode 6 received
40	Opcode 7 received
80	Opcode 8 received

CEC_INTERRUPT_BYTE_ST[7:0], IO Map, Address 0x98[7:0] (Read Only)

Function

CEC_INTERRUPT_BYTE_ST[7:0]	Description
0	No change
1	One of the eight opcodes received

CEC_INTERRUPT_BYTE_CLR[7:0], IO Map, Address 0x99[7:0] (Self-Clearing)

Function

CEC_INTERRUPT_BYTE_CLR[7:0]	Description
0 (Default)	Does not clear
1	Clears CEC_INTERRUPT_BYTE_ST

CEC_INTERRUPT_BYTE_MB1[7:0], IO Map, Address 0x9B[7:0]

Function

CEC_INTERRUPT_BYTE_MB1[7:0]	Description
0 (Default)	Masks CEC_INTERRUPT_BYTE_ST
1	Unmasks CEC_INTERRUPT_BYTE_ST

The ADV7630 has a comprehensive set of interrupt registers located in the IO Map for the Rx section and Main Maps for the TXA and TXB sections. The ADV7630 features three interrupt controllers. One controller handles interrupts for the Rx section, while the other two controllers handle interrupts from the TXA and TXB sections. The signal outputs of the Rx and TX interrupt controllers are or'ed together. The resulting combination of the Rx and Tx interrupt controllers is provided externally via the INT interrupt pin.

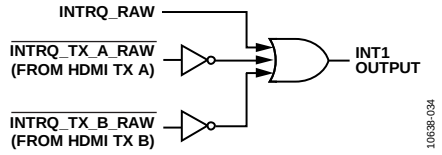


Figure 21. Interrupts Controller Outputs

INTERRUPT SIGNAL CONFIGURATION

Interrupt Duration

The interrupt duration of the INT interrupt signal can be controlled via the INTRQ_DUR_SEL control.

INTRQ_DUR_SEL[1:0], IO Map, Address 0x40[7:6]

A control to select the interrupt signal duration for the INT1 interrupt signal.

Function

INTRQ_DUR_SEL[1:0]	Description
0 (Default)	4 CLK_IN periods
1	16 CLK_IN periods
2	64 CLK_IN periods
3	Active until cleared

Interrupt Drive Level

The drive level of the INT interrupt signal can be controlled via the INTRQ_OP_SEL control.

INTRQ_OP_SEL[1:0], IO Map, Address 0x40[1:0]

Interrupt signal configuration control for INT1.

Function

INTRQ_OP_SEL[1:0]	Description
00 (Default)	Open drain
01	Drives low when active
10	Drives high when active
11	Disabled

Interrupt Manual Assertion

It is possible to manually generate an interrupt on the INT pin by setting MPU_STIM_INTRQ**.** This feature is designed for debug use and not intended for use in normal operation. The appropriate mask bit must be set to generate an interrupt at the pin.

MPU_STIM_INTRQ, IO Map, Address 0x40[2]

Manual interrupt set control. This feature should be used for test purposes only. Note that the appropriate mask bit must be set to generate an interrupt at the pin.

Function

MPU_STIM_INTRQ	Description
0 (Default)	Disables manual interrupt mode
1	Enables manual interrupt mode

MPU_STIM_INTRQ_MB1, IO Map, Address 0x4B[7]

INT1 interrupt mask for manual forced interrupt signal. When set, the manual forced interrupt triggers the INT1 interrupt and MPU_STIM_INTRQ_ST indicates the interrupt status.

Function

MPU_STIM_INTRQ_MB1	Description
0 (Default)	Disables manual forced interrupt for INT1
1	Enables manual forced interrupt for INT1

INTERRUPT SOURCE

Whenever the interrupt output pin activates, it is possible to determine which of the two interrupt controllers has activated via INTRQ_RAW, INTRQ_TX_A_RAW, and INTRQ_TX_B_RAW.

Note: The output of any two or all three interrupt controllers may activate simultaneously with the related interrupts status set to 1.

INTRQ_RAW, IO Map, Address 0x3F[0] (Read Only)

Status of the interrupt signal from HDMI RX. If an interrupt event that has been enabled for the HDMI Rx has occurred, this bit is set to 1. Interrupts for HDMI Rx are set via the Interrupt 1 mask bits. This bit remains set to 1 until all status for interrupts enabled on HDMI Rx are cleared.

Function

INTRQ_RAW	Description
0	No interrupt on HDMI Rx
1	An interrupt event for HDMI Rx has occurred

INTRQ_TX_A_RAW, IO Map, Address 0x3F[1] (Read Only)

Status of the interrupt signal from HDMI TX A. If an interrupt event that has been enabled for the HDMI TX A has occurred, this bit is set to 0. Interrupts for HDMI TX A are set via the Interrupt 1 mask bits. This bit remains set to 0 until all status for interrupts enabled on HDMI TX A are cleared.

Function

INTRQ_TX_A_RAW	Description
0	An interrupt event for Tx A has occurred
1	No interrupt on Tx A

INTRQ_TX_B_RAW, IO Map, Address 0x3F[2] (Read Only)

Status of the interrupt signal from HDMI TX B. If an interrupt event that has been enabled for the HDMI TX B has occurred, this bit is set to 0. Interrupts for HDMI TX B are set via the Interrupt 1 mask bits. This bit remains set to 0 until all status for interrupts enabled on HDMI TX B are cleared.

Function

INTRQ_TX_B_RAW	Description
0	An interrupt event for Tx B has occurred
1	No interrupt on Tx B

RX CONTROLLER

This section describes the interrupt support provided by the interrupt controller of the Rx section.

Interrupt Architecture Overview

The interrupt architecture of the Rx section provides the following four different types of bits:

- Raw bits
- Status bits
- Interrupt mask bits
- Clear bits

Raw bits are defined as being either edge-sensitive or level-sensitive.

CABLE_DET_A_RAW, IO Map, Address 0x6F[3] (Read Only)

Raw status of Port A 5 V cable detection signal.

Function

CABLE_DET_A_RAW	Description
0	No cable detected on Port A
1	Cable detected on Port A (high level on RXA_5V)

AKSV_UPDATE_A_RAW, IO Map, Address 0x88[3] (Read Only)

Status of Port A AKSV Update interrupt signal. When set to 1, it indicates that the transmitter has written its AKSV into the HDCP registers for Port A. Once set, this bit remains high until it is cleared via AKSV_UPDATE_A_CLR.

Function

AKSV_UPDATE_A_RAW	Description
0	No AKSV updates on Port A
1	Detected a write access to the AKSV register on Port A

In the case of CABLE_DET_A_RAW, this bit always represents the current status of whether or not the part's 5 V signal detection for HDMI Rx Port A is high. It is not a latched bit and never requires clearing. This is the definition of a level-sensitive raw bit.

In the case of AKSV_UPDATE_A_RAW, the same strategy does not work. If the AKSV_UPDATE_A_RAW bit were to behave in the same way as CABLE_DET_A_RAW, it would go high at the instant the part receives an AKSV update from the upstream source and would go low again some clock cycles afterwards. Having a raw bit that is held high for only an instant is not useful. Therefore, with these types of events, the raw bit is latched and must be cleared by the corresponding clear bit. Accordingly, the raw bit does not truly represent the current status; instead, it represents the status of an edge event that happened in the past. This is the definition of an edge-sensitive raw bit.

All raw bits, with the exception of INTRQ_RAW, have corresponding status bits. The status bits always work in the same manner, whether the raw bit is edge-sensitive or level-sensitive. Status bits have the following characteristics:

- A status bit must be enabled by setting the corresponding interrupt mask bit.
- Status bits are always latched bits and must be cleared by the corresponding clear bit.

If the interrupt mask bit for a given interrupt is set and that raw bit changes state, the corresponding status bit goes high and an interrupt is generated. The status bit must be cleared using the appropriate clear bit. The status bits, interrupt mask bitsm and clear bits for CABLE_DET_A_RAW and AKSV_UPDATE_A_RAW are described in this section.

CABLE_DET_A_ST, IO Map, Address 0x70[3] (Read Only)

Latched status for Port A 5 V cable detection interrupt signal. Once set, this bit remains high until the interrupt is cleared via CABLE_DET_A_CLR. This bit is valid only if enabled via the corresponding INT1 interrupt mask bit.

Function

CABLE_DET_A_ST	Description
0	CABLE_DET_A_RAW has not changed. Interrupt has not been generated from this register.
1	CABLE_DET_A_RAW has changed. Interrupt has been generated from this register.

CABLE_DET_A_CLR, IO Map, Address 0x71[3] (Self-Clearing)

Clear bit for Port A 5 V cable detection interrupt signal.

Function

CABLE_DET_A_CLR	Description
0 (default)	Does not clear
1	Clears CABLE_DET_A_ST

CABLE_DET_A_MB1, IO Map, Address 0x73[3]

INT1 interrupt mask for Port A 5 V cable detection interrupt. When set, the Port A 5 V cable detection interrupt triggers the INT1 interrupt and CABLE_DET_A_ST indicates the interrupt status.

Function

CABLE_DET_A_MB1	Description
0 (Default)	Disables Port A +5 V Cable Detection interrupt for INT1
1	Enables Port A +5 V Cable Detection interrupt for INT1

AKSV_UPDATE_A_ST, IO Map, Address 0x89[3] (Read Only)

Latched status of Port A AKSV Update Interrupt. Once set, this bit remains high until the interrupt has been cleared via AKSV_UPDATE_A_CLR. This bit is valid only if enabled via corresponding the INT1 interrupt mask bit.

Function

AKSV_UPDATE_A_ST	Description
0	No AKSV updates on Port A
1	Detected a write access to the AKSV register on Port A

AKSV_UPDATE_A_CLR, IO Map, Address 0x8A[3] (Self-Clearing)

Clear bit for the Port A AKSV Update Interrupt.

Function

AKSV_UPDATE_A_CLR	Description
0 (Default)	Does not clear
1	Clears AKSV_UPDATE_A_ST

AKSV_UPDATE_A_MB1, IO Map, Address 0x8C[3]

INT1 interrupt mask for Port A AKSV Update interrupt. When set, the Port A AKSV Update interrupt triggers the INT1 interrupt and AKSV_UPDATE_A_ST indicates the interrupt status.

Function

AKSV_UPDATE_A_MB1	Description
0 (Default)	Disable Port A AKSV Update interrupt on INT1
1	Enable Port A AKSV Update interrupt on INT1

Figure 22 and the example timing figures (Figure 23 and Figure 24) provide a graphical example.

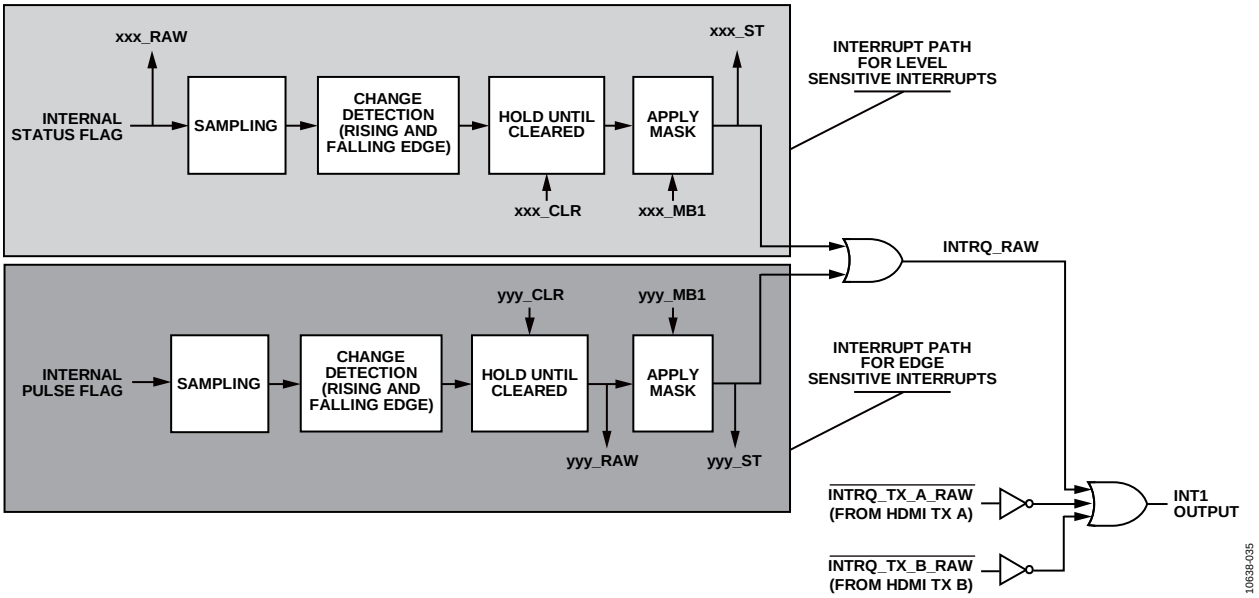


Figure 22. Level- and Edge-Sensitive Raw, Status, and Interrupt Generation

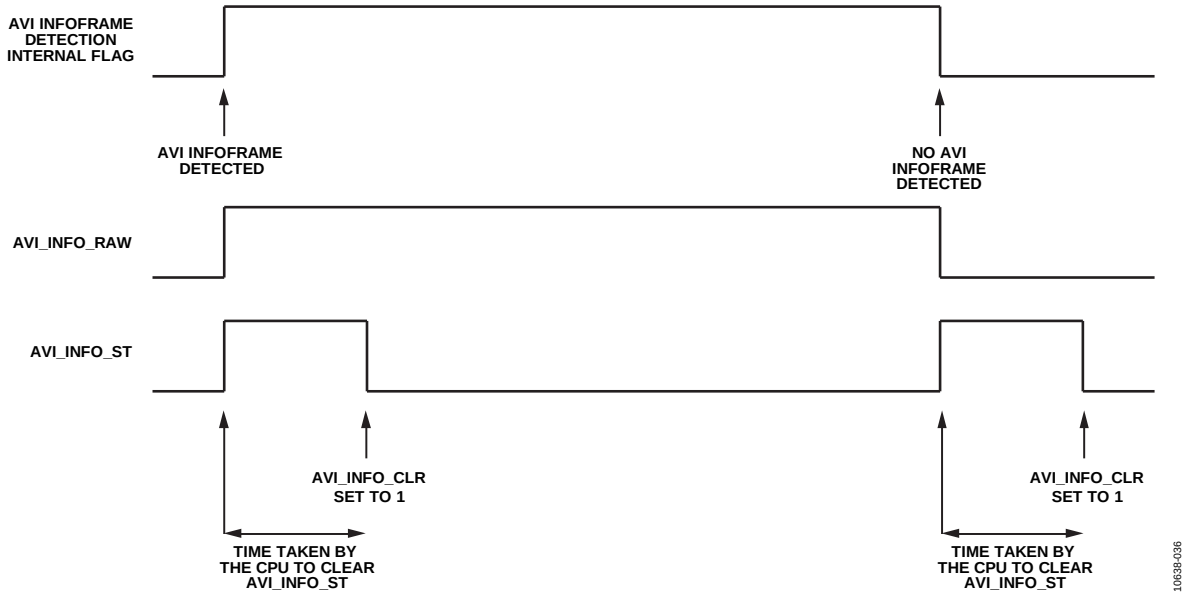


Figure 23. CABLE_DET_A_RAW and CABLE_DET_A_ST Timing

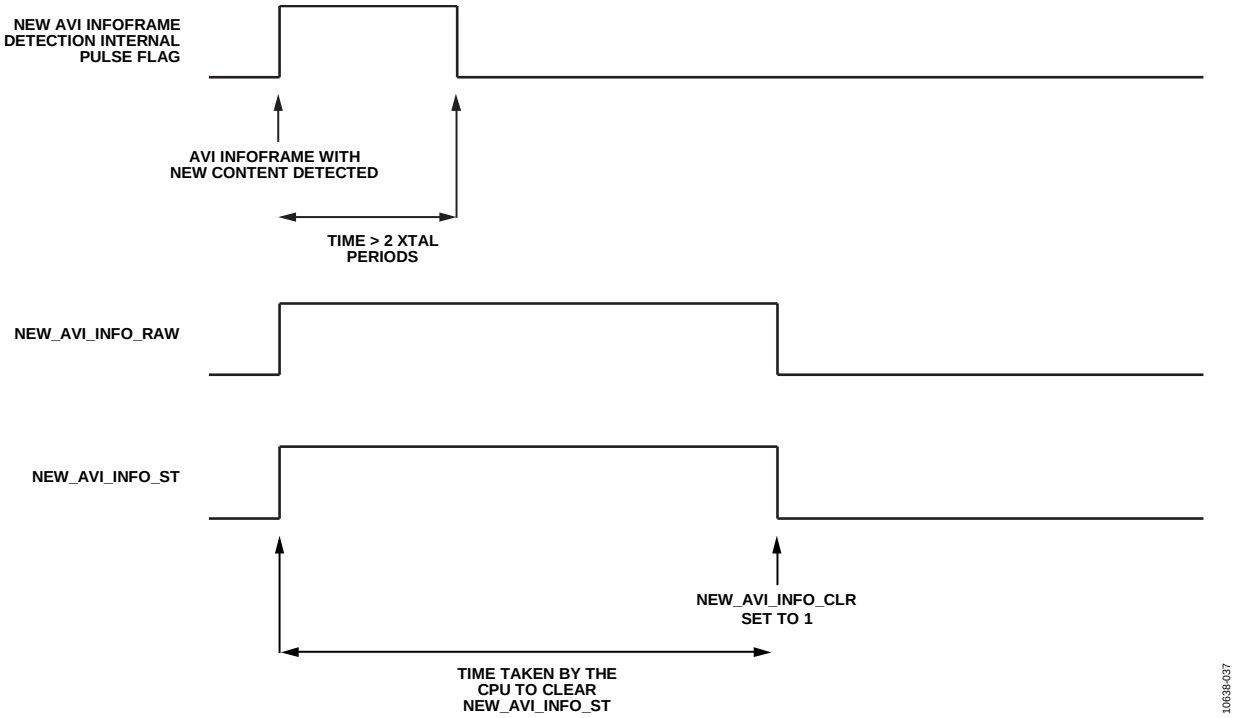


Figure 24. AKSV_UPDATE_A_RAW and AKSV_UPDATE_A_ST Timing

In this section, all raw bits are classified as being triggered by either level-sensitive or edge-sensitive events, with the following understanding of the terminology:

- **Level-sensitive events**:
  Events that are generally either high or low and are not expected to change rapidly. The raw bit for level-sensitive events is not latched and, therefore, always represents the true real-time status of the event in question.
- **Edge-sensitive events**:
  Events that exist for only an instant. The raw bits for edge-sensitive events are latched and, therefore, represent the occurrence of an edge-sensitive event that happened in the past. Raw bits for edge-sensitive events must be cleared by the corresponding clear bit.

Multiple Interrupt Events

If an interrupt event occurs and then a second interrupt event occurs before the system controller has cleared or masked the first interrupt event, the ADV7630 does not generate a second interrupt signal. The system controller should check all unmasked interrupt status bits because more than one may be active.

Description of Interrupt Bits

This section lists all the raw bits in the IO Map of the ADV7630 by category and states whether the bit is an edge-sensitive or level-sensitive bit. A basic explanation for each bit is provided in the ADV7630 Software Manual and/or in the corresponding section of this manual. For certain interrupts that require additional explanations, these are provided in the following sections of this chapter.

The following raw bits are all based on level-sensitive events; therefore, it is not necessary to clear these bits.

- TMDSPLL_LCK_A_RAW
- TMDSPLL_LCK_B_RAW
- TMDSPLL_LCK_C_RAW
- TMDSPLL_LCK_D_RAW
- TMDS_CLK_A_RAW
- TMDS_CLK_B_RAW
- TMDS_CLK_C_RAW
- TMDS_CLK_D_RAW
- HDMI_ENCRPT_A_RAW
- HDMI_ENCRPT_B_RAW
- HDMI_ENCRPT_C_RAW
- HDMI_ENCRPT_D_RAW
- CABLE_DET_A_RAW
- CABLE_DET_B_RAW
- CABLE_DET_C_RAW
- CABLE_DET_D_RAW

The following raw bits are all based on edge-sensitive events; therefore, it is necessary to clear these bits using the corresponding clear bit.

- NEW_TMDS_FRQ_RAW
- AKSV_UPDATE_A_RAW
- AKSV_UPDATE_B_RAW
- AKSV_UPDATE_C_RAW
- AKSV_UPDATE_D_RAW
- VCLK_CHNG_RAW
- BG_MEAS_DONE_RAW
- RI_EXPIRED_A_RAW
- RI_EXPIRED_B_RAW
- RI_EXPIRED_C_RAW
- RI_EXPIRED_D_RAW

Additional Explanations

HDMI Interrupts Validity Checking Process

All HDMI interrupts have a set of conditions that must be taken into account for validation in the display firmware. When the ADV7630 interrupts the display controller for an HDMI interrupt, the host must check that all validity conditions for that interrupt are met before processing that interrupt.

For simplicity, HDMI interrupts can be subdivided into two groups, as listed in the following sections.

Group 1 HDMI Interrupts

The interrupts listed in Table 35 are always valid.

Table 35. Group 1 HDMI Interrupts

Interrupts
TMDS_CLK_A_RAW
TMDS_CLK_B_RAW
TMDS_CLK_C_RAW
TMDS_CLK_D_RAW
TMDSPLL_LCK_A_RAW (TMDSPLL_LCK_A_RAW is valid if, and only if, TMDS_CLK_A is set to 1)
TMDSPLL_LCK_B_RAW (TMDSPLL_LCK_B_RAW is valid if, and only if, TMDS_CLK_B is set to 1)
TMDSPLL_LCK_C_RAW (TMDSPLL_LCK_C_RAW is valid if, and only if, TMDS_CLK_C is set to 1)
TMDSPLL_LCK_D_RAW (TMDSPLL_LCK_D_RAW is valid if, and only if, TMDS_CLK_D is set to 1)
AKSV_UPDATE_A_RAW
AKSV_UPDATE_B_RAW
AKSV_UPDATE_C_RAW
AKSV_UPDATE_D_RAW

Group 2 HDMI Interrupts

The interrupts listed in Table 36 are valid under the following conditions:

- TMDS_CLK_A_RAW is set to 1 if Port A is the active primary HDMI port.
- TMDS_CLK_B_RAW is set to 1 if Port B is the active primary HDMI port.
- TMDS_CLK_C_RAW is set to 1 if Port C is the active primary HDMI port.
- TMDS_CLK_D_RAW is set to 1 if Port D is the active primary HDMI port.

Table 36. Group 2 HDMI Interrupts

Interrupts
VCLK_CHNG_RAW
NEW_TMDS_FRQ_RAW
ISRC2_PCKT_RAW
ISRC1_PCKT_RAW
ACP_PCKT_RAW
VS_INFO_RAW
MS_INFO_RAW
SPD_INFO_RAW
AUDIO_INFO_RAW
AVI_INFO_RAW
AV_MUTE_RAW
GEN_CTL_PCK_RAW
GAMUT_MDATA_RAW
HDMI_MODE
HDMI_ENCRPT_A_RAW
HDMI_ENCRPT_B_RAW
HDMI_ENCRPT_C_RAW
HDMI_ENCRPT_D_RAW

Interrupts
NEW_ISRC2_PCKT_RAW
NEW_ISRC2_PCKT_RAW
NEW_ACP_PCKT_RAW
NEW_VS_INFO_RAW
NEW_MS_INFO_RAW
NEW_SPD_INFO_RAW
NEW_MS_INFO_RAW
NEW_AUDIO_INFO_RAW
NEW_AVI_INFO_RAW
PCKT_ERROR_RAW
NEW_GAMUT_MDATA
RI_EXPIRED_A_RAW
RI_EXPIRED_B_RAW
RI_EXPIRED_C_RAW
RI_EXPIRED_D_RAW

Storing Mask Interrupts

STORE_UNMASKED_IRQS, IO Map, Address 0x40[4]

This bit allows the HDMI status flags for any HDMI interrupt to be triggered, regardless of whether the mask bits are set. It allows an HDMI interrupt to trigger and allows this interrupt to be read back through the corresponding status bit without triggering an interrupt on the interrupt pin. The status is stored until the clear bit is used to clear the status register and allows another interrupt to occur.

Function

STORE_UNMASKED_IRQS	Description
0 (Default)	Does not allow x_ST flag of any HDMI interrupt to be set independently of mask bits
1	Allows x_ST flag of any HDMI interrupt to be set independently of mask bits

TX SECTIONS

This section describes the interrupt support provided by the interrupt controller of the TX sections, TXA and TXB. It should be noted that in most of this section about the TXA and TXB HDMI transmitters, references to TXA also apply to TXB. Unless stated otherwise, the same register bits and controls that are shown in Table 25 apply to both transmitters and should be treated accordingly.

Architecture Overview

The interrupt architecture of the TXA section provides the following two different types of bits:

- Interrupt bits
- Interrupt mask bits

The interrupt bits are used to notify that a specific event has occurred or is active. When an interrupt bit becomes active, it is set to 1 until the user clears the corresponding clear bit by setting it to 1. The description of a TXA interrupt bit is provided for HPD_ST. The complete list of interrupt bits available for the TXA section is provided in Table 26 and Table 27.

HPD_ST, TXA Main Map, Address 0x96[7]

Interrupt for Hot Plug detection.

Function

HPD_ST	Description
0 (default)	No interrupt detected
1	Interrupt detected

The interrupts mask bits are used to activate selectively any interrupt bits on the interrupt output of the TXA interrupt controller. The output of a TXA interrupt controller activates when one or more interrupts bits are set, and their corresponding interrupt mask bits are also set. Note that any given mask bit does not affect its corresponding interrupt bit but, instead, affects only the level on the TXA interrupt controller.

HPD_INTR_MASK, TXA Main Map, Address 0x94[7]

Mask for HPD_ST.

Table 37 and Table 38 list all the interrupt mask bits available for the TXA section.

Table 37. HDMI TXA Interrupt Mask Bits in TXA Main Map, Register 0x94

Bit Name	Bit Position	Associated Interrupt Bit
RI_RDY_INTR_MASK	0 (LSB)	RI_RDY_ST
HDCP_CONTROLLER_STATE_4_INTR_MASK	1	HDCP_CONTROLLER_STATE_4_ST
EDID_RDY_INTR_MASK	2	EDID_RDY_ST
VS_INTR_MASK	5	VS_ST
MSEN_INTR_MASK	6	MSEN_ST
HPD_INTR_MASK	7 (MSB)	HPD_ST

Table 38. HDMI TXA Interrupt Bits in TXA Main Map, Register 0x95

Bit Name	Bit Position	Associated Interrupt Bit
BKSV_FLAG_INTR_MASK	6	BKSV_FLAG_ST
HDCP_ERROR_INTR_MASK	7 (MSB)	HDCP_ERROR_ST

REGISTER ACCESS AND SERIAL PORTS DESCRIPTION

The ADV7630 has seven 2-wire serial (I²C compatible) ports:

- One main I²C port, SDA/SCL, which allows a system I²C master controller to control and configure the ADV7630.
- Four I²C ports for the receiver section, DDC Port A, Port B, Port C, and Port D via which an HDMI host can access the internal HDCP registers.
- Two I²C port for the transmitter section, TXA_DDC and TXB_DDC ports, via which the HDMI transmitters can access the HDCP registers of downstream sink devices.

MAIN I²C PORT

Register Access

The ADV7630 has twelve 256-byte maps that can be accessed via the main I²C ports, SDA and SCL. Each map has its own I²C address and acts as a standard slave device on the I²C bus.

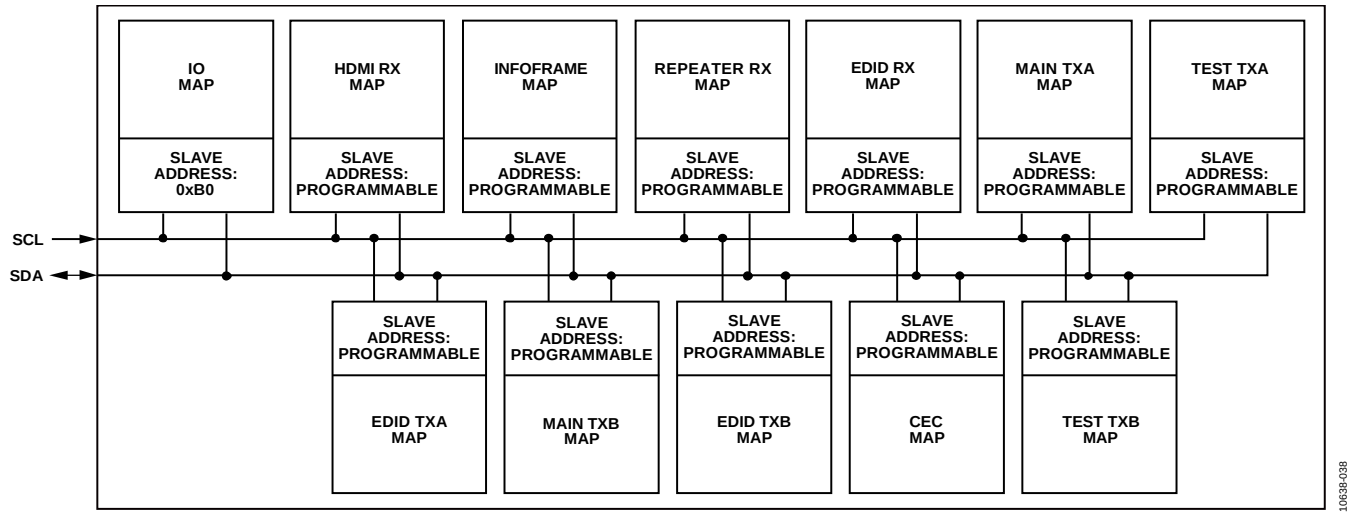


Figure 25. ADV7630 Register Map Access Through Main I²C Port

Eleven of the 12 maps have a programmable I²C address. This facilitates the integration of the ADV7630 in systems that have multiple slaves on the general I²C bus.

Table 39. Register Maps and I²C Addresses

Map	Default Address	Programmable Address	Location at Which Address can be Programmed
IO	0xB0	Not programmable	Not applicable
HDMI Rx	0x00	Programmable	IO Map, Register 0xFB
InfoFrame Rx	0x00	Programmable	IO Map, Register 0xF5
Repeater Rx	0x00	Programmable	IO Map, Register 0xF9
EDID Rx	0x00	Programmable	IO Map, Register 0xFA
Main TXA	0x00	Programmable	IO Map, Register 0xEE
Test TXA	0x00	Programmable	IO Map, Register 0xF1
EDID TXA	0x00	Programmable	IO Map, Register 0xF0
Main TXB	0x00	Programmable	IO Map, Register 0xEA
EDID TXB	0x00	Programmable	IO Map, Register 0xEC
CEC Map	0x00	Programmable	IO Map, Register 0xF4
Test TXB	0x00	Programmable	IO Map, Register 0xED

Protocol for Main I²C Port

The system controller initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This transition indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (7-bit address and R/W bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition.

In the idle condition, the device monitors the SDA and SCL lines for the start condition and the correct transmitted address. The R/W bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. A Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

Each of the ADV7630 maps acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/W bit. It interprets the first byte as the map address and the second byte as the starting subaddress. The subaddresses auto increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, an immediate jump to the idle condition occurs. During a given SCL high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7630 does not issue an acknowledge and returns to the idle condition.

If the user exceeds the highest subaddress in auto increment mode, the following actions are taken:

- In read mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register. A no acknowledge is issued by the ADV7630 and the part returns to the idle condition.

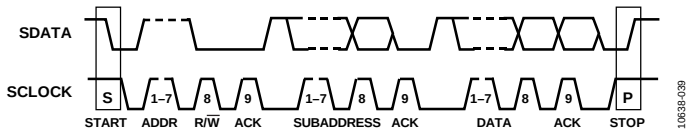


Figure 26. Bus Data Transfer

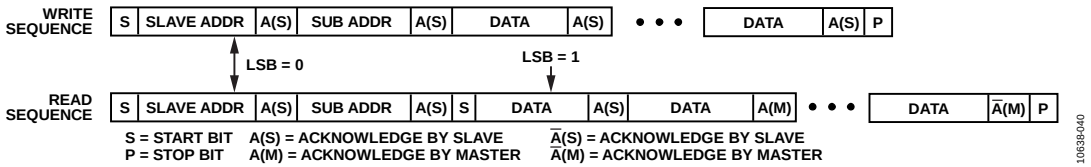


Figure 27. Read and Write Sequence

HDMI RECEIVER DDC PORTS

Four I²C ports, one for each of the HDMI receivers ports (Port RxA, Port RxB, Port RxC and Port RxD), allow an HDMI host to access the HDCP registers of the HDMI receiver. Note that the DDC ports are 5 V tolerant, which simplifies the hardware between the HDMI connector and the ADV7630.

I²C Protocols for Access to the HDCP

An I²C master connected on a DDC port can access the internal HDCP, using the following protocol:

- Write sequence, as defined in the Protocol for Main I2C Port section.
- Read sequence, as defined in the Protocol for Main I2C Port section.
- Current address read sequence, which allows the master on the DDC port to read access HDCP registers without specifying the subaddress that must be read. The ADV7630 stores an address counter for each DDC port that maintains the value of the subaddress that was last accessed. The address counter is incremented by 1 each time a read or a write access is requested on the DDC port.

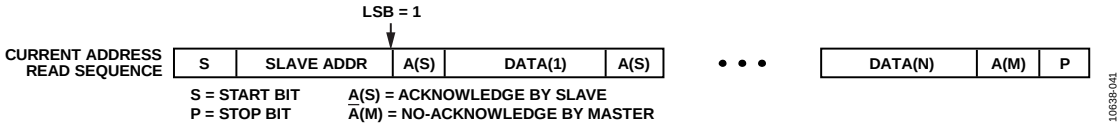


Figure 28. Current Address Read Sequence

I²C Protocols for Access to HDCP Registers

An I²C master connected on a DDC port can access the HDCP registers using the following protocol:

- Write sequence, as defined in the Protocol for Main I2C Port section
- Read sequence, as defined in the Protocol for Main I2C Port section
- Short read format, as defined in the High-bandwidth Digital Content Protection (HDCP) System Specifications

DDC Port A

The DDC lines of the HDMI port RxA comprise the DDCA_SCL and DDCA_SDA pins. An HDMI host connected to the DDC Port A accesses the HDCP registers at address 0x74 in read/write mode (refer to Figure 29).

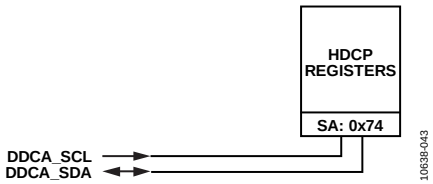


Figure 29. HDCP Registers Access from Port A

Refer to the *High-Bandwidth Digital Content Protection (HDCP) System Specifications* for detailed information about the HDCP registers.

DDC Port B

The DDC lines of the HDMI Port RxB comprise the DDCB_SCL and DDCB_SDA pins. A HDMI host connected to the DDC Port B accesses the HDCP registers at Address 0x74 in read/write mode (refer to Figure 30).

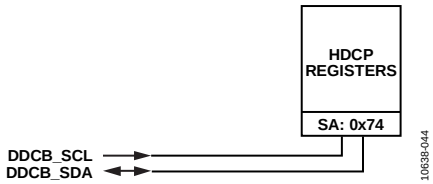


Figure 30. HDCP Registers Access from Port B

Refer to the *High-bandwidth Digital Content Protection (HDCP) System Specifications* for detailed information on the HDCP registers.

DDC Port C

The DDC lines of the HDMI Port RxC comprise the DDCC_SCL and DDCC_SDA pins. A HDMI host connected to the DDC Port RxC accesses the HDCP registers at Address 0x74 in read/write mode (refer to Figure 31).

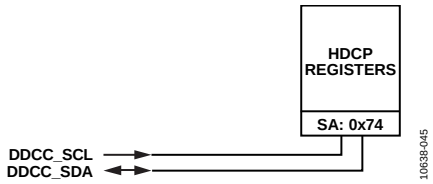


Figure 31. HDCP Registers Access from Port C

Refer to the *High-bandwidth Digital Content Protection (HDCP) System Specifications* for detailed information on the HDCP registers.

DDC Port D

The DDC lines of the HDMI Port RxD comprise the DDCD_SCL and DDCD_SDA pins. A HDMI host connected to the DDC Port D accesses the HDCP registers at address 0x74 in read/write mode (refer to Figure 32).

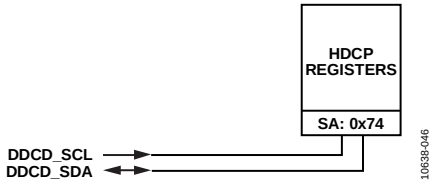


Figure 32. HDCP Registers Access from Port D

Refer to the *High-bandwidth Digital Content Protection (HDCP) System Specifications* for detailed information on the HDCP registers.

HDMI TRANSMITTER DDC PORTS

The ADV7630 features two I²C ports, one for each of the HDMI output ports that allow the ADV7620 to access the E-EDID and HDCP register of the downstream sink it interfaces with.

DDC Port TxA

One I²C port, TXA, allows the HDMI TXA transmitter to access the HDCP registers of an attached HDMI sink. Note that the DDC ports are 5 V tolerant, which simplifies the hardware between the HDMI connector and the ADV7630.

DDC Port TxB

One I²C port, TXB, allows the HDMI TXB transmitter to access the HDCP registers of an attached HDMI sink. Note that the DDC ports are 5 V tolerant, which simplifies the hardware between the HDMI connector and the ADV7630.

APPENDIX A

PRINTED CIRCUIT BOARD (PCB) LAYOUT RECOMMENDATIONS

The ADV7630 is a high precision, high speed device. To achieve maximum performance from the part, it is important to have a well laid out PCB. The following sections are a guide for designing a board using the ADV7630.

POWER SUPPLY BYPASSING

It is recommended that each power supply pin be bypassed with a 0.1 µF and a 10 nF capacitor, where possible. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. The power connection should not be made between the capacitor and the power pin. Generally, the best approach is to place a via underneath the 100 nF capacitor pads down to the power plane (refer to Figure 33).

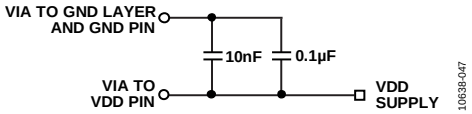


Figure 33. Recommended Power Supply Decoupling

It is particularly important to maintain low noise and good stability of the PVDD (the clock generator supply). Abrupt changes in the PVDD supply can result in similarly abrupt changes in the sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated or heavily filtered supplies for each of the analog circuitry groups (CVDD, TVDD, and PVDD).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical synchronization periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which, in turn, can produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PVDD, from a different, cleaner power source, for example, from a 12 V supply.

It is also recommended that a single ground plane be used for the entire board. Repeatedly, experience has shown that noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

APPENDIX B
PACKAGE OUTLINE DRAWING

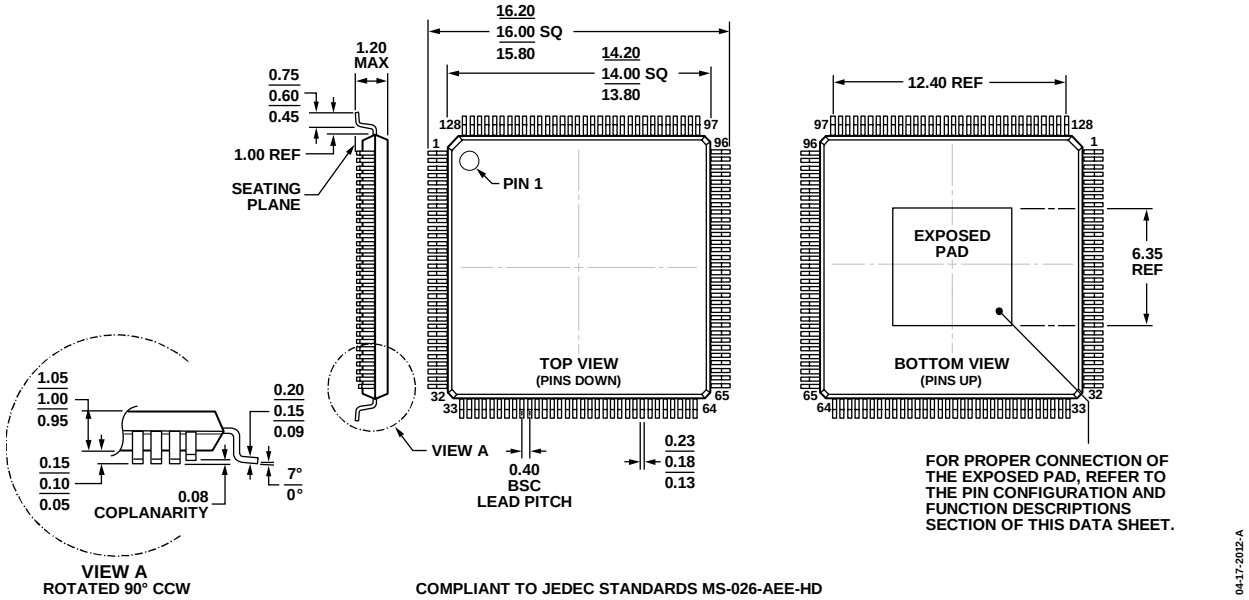


Figure 34. 128-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-128-1)
Dimensions are shown in millimeters

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG10638-0-10/12(0)

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