

Low-Power IC Digitizes 300 MHz IF

*Flexible IF digitizer has up to
270 kHz BW with >90 dB dynamic range*

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SUPERHETERODYNE receivers achieve high dynamic range, but typically require more power and are more complex than lower-performance direct conversion receivers. The AD9874 IF-digitizing IC eliminates this barrier by integrating all the blocks except the VCOs needed for IF-to-digital conversion in a narrowband superheterodyne receiver. This high level of integration is provided by a small device with low power consumption, without compromising dynamic range.

Designers of next-generation digital radio communications systems are faced with many challenges as they strive to advance the state of the art in mobile radio systems. These challenges culminate in finding unique ways to reduce power consumption, physical size and equipment cost, while increasing performance, functionality and multi-mode configurability. A key strategy for achieving these goals is *smart partitioning*, namely determining the best system structure given power, performance and time constraints. Should a traditional superheterodyne receiver or a direct RF or IF solution be used? Is an analog or a digital quadrature modulation scheme better? What is the distribution of analog and digital filtering in the RF strip? The answers to these questions depend on the specific application requirements and on the capabilities of available components.

For example, police, fire and ambulance services rely on radio communications to coordinate their daily operations. In these applications the radio is a life-saving device which must meet the highest standards of reliability and performance. Private mobile radio (PMR) encompasses the above mission-critical applications as well as taxi, delivery and security services, which also demand high-performance radios in order to maximize coverage. PMR applications require components for

three main platforms: handsets, mobile units (in vehicles) and basestations. PMR handsets require ultra low power to maximize operating time, but PMR basestations emphasize linearity and dynamic range in order to maximize network performance. In next-generation cellular basestations, smaller size, lower power and lower costs are driving reasons for redesign. GSM basestation designers are seeking ways to achieve these advancements while maintaining the overall integrity of the system. The AD9874 takes a novel approach to partitioning the IF strip of a narrowband radio receiver that helps designers meet their power, size and cost goals while achieving high dynamic range.

The superheterodyne receiver, an example of which is illustrated in Figure 1, is a popular architecture known for high dynamic range. The implementation shown avoids quadrature analog downconversion to baseband by using filtering together with multiple analog downconversion operations, thereby side-stepping troublesome issues associated with quadrature analog downconversion and low-frequency analog signal processing. Constructing such a receiver is complicated by the need to find a good frequency-plan and the need to deal with a multitude of sub-blocks.

The AD9874 simplifies the design problem by inte-

grating the bulk of the radio's back-end into a single IC whose performance is guaranteed by the manufacturer. The designer is spared the need for numerous prototypes because all interface, spur and coupling issues are either solved or at least understood in advance. Furthermore, since the input IF frequency range of the AD9874 is very broad and since all modulation-specific functions are delegated to a digital signal processor (DSP), the AD9874 can be used to make a reusable or even reconfigurable radio platform. The integration of key analog blocks with the right amount of digital filtering and control is the essence of smart partitioning.

The dynamic range of a radio is primarily a function of three key parameters. The first is its noise figure (NF), which is the ratio of the input-referred noise power to the thermal noise limit (-174 dBm/Hz, or $0.5nV/\sqrt{\text{Hz}}$ in a 50Ω system). A sensitive receiver such as that found in a basestation might have a NF of only a few dB. Given the NF and signal bandwidth, a system designer can calculate the signal-to-noise ratio (SNR) as a function of the signal power, and vice versa. For example, if a receiver with NF=3 dB and a signal bandwidth of 10 kHz needs 6 dB SNR to detect an input with acceptable fidelity or bit-error-rate, the sensitivity limit of the receiver is

$$-174 + 10\log_{10}(10 \times 10^3) + 3 + 6 = -125\text{dBm},$$

or about $0.12\mu V_{\text{rms}}$ in a 50Ω system.

The second key parameter affecting the dynamic range of a receiver is its linearity. Linearity can be

described in several ways, but the most common linearity specification in an analog receive chain is the third-order input intercept point (IIP3). IIP3 is the extrapolated input power needed by two tones in order to produce a third-order intermodulation product equal in height to those two tones. From the IIP3 specification and the characteristic 3 dB/dB slope of third-order distortion, a system designer can calculate the tolerable blocker amplitude for two-tone interference. For example, if a receiver with $IIP3 = -10$ dBm experiences a 3 dB loss in sensitivity when the effective in-band interference is -130 dBm, then a low-level desired signal 3 dB above sensitivity could be received in the presence of two tones whose powers were as large as

$$P_{in} = IIP_3 - \left(\frac{IIP_3 - IM_3}{3} \right) \\ = -10 - \frac{-10 + 130}{3} = -50\text{dBm}$$

In the context of a system employing a hard-limiting element such as an ADC, another consideration is the input level which results in clipping. The *instantaneous dynamic range* (IDR) of a receiver is the ratio between the power of a single interferer which causes sensitivity degradation and the sensitivity limit, and is measured with all automatic gain control (AGC) circuits set at minimum attenuation. IDR expresses the receiver's ability to cope with a single large interferer and is as or more important a measure of receiver linearity as IIP3 when an ADC is part of the signal chain. After all, it is more likely to have a single large

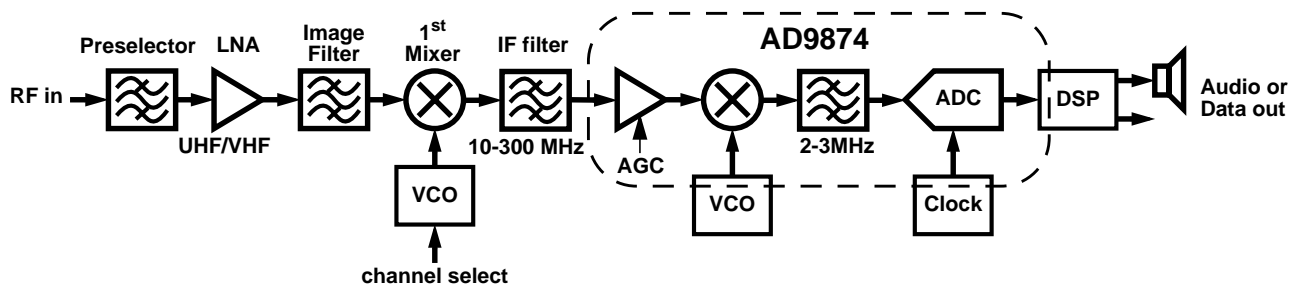
interferer than to have two interferers with large and comparable powers situated at frequencies that create an on-channel distortion product.

IC OVERVIEW

As shown in Figure 2, the AD9874 accepts an IF input up to 300 MHz and outputs complex baseband (I/Q) data. The data stream is serial, consisting of 16/24-b I and Q data followed by an optional 16-b AGC/status word. To facilitate a trade-off between pin usage and decode complexity, the AD9874 supports several 1-, 2- and 3-wire serial formats.

The primary blocks within the IC are an LNA, a mixer, an ADC and a digital filter. The LNA presents a 360Ω resistance to the IFIN pin and drives the doubly-balanced mixer with an amplified version of the IFIN input. The mixer downconverts this signal to a second IF which is then digitized by the bandpass ADC. A digital filter mixes the bandpass data down to baseband and also filters the output down to the desired bandwidth. Finally, the parallel-to-serial converter outputs the data in the desired serial format.

Secondary blocks within the IC include LO and clock synthesizers, a serial peripheral interface (SPI) block as well as automatic gain control (AGC) and bias circuitry. The LO and clock synthesizers lock the LO and clock signals produced by external LO and clock VCOs to the frequency reference applied to the FREF pin. Alternatively, either synthesizer can be placed in standby and LO/clock signals applied



1. Structure of a dual-conversion superheterodyne receiver employing the AD9874.

Parameter	AD9870	AD9874	Units
Noise Figure	12	10	dB
Third-Order Intercept Point	-1	-1	dBm
Instantaneous Dynamic Range	80	90	dB
Current Consumption	45	22	mA
Maximum Clock Frequency	18	26	MHz
Maximum Signal Bandwidth	150	270	kHz

3. Typical performance of the AD9874 vs. its predecessor, the AD9870, which employed a more conventional architecture.

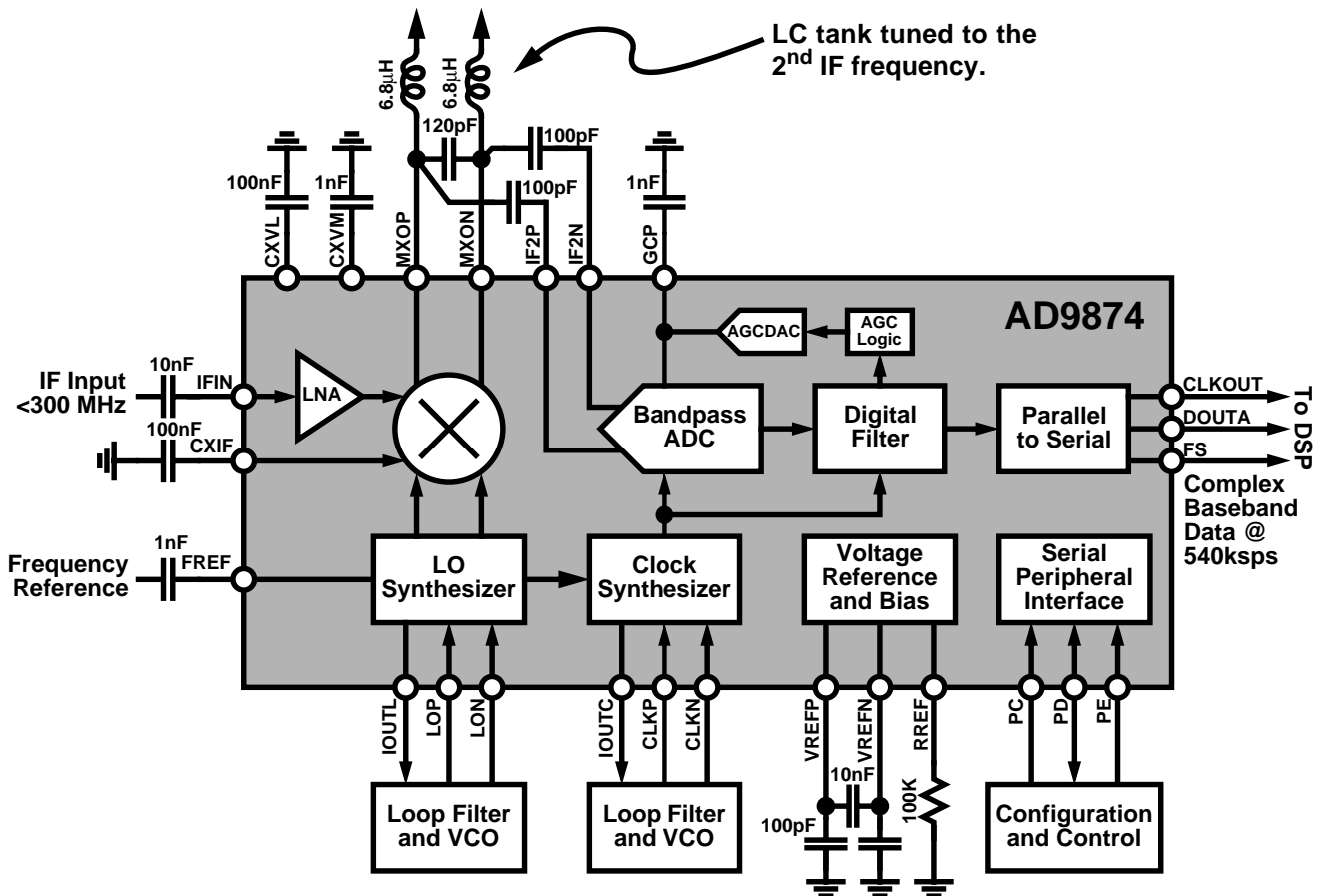
directly to the IC. The SPI port provides a 3-wire interface to the status and control registers within the IC. The AGC circuitry prevents clipping in the ADC when signals are large by reducing the gain in the signal path.

A unique aspect of the AD9874 is its use of inductors as signal-processing elements. Inductors are much-maligned components but are

the key to the AD9874's ability to accurately digitize a bandpass signal while consuming only a small amount of power. As evidence of this point, Figure 3 compares the AD9874 with the AD9870, a similar part released by Analog Devices earlier this year. The AD9870 uses switched-capacitor technology to realize a fully-integrated bandpass ADC whereas the AD9874 takes

advantage of external inductors in the construction of its ADC. As a result of this architectural difference, the AD9874 is able to achieve 10 dB more instantaneous dynamic range while simultaneously cutting the power consumption in *half*.

Modern inductors are small, rugged and inexpensive. Since tolerances of $\pm 10\%$ are easily accommodated by the on-chip tun-



2. AD9874 IF digitizing subsystem configured for 26 MHz clock frequency and set for maximum output signal bandwidth.

ing circuitry, precision components are not needed. Suitable surface-mount inductors measuring 2.5x2.0x1.6mm (1008 package) and weighing <100mg are available for \$0.08 in quantity. The fact that inductors yield significant power and performance advantages with low cost, weight and size, justifies their use in the AD9874.

IC DETAILS

To allow the AD9874 to serve a wide variety of applications, a broad frequency range is supported and many parameters of the IC are programmable via the SPI port.

A flexible frequency plan is afforded by the 10-300-MHz IF frequency range, the 0.1-50-MHz reference frequency range and the 13-26 MHz ADC clock frequency range. Good frequency planning involves choosing an IF frequency such that no spurs (such as harmonics of the clock) exist near either the IF or its image on the opposite side of the LO. Also, since the AD9874 uses integer- N synthesizers with programmable dividers on the reference frequency, the LO and clock frequencies must be rationally related to the reference frequency.

The clock frequency (f_{CLK}) is also integrally related to the center frequency (f_0) of the ADC as well as to

the output data rate. In the case of the center frequency this ratio is fixed at 1:8 (i.e. $f_0=f_{CLK}/8$) in order to be compatible with the first-generation AD9870. This integer relationship is used because it simplifies the internal hardware which performs quadrature digital down-conversion.

In a digital radio, the clock frequency is typically a multiple of the symbol rate. Since 13 MHz is a standard frequency within a GSM receiver (13 MHz is 48 times the 270.833-kHz baud rate), the AD9874 is designed to accept either a 13 MHz or a 26 MHz clock. For the sake of universality, any frequency between these limits is also allowed.

In the AD9874, the output signal bandwidth is equal to half of the output data rate, which is in turn equal to the clock frequency divided by the decimation factor (DF). DF can be one of $48n$ or $60n$, where n ranges from 1 to 16. For example, with a clock frequency of 24 MHz the signal bandwidth can be as low as 12.5 kHz or as high as 250 kHz. Figure 4a illustrates the filtering characteristics of the IC with DF=48 and DF=300, while Figure 4b shows an expanded view of the passband for DF=48. The steep cutoff and massive attenuation of signals folding into the ± 125 -kHz passband are

hallmarks of digital filtering. Since the AD9874 uses finite-impulse-response (FIR) filters, these desirable attenuation characteristics are provided by filters which have perfectly flat group delay. The 2x oversampled output data must undergo a final stage of channel filtering in the DSP before being demodulated since the transition band region may contain aliased signals, primarily from the adjacent channel.

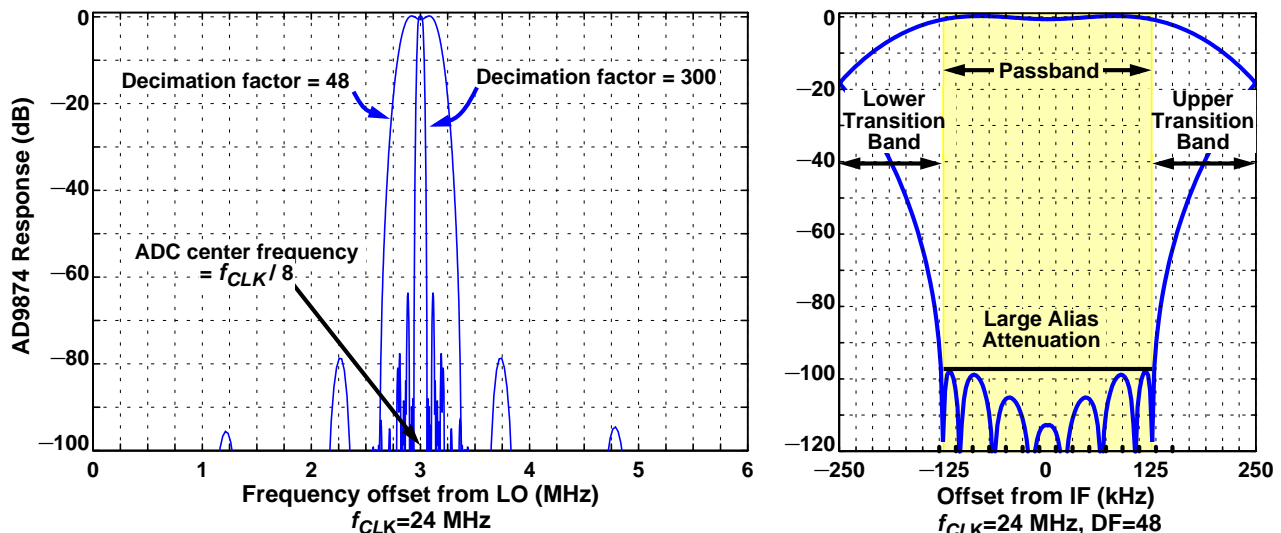
The AD9874 also includes automatic gain control (AGC) with programmable parameters. The AGC bandwidth spans 50Hz-9 kHz and includes adjustable fast attack/slow decay characteristics.

The AD9874 is designed to operate with supply voltages from 2.7 to 3.6V (up to 5.5V for the charge pumps within the synthesizers) over the extended industrial temperature range of -40 to +85°C. The AD9874 is housed in a space-saving 48LQFP (9x9x1.4mm) package.

IC PERFORMANCE

As described in the introduction, the dynamic range of a receiver is determined primarily by the noise figure (NF) and third-order intercept point (IIP3) specifications.

A receiver which uses a standard high-power ADC would have a NF



4. a) The filtering characteristics of the AD9874 are adjustable via the decimation factor setting.
b) The output data is 2x oversampled, so the signal bandwidth is half the output data rate.

which is independent of the signal bandwidth, but since the ADC of the AD9874 is optimized for narrow-band operation, its NF increases somewhat as the bandwidth increases. This property is illustrated in Figure 5, which shows that NF typically increases by about 2 dB as the signal bandwidth goes from 100 to 270 kHz. Below 100 kHz, NF is essentially constant at about 10 dB.

It is desirable for NF to increase only slowly as AGC attenuation increases since the receiver's ability to detect a weak signal will then degrade gracefully as interferers increase in strength. This desirable behavior is visible in Figure 6, which shows that as the signal han-

dling capability of the AD9874's ADC is increased by 12 dB, NF typically increases by only 2-3 dB.

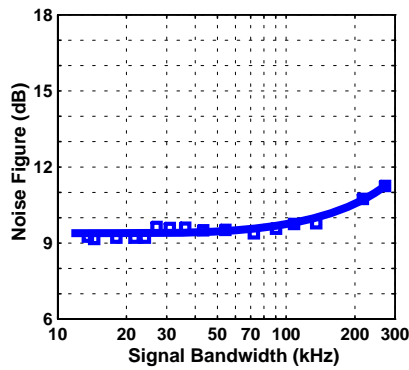
Figure 7 shows the in-band portion of the output spectrum when two relatively large (-37 dBm) tones are applied to the IC. Third-order nonlinearity results in -70 dBc intermodulation distortion (IMD), but all other distortion products and spurs are below -90 dBc.

To allow the user to trade system performance for reduced power consumption, the bias currents of the most power-hungry blocks, namely the LNA and the mixer, are digitally selectable. Figure 8 plots IMD3 as a function of the input power when the

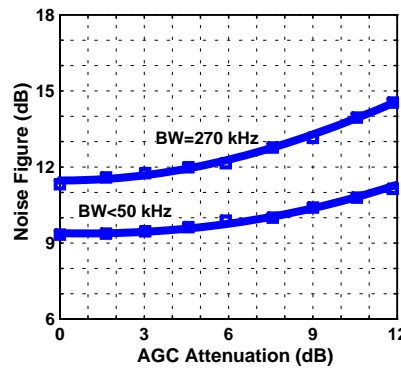
bias currents are maximum and when bias currents have been throttled back by 4mA. As this figure shows, scaling back on the bias currents reduces IIP3 from 0 dBm to -10 dBm. The impact of this bias change on NF is negligible. In all, four LNA and four mixer bias settings with different IIP3/NF trade-offs are available.

APPLICATION EXAMPLE

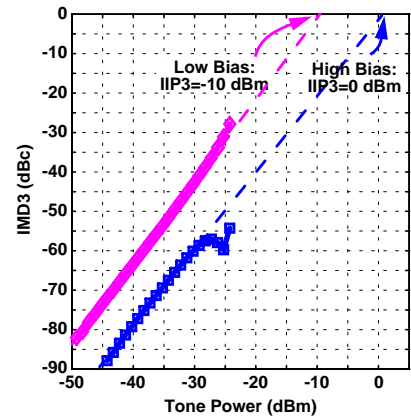
Digital receivers used in GSM cellular basestation (BTS) equipment must meet some of the most



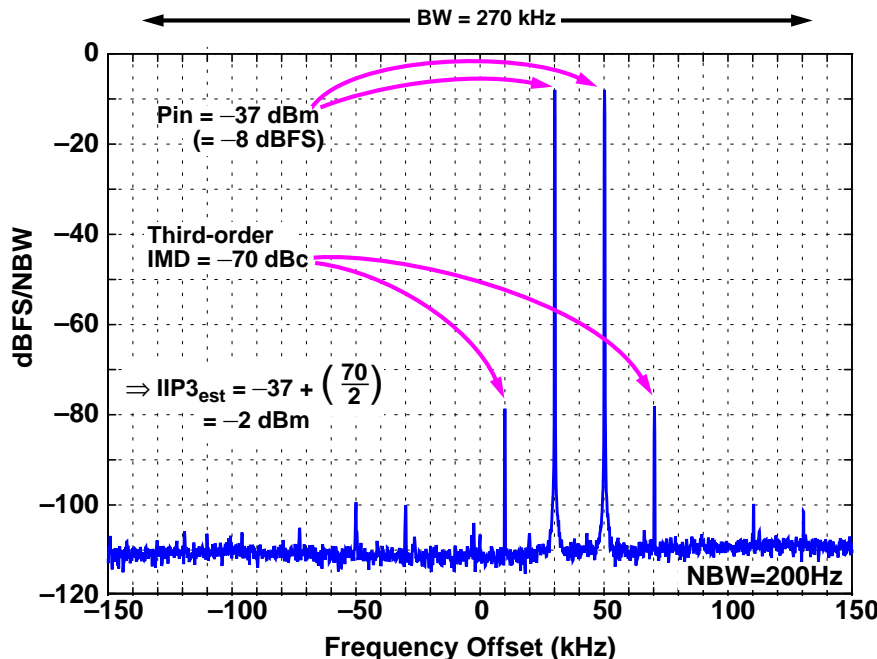
5. NF-bandwidth trade-off.
($f_{IF} = 109$ MHz, $f_{CLK} = 26$ MHz)



6. NF increases only gradually with AGC thanks to the high dynamic range ADC.
($f_{IF} = 109$ MHz, $f_{CLK} = 26$ MHz)



8. IMD3 vs. tone power for high and low bias settings.
($f_{IF} = 109$ MHz, $f_{CLK} = 26$ MHz)



7. In-band portion of the output spectrum for a two-tone input.
($f_{IF} = 104.25$ MHz, $f_{CLK} = 26$ MHz, $BW = 270$ kHz.) The two large tones produce -70 dBc intermodulation distortion products.

demanding performance requirements found in wireless mobile applications. These receivers are designed to operate in a hostile radio environment while providing high quality voice and data services to their mobile handsets. In order to provide a reliable link, these receivers require exceptional dynamic range and selectivity to recover target signals that can vary over a 89-dB range in the presence of strong adjacent interferers. Receivers supporting macro cells within the 900-MHz band (i.e. GSM900) represent the most challenging dynamic range requirements, while receivers supporting micro or pico cells and receivers operating in the 1900-MHz band have relaxed interferer and sensitivity specifications as detailed in the ETSI GSM 11.21 specification. In the GSM900 macro-BTS case, the digital receiver must recover target signals ranging from -15 dBm to -104 dBm while maintaining sufficiently low bit-error-rate. Since GSM achieves its high capacity by using a TDMA scheme whose time slots separated by only $28\mu\text{s}$, the instantaneous dynamic range of the receiver must be high in order to cope with large slot-to-slot variations in signal strength. Furthermore, the receiver must display a high degree of linearity and selectivity to deal with blocker(s) that may fall in adjacent channels with input levels up to -16 dBm at frequency offsets as small as 800 kHz from the target signal.

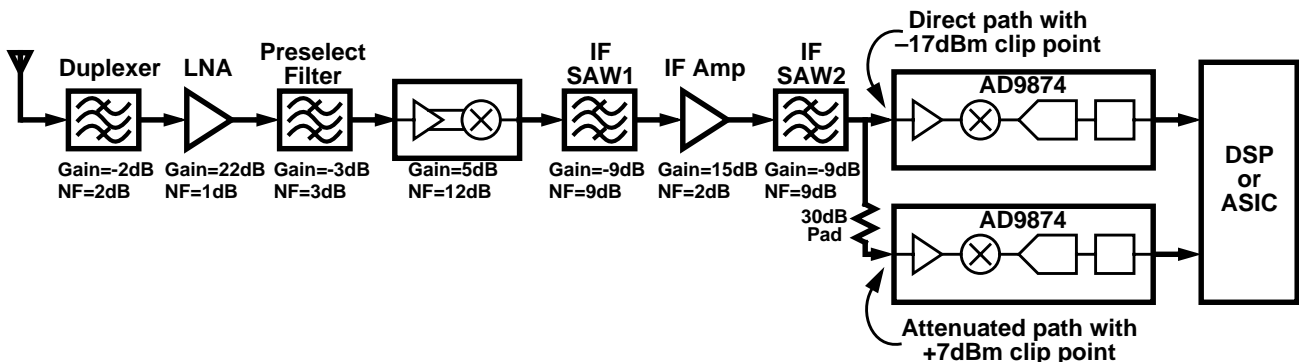
The AD9874's high level of inte-

gration and programmability makes it well suited for all GSM BTS classes. In particular, its low power dissipation makes it especially attractive for micro and pico BTSs. To cope with the high dynamic range requirements, two AD9874s can be operated in parallel with their respective *clip points* offset by a fixed amount. The clip point is the signal level which causes the AD9874's internal ADC to saturate. Adding a fixed amount of attenuation in front of the AD9874 and/or programming the attenuation setting of its internal VGA can be used to adjust the input-referred clip point. To save power and simplify hardware, the LO and CLK circuits of the device can be shared. Connecting the SYNCB pins of the two devices together and pulsing this line low synchronizes their digital filters and thus ensures precise time alignment of the two data streams.

An example of a possible GSM BTS receiver architecture based on this concept is shown in Figure 9. The signal chain consists of a high linearity RF front end and IF stage followed by two AD9874s operating in parallel. The RF front end consists of a duplexer and preselect filter to pass the GSM RF band of interest. A high performance LNA isolates the duplexer from the preselect filter while providing sufficient gain to minimize system NF. An RF mixer is used to downconvert the entire GSM band to a suitable IF where much of the channel selectivity is accomplished. The 170.6-MHz IF is

chosen to avoid any self-induced spurs from the AD9874. The IF stage consists of two SAW filters isolated by a 15-dB gain stage. The cascaded SAW filter response must provide sufficient blocker rejection in order for the receiver to meet its sensitivity requirements under worst-case blocker conditions. A composite response having 27, 60 and 100 dB rejection at frequency offsets of ± 0.8 , ± 1.6 , and ± 6.5 MHz respectively provides enough blocker suppression to ensure that the AD9874 with the lower clip point will not be overdriven by any blocker. This configuration results in the best possible receiver sensitivity under all blocking conditions.

The output of the last SAW filter drives the two AD9874s via a direct signal path and an attenuated signal path. The direct path corresponds to the AD9874 having the lowest clip point and provides the highest receiver sensitivity with a system noise figure of 4.7 dB. The VGA of this device is set for maximum attenuation, so its clip point is approximately -17 dBm. Since the conversion gain from the antenna to the AD9874 is 19 dB, the digital output of this path will nominally be selected unless the target signal's power exceeds -36 dBm at the antenna. The attenuated path corresponds to the AD9874 having the highest input-referred clip point and its digital output will be selected under high target signal conditions (i.e. > -36 dBm) when the direct path has been overdriven. The



9. A high-performance GSM receiver employing two AD9874s with clip points offset by 24 dB avoids the need for AGC action.

input-referred clip point of this path is set to +7 dBm by inserting a 30-dB attenuator and setting the AD9874's VGA to the middle of its 12-dB range. This setting gives a ± 6 -dB adjustment of the clip point, allowing the clip point difference to be calibrated to exactly 24 dB so that a simple 4-bit shift would compensate for the gain difference. The attenuated path can handle signal levels up to -12 dBm at the antenna before being overdriven. Since the SAW filters provide sufficient blocker suppression, the digital data from this path need only be selected when the target signal exceeds -36 dBm. Although the sensitivity of the receiver with the attenuated path is 20 dB lower than the direct path, the strong target signal ensures a sufficiently high carrier-to-noise ratio.

Since GSM is based on a TDMA scheme, digital data (or path) selection can occur on a slot-by-slot basis. The AD9874 would be configured to provide serial I and Q data at a frame rate of 541.67ksps as well as some additional information including a 2-bit reset field and a 6-bit RSSI field. These two fields contain the information needed to decide whether the direct or the attenuated path should be used for the current time slot.

The AD9874 provides a flexible implementation of the IF-to-bits portion of a superheterodyne receiver. Its high performance satisfies the demanding requirements of a base-station while its low power consumption and small size also make it an excellent choice for a handset. An evaluation board and evaluation software are available. P&A: Less than \$20 (1000 qty.); Jan. 2002. **Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; (800) 262-5643, (781) 329-4799, FAX: (781) 326-8703, Internet: <http://www.analog.com>.**