

RELIABILITY REPORT  
FOR  
MAX8805WEREEE+ /  
MAX8805WEWEEE+  
WAFER LEVEL PRODUCTS

November 2, 2009

**MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX8805WEREEE+ / MAX8805WEWEEE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	IV. ....Die Information
.....Attachments	

### I. Device Description

#### A. General

The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z high-frequency step-down converters are optimized for dynamically powering the power amplifier (PA) in WCDMA or NCDMA handsets. The devices integrate a high-efficiency PWM step-down converter for medium- and low-power transmission, and a 60m typical bypass FET to power the PA directly from the battery during high-power transmission. Dual 200mA low-noise, high-PSRR low-dropout regulators (LDOs) for PA biasing are also integrated. Two switching frequency options are available (2MHz for the MAX8805W/MAX8805Y and 4MHz for the MAX8805X/MAX8805Z), allowing optimization for smallest solution size or highest efficiency. Fast switching allows the use of small ceramic 2.2 $\mu$ F input and output capacitors while maintaining low ripple voltage. The feedback network is integrated, further reducing external component count and total solution size. The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z use an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. The REFIN to OUT gain is available in two options (2V/V for the MAX8805Y/MAX8805Z and 2.5V/V for the MAX8805W/MAX8805X). At high-duty cycle, the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z automatically switch to the bypass mode, connecting the input to the output through a low-impedance (60m typ) MOSFET. The user can also enable the bypass mode directly through a logic-control input. The LDOs in the MAX8805W/MAX8805X/MAX8805Y/MAX8805Z are designed for low-noise operation (35 $\mu$ VRMS typ). Each LDO is individually enabled through its own logic control interface. The MAX8805W/MAX8805X/MAX8805Y/MAX8805Z are available in a 16-bump, 2mm x 2mm WLP package (0.7mm max height).

**II. Manufacturing Information**

A. Description/Function:	600mA/650mA PWM Step-Down Converters in 2mm x 2mm WLP for WCDMA PA Power
B. Process:	S45
C. Number of Device Transistors:	6264
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Texas or Japan
F. Date of Initial Production:	2007

**III. Packaging Information**

A. Package Type:	16-bump WLP 4 x 4 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3422 or #05-9000-2787
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	°C/W
M. Multi Layer Theta Jc:	°C/W

**IV. Die Information**

A. Dimensions:	83 X 83 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)  
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$
$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

### C. E.S.D. and Latch-Up Testing

The PP31-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of 250 mA.

**Table 1**  
 Reliability Evaluation Test Results  
**MAX8805WEREEE+ / MAX8805WEWEEE+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
<b>Moisture Testing</b> (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data