RELIABILITY REPORT

FOR

MAX77812EWB+T

WAFER LEVEL DEVICES

February 24, 2018

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX77812EWB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX77812 is a quad-phase, high-current, buck regulator for multicore applications processors in the latest smart phones and tablets. The MAX77812 achieves world-class transient response with miniature PCB footprint through the use of small inductors and output capacitors. Differential remote sense feedback enables tight DC and AC accuracy at the point of load. The MAX77812"s flexible architecture allows user-selectable phase configurations such as 4, 3 + 1, 2 + 2, 2 + 1 + 1, and 1 + 1 + 1 + 1. Programmable current limit minimizes inductor size given the system’s actual requirements. Programmable soft-start ramp rate, rising and falling ramp rates, and startup operation provide control over inrush current as the regulator transitions between operating states. An output voltage range of 0.25V to 1.525V supports a wide range of application processors, down to the lowest power retention states. Multifunction general-purpose inputs and high-speed serial interface provide flexible enable control of each regulator, DVS operation, and output voltage ramp rate control that enables rapid output voltage adjustment to optimize performance in all system operating states. The MAX77812 features I^2C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77812 I2C supports SCL clock rates up to 3.4MHz. The MAX77812 I^2C can be configured as a 26MHz (typ) SPI interface by I^2C_SPI_SEL input pin. The MAX77812 is available in a 64-bump 0.4mm pitch WLP package with a maximum height of 0.8mm.

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II. Manufacturing Information

A. Description/Function:	Quad-Phase, 20A Max, Configurable Buck Regulator
B. Process:	S18
C. Number of Device Transistors:	296402
D. Fabrication Location:	Taiwan, USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	June 10, 2016

III. Packaging Information

A. Package Type:	64-bump WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Assembly Diagram:	#05-100270
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	N/A°C/W
J. Single Layer Theta Jc:	N/A°C/W
K. Multi Layer Theta Ja:	33.2°C/W
L. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	133.8582X135.433 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PB02 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX77812EWB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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