RELIABILITY REPORT

FOR MAX5971AETI+T

PLASTIC ENCAPSULATED DEVICES

July 14, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX5971AETI+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5971A is a single-port, power-sourcing equipment (PSE) power controller designed for use in IEEE® 802.3af/at-compliant PSE. This device provides powered device (PD) discovery, classification, current limit, DC and AC load-disconnect detections. The MAX5971A operates automatically without the need for any software programming and features an integrated power MOSFET and sense resistor. The device also supports new Class 5 and 2-event classification for detection and classification of high-power PDs. The MAX5971A provides up to 40W to a single port (Class 5 enabled) and still provides high-capacitance detection for legacy PDs. The MAX5971A provides input undervoltage lockout (UVLO), input overvoltage lockout, overtemperature detection, output voltage slew-rate limit during startup, and LED status indication. The MAX5971A is available in a space-saving, 28-pin TQFN (5mm x 5mm) power package, and is rated for the extended (-40°C to +85°C) temperature range.

II. Manufacturing Information

A. Description/Function:	Single-Port, 40W, IEEE 802.3af/at PSE Controller with Integrated MOSFET
B. Process:	S45
C. Number of Device Transistors:	59516
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Thailand
F. Date of Initial Production:	January 23, 2010

III. Packaging Information

A. Package Type:	28-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3824
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	2.1°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2.1°C/W

IV. Die Information

A. Dimensions:	105 X 101 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$

(Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.4 \times 10^{-9}$

λ = 23.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The NQ44 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage within AMR per JEDEC JESD78, except pin 5 (ILM2) which passes -85mA/+100mA.

Table 1

Reliability Evaluation Test Results

MAX5971AETI+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0

Note 1: Life Test Data may represent plastic DIP qualification lots.