RELIABILITY REPORT

FOR

MAX5969BETB+

PLASTIC ENCAPSULATED DEVICES

April 6, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX5969BETB+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5969A/MAX5969B provide a complete interface for a powered device (PD) to comply with the IEEE® 802.3af/at standard in a power-over-Ethernet (PoE) system. The MAX5969A/MAX5969B provide the PD with a detection signature, classification signature, and an integrated isolation power switch with inrush current control. During the inrush period, the MAX5969A/MAX5969B limit the current to less than 180mA before switching to the higher current limit (720mA to 880mA) when the isolation power MOSFET is fully enhanced. The devices feature an input UVLO with wide hysteresis and long deglitch time to compensate for twisted-pair cable resistive drop and to assure glitch-free transition during power-on/-off conditions. The MAX5969A/MAX5969B can withstand up to 100V at the input. The MAX5969A/MAX5969B support a 2-event classification method as specified in the IEEE 802.3at standard and provide a signal to indicate when probed by Type 2 power-sourcing equipment (PSE). The devices detect the presence of a wall adapter power-source connection and allow a smooth switchover from the PoE power source to the wall power adapter. The MAX5969A/MAX5969B also provide a power-good (PG) signal, two-step current limit and foldback, overtemperature protection, and di/dt limit. The MAX5969A/MAX5969B are available in a space-saving, 10-pin, 3mm × 3mm, TDFN power package. These devices are rated over the -40°C to +85°C extended temperature range.

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II. Manufacturing Information

A. Description/Function:	IEEE 802.3af/at-Compliant, Powered Device Interface Controllers with Integrated Power MOSFET
B. Process:	S45
C. Number of Device Transistors:	4476
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Thailand, China, Malaysia
F. Date of Initial Production:	October 23, 2009

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3863
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.5°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.5°C/W

IV. Die Information

A. Dimensions:	60 X 68 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot # SXEZBQ002D, D/C 1104)

The NQ39 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX5969BETB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SXEYAQ002A, D/C 1032

Note 1: Life Test Data may represent plastic DIP qualification lots.

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