

RELIABILITY REPORT FOR MAX44248AUA+ / MAX44248ASA+ PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

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Quality Assurance				
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Conclusion

The MAX44248AUA+ / MAX44248ASA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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- I. Device Description
 - A. General

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The MAX44248 is an ultra-precision, low-noise, zero-drift dual operational amplifier featuring very low-power operation with a wide supply range. The device incorporates a patented auto-zero circuit that constantly measures and compensates the input offset to eliminate drift over time and temperature as well as the effect of 1/f noise. The device also features integrated EMI filters to reduce high-frequency signal demodulation on the output. The op amp operates from either a single 2.7V to 36V supply or dual ±1.35V to ±18V supply. The device is unity-gain stable with a 1MHz gain-bandwidth product and a low 90µA supply current per amplifier. The low offset and noise specifications and high supply range make the device ideal for sensor interfaces and transmitters. The device is available in 8-pin µMAX® and SO packages and is specified over the -40°C to +125°C automotive operating temperature range.



II. Manufacturing Information

A. Description/Function: 36V, Precision, Low-Power, 90µA, Dual Op Amp
B. Process: S18
C. Number of Device Transistors: 3419
D. Fabrication Location: USA
E. Assembly Location: Philippines, Thailand Malay
F. Date of Initial Production: September 7, 2012

III. Packaging Information

A. Package Type:	8-pin uMAX	8-pin SOIC
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (0.8 mil dia.)	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4893	#05-9000-4892
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	221°C/W	170°C/W
K. Single Layer Theta Jc:	41.9°C/W	40°C/W
L. Multi Layer Theta Ja:	206.3°C/W	132°C/W
M. Multi Layer Theta Jc:	41.9°C/W	38°C/W

IV. Die Information

A. Dimensions:	42.5197X52.7559 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

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A. Accelerated Life Test
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The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{240 \text{ x } 4340 \text{ x } 80 \text{ x } 2}$ (Chi square value for MTTF upper limit) (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV) $\lambda = 10.9 \times 10^{-9}$

 λ = 10.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The OY78-0 die type has been found to have all pins able to withstand a transient pulse of: ESD-HBM: +/- 2000V per JEDEC JESD22-A114 ESD-MM: +/- 200 V per JEDEC JESD22-A115

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.



Table 1 Reliability Evaluation Test Results

MAX44248AUA+ / MAX44248ASA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note	e 1) Ta = 135°C Biased Time = 240 hrs.	DC Parameters & functionality	80	0	SAG05Q002C, D/C 1224

Note 1: Life Test Data may represent plastic DIP qualification lots.