RELIABILITY REPORT

FOR

MAX3378EEUD+T / MAX3378EETD+T

PLASTIC ENCAPSULATED DEVICES

January 15, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX3378EEUD+T / MAX3378EETD+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3372E-MAX3379E and MAX3390E-MAX3393E ±15kV ESD-protected level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. A low-voltage logic signal present on the V_L side of the device appears as a high-voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX3374E/MAX3375E/MAX3376E/MAX3379E and MAX3390E-MAX3393E unidirectional level translators level shift data in one direction (V_L -> V_{CC} or V_{CC} -> V_L) on any single data line. The MAX3372E/MAX3373E and MAX3377E/MAX3378E bidirectional level translators utilize a transmission-gate-based design (Figure 2 in the full data sheet) to allow data translation in either direction (VL <-> VCC) on any single data line. The MAX3372E-MAX3379E and MAX3390E-MAX3393E accept V_L from +1.2V to +5.5V and VCC from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. All devices in the MAX3372E-MAX3379E, MAX3390E-MAX3393E family feature a three-state output mode that reduces supply current to less than 1µA, thermal shortcircuit protection, and ±15kV ESD protection on the V_{CC} side for greater protection in applications that route signals externally. The MAX3372E/MAX3377E operate at a guaranteed data rate of 230kbps. Slew-rate limiting reduces EMI emissions in all 230kbps devices. The MAX3373E-MAX3376E/MAX3378E/MAX3379E and MAX3390E-MAX3393E operate at a guaranteed data rate of 8Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible. (See the *Timing Characteristics* table in the full data sheet.) The MAX3372E-MAX3376E are dual level shifters available in 3 x 3 UCSP™, 8-pin TDFN, and 8-pin SOT23 packages. The MAX3377E/MAX3378E/MAX3379E and MAX3390E-MAX3393E are quad level shifters available in 3 x 4 UCSP, 14-pin TDFN, and 14-pin TSSOP packages.

II. Manufacturing Information

A. Description/Function:	±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP	
B. Process:	B8	
C. Number of Device Transistors:	295	
D. Fabrication Location:	USA	
E. Assembly Location:	Malaysia, Philippines and Thailand	China, Taiwan and Thailand
F. Date of Initial Production:	April 27, 2002	

III. Packaging Information

A. Package Type:	14-pin TSSOP	14-pin TDFN
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-2601-0074	#05-9000-1642
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	110°C/W	54°C/W
K. Single Layer Theta Jc:	30°C/W	8°C/W
L. Multi Layer Theta Ja:	100.4°C/W	41°C/W
M. Multi Layer Theta Jc:	30°C/W	8°C/W

IV. Die Information

A. Dimensions:	80 X 61 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 89 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 12.4 \times 10^{-9}$

λ = 12.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.03 @ 25C and 0.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The RT40-4 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 1000V per JEDEC JESD22-A114 (lot S8N4CQ002H, D/C 0534)
ESD-CDM:	+/- 750V per JEDEC JESD-C101 (lot S8N4CQ002H, D/C 0534)

Latch-Up testing has shown that this device withstands a current of 250mA (lot S8N4CQ001A, D/C 0452).

Table 1

Reliability Evaluation Test Results

MAX3378EEUD+T/ MAX3378EETD+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	44 45	0 0	S8N4CQ002H, D/C 0534 I8N0BQ001A

Note 1: Life Test Data may represent plastic DIP qualification lots.