RELIABILITY REPORT

FOR

MAX17501xATB+T / MAX17501xAUD+T

PLASTIC ENCAPSULATED DEVICES

January 29, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX17501xATB+T / MAX17501xAUD+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17501 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input voltage range. It delivers output currents up to 500mA at output voltages of 0.9V to 92%VIN. The output voltage is accurate to within ±1.7% over -40°C to +125°C. The MAX17501 is available in a compact TDFN package. Simulation models are available. The device features peak-current-mode control with pulse-width modulation (PWM). Users can choose devices with either pulse frequency modulation (PFM) or forced PWM scheme. PFM devices skip pulses at light load for higher efficiency, while forced-PWM devices operate with fixed switching frequency at any load for noise sensitive-applications. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify the layout. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain active-low RESET pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage.

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II. Manufacturing Information

A. Description/Function:	60V, 500mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converter	
B. Process:	S18	
C. Number of Device Transistors:		
D. Fabrication Location:	USA	
E. Assembly Location:	Thailand	Thailand
F. Date of Initial Production:	March 22, 2012	

III. Packaging Information

A. Package Type:	10-pin TDFN 3x2	14-pin TSSOP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	NiPdAu	100% matte Tin
D. Die Attach:	Non-conductive	Conductive
E. Bondwire:	Au (1.3 mil dia.)	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4357	#05-9000-4358
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	87.5°C/W	48°C/W
K. Single Layer Theta Jc:	18.2°C/W	3°C/W
L. Multi Layer Theta Ja:	67.3°C/W	39°C/W
M. Multi Layer Theta Jc:	18.2°C/W	3°C/W

IV. Die Information

A. Dimensions:	
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 158 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.0 \times 10^{-9}$

$\lambda = 7.0$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25C and 1.05 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAKP5A004C, D/C 1250)

The PI01-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage to 85V per JEDEC JESD78, except pin 5 (FB) which passes +100mA/-90mA..

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Table 1

Reliability Evaluation Test Results

MAX17501xATB+T / MAX17501xAUD+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C	DC Parameters	79	0	SAIP0Q003D, D/C 1239
	Biased	& functionality	79	0	SAKP5A004C, D/C 1250
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.

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