

RELIABILITY REPORT
FOR
MAX15053EWL+TCN1
WAFER LEVEL DEVICES

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# **MAXIM INTEGRATED**

160 RIO ROBLES SAN JOSE, CA 95134

Eric Wright
Reliability Engineer

Brian Standley Manager, Reliability



#### Conclusion

The MAX15053EWL+TCN1 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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#### I. Device Description

#### A. General

The MAX15053 high-efficiency, current-mode, synchronous step-down switching regulator with integrated power switches delivers up to 2A of output current. The device operates from 2.7V to 5.5V and provides an output voltage from 0.6V up to 94% of the input voltage, making the device ideal for distributed power systems, portable devices, and preregulation applications. The MAX15053 utilizes a current-mode control architecture with a high gain transconductance error amplifier. The current-mode control architecture facilitates easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients. The MAX15053 offers selectable skip-mode functionality to reduce current consumption and achieve a higher efficiency at light output load. The low RDS(ON) integrated switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout design a much simpler task with respect to discrete solutions. Utilizing a simple layout and footprint assures first-pass success in new designs. The MAX15053 features a 1MHz, factory-trimmed, fixed-frequency PWM mode operation. The high switching frequency, along with the PWM current-mode architecture, allows for a compact, all-ceramic capacitor design. The MAX15053 offers a capacitor-programmable soft-start reducing inrush current, startup into PREBIAS operations, and a PGOOD open-drain output that can be used as an interrupt and for power sequencing. The MAX15053 is available in a 9-bump (3 x 3 array), 1.5mm x 1.5mm WLP package and is specified over the -40°C to +85°C temperature range.



## II. Manufacturing Information

A. Description/Function: High-Efficiency, 2A, Current-Mode Synchronous, Step-Down Switching

Regulator

Level 1

B. Process: S18 10543 C. Number of Device Transistors: USA D. Fabrication Location:

E. Assembly Location: Taiwan, USA F. Date of Initial Production: April 23, 2010

## III. Packaging Information

9-bump WLP A. Package Type:

B. Lead Frame: N/A C. Lead Finish: N/A D. Die Attach: None

E. Bondwire: N/A (N/A mil dia.)

F. Mold Material: None

G. Assembly Diagram: #05-100306 H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard J-STD-020-C

N/A°C/W J. Single Layer Theta Ja: N/A°C/W K. Single Layer Theta Jc: 71°C/W L. Multi Layer Theta Ja: N/A°C/W M. Multi Layer Theta Jc:

### IV. Die Information

A. Dimensions: 60.2362X60.2362 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)

AI/0.5%Cu with Ti/TiN Barrier C. Interconnect:

D. Backside Metallization: None

E. Minimum Metal Width: 0.23 microns (as drawn) F. Minimum Metal Spacing: 0.23 microns (as drawn)

G. Isolation Dielectric: SiO<sub>2</sub> H. Die Separation Method: Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)

Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm</li>D. Sampling Plan: Mil-Std-105D

#### VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 85C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (3) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{500 \times 4340 \times 159 \times 2}$$
 (Chi square value for MTTF upper limit)  $\frac{1}{500 \times 4340 \times 159 \times 2}$  (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)  $\frac{1}{1000 \times 1000} = \frac{1.83}{1000 \times 1000} = \frac{1.83}{10000} = \frac{1.83}{1000 \times 1000} = \frac{1.83}{1000 \times 1000} = \frac{1.83}{10000} = \frac{1.83$ 

 $\lambda = 63.2 \text{ F.I.T.}$  (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (Lot: TBNB0A017B D/C: 1647)

The NQ48 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.



# **Table 1**Reliability Evaluation Test Results

# MAX15053EWL+TCN1

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (	Note 1)				
	Ta = 85C	DC Parameters	159	0	TBUQ9Q001 D/C 1513
	Biased	& functionality			TBNB0A017B D/C 1647
	Time = $500 \text{ hrs.}$	•			

Note 1: Life Test Data may represent plastic DIP qualification lots.