

RELIABILITY REPORT FOR
MAX14821ETG+T / MAX14821EWA+T
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Quality Assurance
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Conclusion

The MAX14821ETG+T / MAX14821EWA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14821 transceiver is suitable for IO-Link® devices and 24V binary sensors/actuators. All specified IO-Link data rates are supported. In IO-Link applications, the transceiver acts as the physical layer interface to a microcontroller running the data-link layer protocol. Additional 24V digital inputs and outputs are provided. Two internal linear regulators generate common sensor and actuator power requirements: 5V and 3.3V. On-board C/Q and DO drivers are independently configurable for push-pull, high-side (PNP), or low-side (NPN) operation. The device detects the IO-Link C/Q wake-up condition and generates a wake-up signal on the active-low WU output. The C/Q and DI inputs have selectable current loads for use in actuators. An SPI(tm) interface allows configuration and monitoring of the device. Extensive alarm conditions are detected and communicated through the active-low IRQ output and the SPI interface. The device features reverse-polarity, short-circuit, and thermal protection. All power lines are monitored for undervoltage conditions. The C/Q and DO drivers are specified for sourcing/sinking up to 100mA. The device is available in a 2.5mm x 2.5mm, 25-pin WLP and a 4mm x 4mm, 24-pin TQFN package. Both are specified over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	IO-Link Device Transceiver
B. Process:	S45
C. Number of Device Transistors:	15024
D. Fabrication Location:	U.S.A.
E. Assembly Location:	Taiwan, China, Thailand, Malaysia Japan
F. Date of Initial Production:	June 24, 2011

III. Packaging Information

A. Package Type:	24-pin TQFN 4x4	25-bump WLP
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Die Attach:	Conductive	None
E. Bondwire:	Au (1 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	None
G. Assembly Diagram:	#05-9000-3925	#05-9000-3924
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	48°C/W	N/A°C/W
K. Single Layer Theta Jc:	3°C/W	N/A°C/W
L. Multi Layer Theta Ja:	36°C/W	44°C/W
M. Multi Layer Theta Jc:	3°C/W	N/A°C/W

IV. Die Information

A. Dimensions:	100 X 100 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.4 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- | | |
|-----------------------------------|---|
| A. Quality Assurance Contacts: | Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 96 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 11.5 \times 10^{-9}$$

$$\lambda = 11.5 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.04 @ 25°C and 0.69 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SC6VBQ003B, D/C 1118)

The RU45-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results
MAX14821ETG+T / MAX14821EWA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	48	0	SC6YDA004A, D/C 1048
	Biased	& functionality	48	0	SC6ZDA004A, D/C 1048
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.