RELIABILITY REPORT

FOR

MAX14661ETI+

PLASTIC ENCAPSULATED DEVICES

January 22, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX14661ETI+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14661 is a serially controlled, dual-channel analog multiplexer allowing any of the 16 pins to be connected to either common pin simultaneously in any combination. The device features Beyond-the-Rails(tm) capability so that Â±5.5V signals can be passed with any single supply between +1.6V and +5.5V. The serial control is selectable between I2C and SPI. Both modes provide individual control of each independent switch so that any combination of switches can be applied. I2C mode provides two address-select pins allowing for addressing up to four devices on a single bus. The SPI mode includes a DOUT pin that can be used to chain multiple devices together with a single select signal. The IC is available in a 28-pin (4mm x 4mm) TQFN package and is specified over the -40ÂºC to +85ÂºC extended temperature range. The AB_ and COM_ pins provide Â±10kV ESD protection (HBM).

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II. Manufacturing Information

A. Description/Function:	Beyond-the-Rails 16:2 Multiplexer
B. Process:	S18
C. Number of Device Transistors:	26162
D. Fabrication Location:	California
E. Assembly Location:	Taiwan
F. Date of Initial Production:	August 6, 2013

III. Packaging Information

A. Package Type:	28L TQFN-CU
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Cu (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5212
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	3°C/W
L. Multi Layer Theta Ja:	35°C/W
M. Multi Layer Theta Jc:	3°C/W

IV. Die Information

A. Dimensions:	54.3307X70.8661 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot EALN9Q002A, D/C 1310)

The AL61-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX14661ETI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	EALN9Q002A, D/C 1310

Note 1: Life Test Data may represent plastic DIP qualification lots.

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