RELIABILITY REPORT

FOR

MAX11270EUG+

PLASTIC ENCAPSULATED DEVICES

November 12, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX11270EUG+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. .....Device Description

II. .....Manufacturing Information

III. .....Packaging Information

.....Attachments

IV. .....Die Information

V. .....Quality Assurance Information

VI. .....Reliability Evaluation

I. Device Description

A. General

The MAX11270 is a 24-bit delta-sigma ADC that achieves excellent 130dB SNR while dissipating an ultra-low 10mW. Sample rates up to 64ksps allow both precision DC and AC measurements. Integral nonlinearity is guaranteed to 4ppm maximum. The THD is -122dB. The MAX11270 communicates via an SPI-compatible serial interface and is available in a small 24-pin TSSOP package. The MAX11270 offers a 6.5nV/ noise programmable gain amplifier with gain settings between 1x to 128x. Optional buffers are also included to provide isolation of the signal inputs from the switched capacitor sampling network. This allows the MAX11270 to be used with high-impedance sources without compromising available dynamic range. The MAX11270 operates from a single 2.7V to 3.6V analog supply, or split ±1.8V analog supplies, allowing the analog input to be sampled below ground. The digital supply range is 2.0V to 3.6V, allowing communication with 2.5V, 3V, or 3.3V logic.

II. Manufacturing Information

A. Description/Function:	24-Bit, 10mW, 130dB SNR, 64ksps Delta-Sigma ADC with Integrated PGA
B. Process:	TS18
C. Number of Device Transistors:	674577
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	September 10, 2014

III. Packaging Information

A. Package Type:	24-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5461
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	82°C/W
K. Single Layer Theta Jc:	15°C/W
L. Multi Layer Theta Ja:	72°C/W
M. Multi Layer Theta Jc:	13°C/W

IV. Die Information

A. Dimensions:	107.9645X139.6364 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QAQC8Q001B, D/C 1415)

The AC87-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX11270EUG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	QAQC8Q001B, D/C 1415

Note 1: Life Test Data may represent plastic DIP qualification lots.