RELIABILITY REPORT

FOR

DS28E38

PLASTIC ENCAPSULATED DEVICES

September 23, 2017

**MAXIM INTEGRATED**

160 RIO ROBLES

SAN JOSE, CA 95134

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|---|---|

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**Conclusion**

The DS28E38 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

**Table of Contents**


| | |
|---|---|
| **I. ........Device Description** | **IV........ Die Information** |
| **II. ........Manufacturing Information** | **V......... Quality Assurance Information** |
| **III. .......Packaging Information** | **VI........ Reliability Evaluation** |
| **.....Attachments** | |


**I. Device Description**

A. General

The DS28E38 is an ECDSA public key-based secure authenticator that incorporates Maxim's patented ChipDNA™ PUF technology. ChipDNA technology involves a physically unclonable function (PUF) that enables the DS28E38 to deliver cost-effective protection against invasive physical attacks. Using the random variation of semiconductor device characteristics that naturally occur during wafer fabrication, the ChipDNA circuit generates a unique output value that is repeatable over time, temperature, and operating voltage. Attempts to probe or observe ChipDNA operation modifies the underlying circuit characteristics, preventing discovery of the unique value used by the chip cryptographic functions. The DS28E38 utilizes the ChipDNA output as key content to cryptographically secure all device stored data and optionally, under user control, as the private key for the ECDSA signing operation. With ChipDNA capability, the device provides a core set of cryptographic tools derived from integrated blocks including an asymmetric (ECC-P256) hardware engine, a FIPS/NIST-compliant true random number generator (TRNG), 2Kb of secured EEPROM, a decrement-only counter and a unique 64-bit ROM identification number (ROM ID). The ECC public/ private key capabilities operate from the NIST-defined P-256 curve to provide a FIPS 186-compliant ECDSA signature generation function. The unique ROM ID is used as a fundamental input parameter for cryptographic operations and serves as an electronic serial number within the application. The DS28E38 communicates over the single-contact 1-Wire® bus at both standard and overdrive speeds. The communication follows the 1-Wire protocol with the ROM ID acting as node address in the case of a multidevice 1-Wire network.

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## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | DeepCover® Secure ECDSA Authenticator with ChipDNA PUF Protection |
| B. Process: | TS18 |
| C. Fabrication Location: | Taiwan |
| D. Assembly Location: | Thailand |
| E. Date of Initial Production: | June 29, 2017 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 6-pin TDFN |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Ab8200t |
| E. Bondwire: | Au (0.8 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-100751 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 55°C/W |
| K. Single Layer Theta Jc: | 9°C/W |
| L. Multi Layer Theta Ja: | 42°C/W |
| M. Multi Layer Theta Jc: | 9°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 70X94 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ |
| C. Interconnect: | Al/0.5%Cu |
| D. Minimum Metal Width: | 0.23 microns (as drawn) |
| E. Minimum Metal Spacing: | 0.23 microns (as drawn) |
| F. Isolation Dielectric: | $SiO_2$ |
| G. Die Separation Method: | Wafer Saw |

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**V. Quality Assurance Information**

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

**VI. Reliability Evaluation**

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda$ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.1@ 25C and 1.9@ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The ES13-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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**Table 1**

Reliability Evaluation Test Results

**DS28E38**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 80 | 0 | |

Note 1: Life Test Data may represent plastic DIP qualification lots.

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