RELIABILITY REPORT

FOR

DS28E36

PLASTIC ENCAPSULATED DEVICES

January 15, 2018

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The DS28E36 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The DS28E36 is a DeepCover® secure authenticator that provides a core set of cryptographic tools derived from integrated asymmetric (ECC-P256) and symmetric (SHA-256) security functions. In addition to the security services provided by the hardware implemented crypto engines, the device integrates a FIPS/NIST true random number generator (RNG), 8Kb of secured EEPROM, a decrement-only counter, two pins of configurable GPIO, and a unique 64-bit ROM identification number (ROM ID). This unique ROM ID is used as a fundamental input parameter for cryptographic operations and also serves as an electronic serial number within the application. The DS28E36 communicates over the single-contact 1-Wire® bus at overdrive speed. The communication follows the 1-Wire protocol with the ROM ID acting as node address in the case of a multi-device 1-Wire network. The ECC public/private key capabilities operate from the NIST defined P-256 curve and include FIPS 186 compliant ECDSA signature generation and verification to support a bidirectional asymmetric key authentication model. The SHA-256 secret-key capabilities are compliant with FIPS 180 and are flexibly used either in conjunction with ECDSA operations or independently for multiple HMAC functions. Two GPIO pins can be independently operated under command control and include configurability supporting authenticated and non-authenticated operation including an ECDSA-based crypto-robust mode to support secure-boot of a host processor. DeepCover embedded security solutions cloak sensitive data under multiple layers of advanced security to provide the most secure key storage possible. To protect against device-level security attacks, invasive and noninvasive countermeasures are implemented including active die shield, encrypted storage of keys, and algorithmic methods.

II. Manufacturing Information

A. Description/Function:	DeepCover Secure Authenticator
B. Process:	TS18
C. Fabrication Location:	Taiwan
D. Assembly Location:	China, Thailand
E. Date of Initial Production:	November 3, 2017

III. Packaging Information

A. Package Type:	6-pin TDFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Ab8200t
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-100787
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	55°C/W
K. Single Layer Theta Jc:	9°C/W
L. Multi Layer Theta Ja:	42°C/W
M. Multi Layer Theta Jc:	9°C/W

IV. Die Information

A. Dimensions:	65.2756X89.2756 mils
B. Passivation:	Si_3N_4/SiO_2
C. Interconnect:	Al/0.5%Cu
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.1@ 25C and 1.9@ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The ES10-1 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V with the following exception:

IO pin: +/-8000V per JEDEC JESD22-A114

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

DS28E36

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.