LTM4676 to LTM4676A

INTRODUCTION

The LTM®4676A is a pin-compatible upgrade to the LTM4676. Key benefits of the LTM4676A over the LTM4676 include:

- Faster Power-Up
- Reduced PWM Minimum On-Time
- Faster ADC Telemetry Update
- Support of I^2C PMBus Thresholds Compatible with Bus Power Supplies as low as 1.8V
- Improved Internal EEPROM Robustness
- Wider Output Voltage Range
- More Accurate Output Setpoint Voltage
- PolyPhase® applications can use the differential sense amplifier of channel 0 for improved current sharing
- PolyPhase applications can clock at the desired frequency even if the SYNC pin is not clocking.

This guide describes the differences and explains the configuration file changes needed when migrating a design from the LTM4676 to the LTM4676A.

FEATURE COMPARISON

	LTM4676	LTM4676A
MFR_ADC_CONTROL for Fast ADC Sampling of a Parameter		✓
PMBus Version	1.1	1.2
Alert Masking (a Part of 1.2 PMBus Compliant)		✓
Shared Differential Sense Amp		✓
Improved SYNC Circuit if Input Clock is Lost		✓
Improved Fault Log Recording, EEPROM Robustness		✓
Uppermost Three Bits of the Module's PMBus Address are User-Configurable		✓
Supports PWM Burst Mode® Operation	✓	

PIN CONFIGURATION

All pins of the LTM4676A are fully compatible with the LTM4676. In most cases, the LTM4676A will work as a drop in replacement for the LTM4676.

ELECTRICAL CHARACTERISTICS

The electrical characteristics of the LTM4676A are the same as the LTM4676 with the following exceptions:

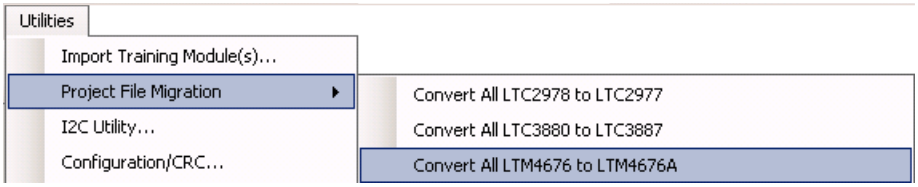
	LTM4676 (Obsolete)	LTM4676A
Turn-On Start-Up Time (t_{START}) TYP	153ms	**35ms**
Minimum On-Time ($t_{ON(MIN)}$) TYP	90ns	**45ns**
NVM Enhanced by ECC	No	**Yes**
ADC Update Period ($t_{CONVERT-*}$) TYP where * = various telemetry parameters	100ms	**90ms**
V_{IL} Logic Thresholds of the following TYP Pins: SCL, SDA, RUN0, RUN1, $\overline{GPIO_0}$, $\overline{GPIO_1}$	1.4V	**0.8V**
V_{IH} Logic Thresholds of the following TYP Pins: SCL, SDA, RUN0, RUN1, $\overline{GPIO_0}$, $\overline{GPIO_1}$	2.0V	**1.35V**
Output Voltage Range	Ch0: 0.5V to 4.0V Ch1: 0.5V to 5.4V	Ch0: 0.5V to **5.5V** Ch1: 0.5V to **5.5V**
Output Voltage Setpoint Accuracy	±1%, for all $V_{OUT} \geq 0.6V$	**±0.5%**, for all $V_{OUT} \geq 1V$ **±5mV**, for $0.6V \leq V_{OUT} < 1V$

CONFIGURATION FILE

Table 1 of the LTM4676A data sheet identifies PMBus commands of the LTM4676A that are new or have changed from the LTM4676. An automatic conversion utility is provided in LTpowerPlay™ to simplify the transition from an LTM4676 configuration file to a functionally equivalent LTM4676A configuration file.

If you have an existing LTM4676 project file (.proj file), the simplest way to convert a LTM4676 configuration into a LTM4676A configuration is to use the built-in project file migration tool in LTpowerPlay. Follow this simple procedure to convert your project file:

- Launch LTpowerPlay
- Select “File > Open…” on the menu and browse to the project file containing one or more LTM4676 devices
- Select “Utilities > Project File Migration > Convert All LTM4676 to LTM4676A” on the menu



After running the migration tool, all LTM4676 devices in your project file will be replaced with LTM4676A devices with equivalent configurations. For complete detail on how LTpowerPlay performs the migration at the register level, consult the “Writable Commands” section.

Read-Only Commands

The following read-only commands return different values on the LTM4676 and LTM4676A. No configuration file changes are required, but if your software or firmware reads these registers and expects certain values, note that they have changed.

CONFIGURATION FILE

	LTM4676	LTM4676A
MFR_SPECIAL_ID (0xE7)	0x440X or 0x448X	0x47EX
PMBUS_REVISION (0x98)	0x11	0x22
MFR_MODEL (0x9A)	LTM4676	LTM4676A

Writable Commands

A simple procedure exists to migrate an existing LTM4676 configuration for use in a LTM4676A device. The LTpowerPlay project file migration tool uses this procedure to automatically migrate your project file. The conversion details are provided below for those writing software/firmware and those wanting complete details on the migration process. Functions that require attention are listed in the table below, with the LTM4676 register and bit-field location shown in the second column, and the corresponding LTM4676A register and bit-field locations in the third column with the recommended action in the fourth column:

	LTM4676	LTM4676A	PROCEDURE
Mask PLL_UNLOCK	MFR_CONFIG_ALL Bit 3	MASK_STATUS_MFR_SPECIFIC Bit 4	Move to new location.
Mask Pull GPIO Low (Paged)	MFR_CHAN_CONFIG Bit 1	MASK_STATUS_MFR_SPECIFIC Bit 0	Move to new location and disable in old location.
Set Channel 0 VRANGE LO/HI	MFR_PWM_CONFIG Bit 6	MFR_PWM_MODE Bit 1 (Page 0)	Move to new location.
Set Channel 1 VRANGE LO/HI	MFR_PWM_CONFIG Bit 5	MFR_PWM_MODE Bit 1 (Page 1)	Move to new location.
Set PWM to CCM (Paged)	MFR_PWM_MODE Bit 1 and 0 = 10	MFR_PWM_MODE Bit 0 = 1	Move to new location.
Set PWM to DCM (Paged)	MFR_PWM_MODE Bit 1 and 0 = 00 or 01	MFR_PWM_MODE Bit 0 = 0	Move to new location and Burst Mode operation set to CCM.*
Set SYNC Out to Off (for PolyPhase Sync Slaves)	FREQUENCY_SWITCH = 00 (External Clock)	MFR_CONFIG_ALL Bit 3 = 0	Change as specified.**
Set Frequency (for PolyPhase Sync Slaves)	FREQUENCY_SWITCH = 00 (External Clock)	FREQUENCY_SWITCH = Frequency of Rail Master	Change as specified.**
Disable CML Quick Read	Quick Read Always Disabled	MFR_CONFIG_ALL Bit 5 = 1	Set to 1/disabled for backward compatibility.
Enable 32ms Timeout	32ms Timeout Always Enabled	MFR_CONFIG_ALL Bit 3 = 0	Set to 0/enabled for backward compatibility.
Enable Channel 0 EA for Channel 1 PWM Control	Not Available	MFR_PWM_CONFG Bit 7 = 1	Set to 0/disabled. User must change manually if desired.***
PGOOD Thresholds	Used for ADC PGOOD	Uses OV/UV Thresholds.	PGOOD thresholds not used in LTM4676A.
MFR_CHANNEL ADDRESS	Used to Communicate Directly with a Paged Command	Not Available, Use PAGE_PLUS if Atomic Commands Required	MFR_CHANNEL_ADDRESS is not used in the LTM4676A.

* The LTM4676 in burst mode, MFR_PWM_MODE bits 1 and 0 set to 01, cannot be supported in the LTM4676A. The closest option is DCM or MFR_PWM_MODE bit 0 set to 0.

** If and only if the project file has PolyPhase rails, LTpowerPlay infers frequency master of each rail as the module whose FREQUENCY_SWITCH is programmed as non-zero. During migration, LTpowerPlay will set all slave module FREQUENCY_SWITCH registers to match the master module. In addition, the SYNC output will only be enabled on the master channel. For all non-PolyPhase rails or systems where LTpowerPlay cannot determine which module is the frequency master (for instance, all FREQUENCY_SWITCH registers programmed to zero), the frequency commands will remain unchanged after the migration process.

*** This bit allows the differential sense amplifier from channel 0 to be the input to the channel 1 error amplifier. This bit may only be set if both channel 0 and channel 1 are part of the same PolyPhase rail and $COMP_{0a}$ and $COMP_{1a}$ are electrically connected together. Because this bit may cause application problems if incorrectly set, it will be set to zero when projects are migrated. The LTM4676 does not support this command so no change in operation will occur.

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