

## 5.0 kV RMS, 6-Channel Digital Isolators

## FEATURES

- ▶ High common-mode transient immunity: 100 kV/μs
- ▶ High robustness to radiated and conducted noise
- ▶ Low propagation delay
  - ▶ 13 ns maximum for 5 V operation
  - ▶ 15 ns maximum for 1.8 V operation
- ▶ 150 Mbps maximum guaranteed data rate
- ▶ Safety and regulatory approvals
  - ▶ UL 1577
    - ▶  $V_{ISO} = 5000 V_{RMS}$  for 1 minute
  - ▶ IEC/CSA 62368-1
  - ▶ IEC/CSA 60601-1
  - ▶ IEC/CSA 61010-1
  - ▶ CQC GB 4943.1
  - ▶ DIN EN IEC 60747-17 (VDE 0884-17)
    - ▶  $V_{IORM} = 849 V_{PEAK}$
- ▶ Low dynamic power consumption
- ▶ 1.8 V to 5 V level translation
- ▶ High temperature operation: 125°C
- ▶ Fail-safe high or low options
- ▶ 16-lead, RoHS-compliant, wide body SOIC\_IC package
- ▶ AEC-Q100 qualified for automotive applications

## APPLICATIONS

- ▶ General-purpose multichannel isolation
- ▶ Serial peripheral interface (SPI)/data converter isolation
- ▶ Industrial field bus isolation

## GENERAL DESCRIPTION

The ADuM260N/ADuM261N/ADuM262N/ADuM263N<sup>1</sup> are 6-channel digital isolators based on Analog Devices, Inc., iCoupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated couplers. The maximum propagation delay is 13 ns with a pulse width distortion of less than 4.5 ns at 5 V operation. Channel to channel matching of propagation delay is tight at 4.0 ns maximum.

The ADuM260N/ADuM261N/ADuM262N/ADuM263N data channels are independent and are available in a variety of configurations with a withstand voltage rating of 5.0 kV<sub>RMS</sub> (see the [Ordering Guide](#)). The devices operate with the supply voltage on either side ranging from 1.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Unlike other optocoupler alternatives, dc correctness is ensured in the absence of input logic transitions. Two different fail-safe options are available by which the outputs transition to a predetermined state when the input power supply is not applied.

<sup>1</sup> Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

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**REVISION HISTORY****2/2025—Rev. B to Rev. C**

Changes to Features Section.....	1
Moved Figure 1 to Figure 4.....	3
Changes to Table 9.....	12
Changes to Regulatory Information Section and Table 11.....	13
Changed DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section.....	14
Changes to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section, Table 12, and Figure 5 Caption.....	14
Added No. of Inputs, Withstand Voltage Rating, and Fail-Safe Output State Options.....	26

FUNCTIONAL BLOCK DIAGRAMS

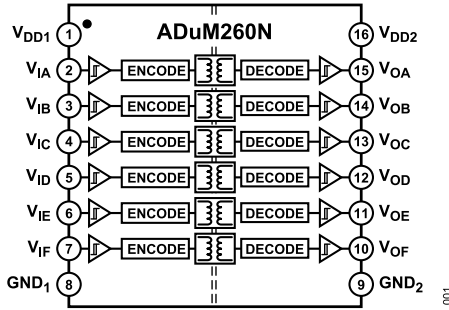


Figure 1. ADuM260N Functional Block Diagram

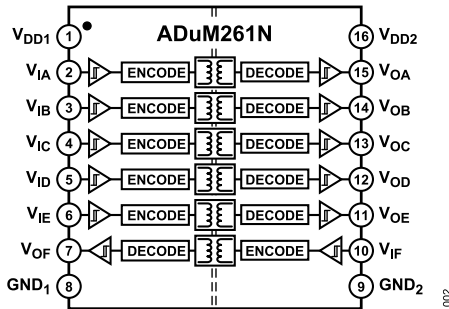


Figure 2. ADuM261N Functional Block Diagram

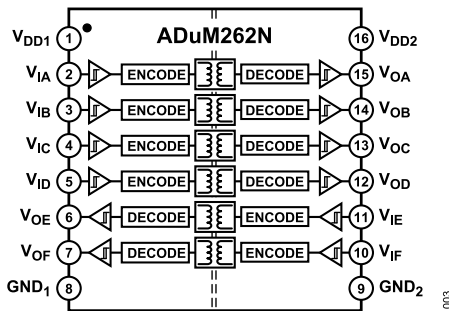


Figure 3. ADuM262N Functional Block Diagram

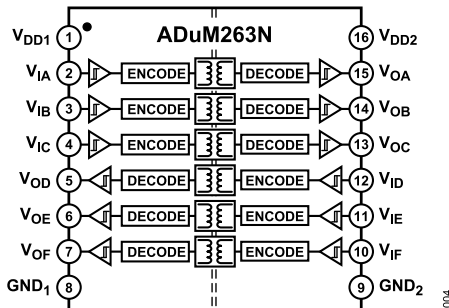


Figure 4. ADuM263N Functional Block Diagram

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range of  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>SWITCHING SPECIFICATIONS</b>						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate <sup>1</sup>		150			Mbps	Within PWD limit
Propagation Delay	$t_{PHL}$ , $t_{PLH}$	4.8	7.2	13	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	4.5	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/ $^\circ\text{C}$	
Propagation Delay Skew	$t_{PSK}$			6.1	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	$t_{PSKCD}$		0.5	4.0	ns	
Opposing Direction	$t_{PSKOD}$		0.5	4.5	ns	
Jitter			490		ps p-p	See the <a href="#">Jitter Measurement</a> section
			70		ps rms	See the <a href="#">Jitter Measurement</a> section
<b>DC SPECIFICATIONS</b>						
Input Threshold Voltage						
Logic High	$V_{IH}$	$0.7 \times V_{DDx}$			V	
Logic Low	$V_{IL}$			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{OX}^2 = -20\ \mu\text{A}$ , $V_{IX} = V_{IXH}^3$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{OX}^2 = -4\ \text{mA}$ , $V_{IX} = V_{IXH}^3$
Logic Low	$V_{OL}$		0.0	0.1	V	$I_{OX}^2 = 20\ \mu\text{A}$ , $V_{IX} = V_{IXL}^4$
			0.2	0.4	V	$I_{OX}^2 = 4\ \text{mA}$ , $V_{IX} = V_{IXL}^4$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{IX} \leq V_{DDx}$
Quiescent Supply Current						
ADuM260N						
	$I_{DD1(Q)}$		2.3	3.5	mA	$V_I^5 = 0\ (N0), 1\ (N1)^6$
	$I_{DD2(Q)}$		3.3	4.52	mA	$V_I^5 = 0\ (N0), 1\ (N1)^6$
	$I_{DD1(Q)}$		19.3	30	mA	$V_I^5 = 1\ (N0), 0\ (N1)^6$
	$I_{DD2(Q)}$		3.5	4.82	mA	$V_I^5 = 1\ (N0), 0\ (N1)^6$
ADuM261N						
	$I_{DD1(Q)}$		2.5	3.8	mA	$V_I^5 = 0\ (N0), 1\ (N1)^6$
	$I_{DD2(Q)}$		3.2	4.22	mA	$V_I^5 = 0\ (N0), 1\ (N1)^6$
	$I_{DD1(Q)}$		16.0	24.8	mA	$V_I^5 = 1\ (N0), 0\ (N1)^6$
	$I_{DD2(Q)}$		7.2	11.2	mA	$V_I^5 = 1\ (N0), 0\ (N1)^6$
ADuM262N						
	$I_{DD1(Q)}$		2.8	4.0	mA	$V_I^5 = 0\ (N0), 1\ (N1)^6$
	$I_{DD2(Q)}$		3.0	4.2	mA	$V_I^5 = 0\ (N0), 1\ (N1)^6$
	$I_{DD1(Q)}$		14.1	22.5	mA	$V_I^5 = 1\ (N0), 0\ (N1)^6$
	$I_{DD2(Q)}$		10.5	16.7	mA	$V_I^5 = 1\ (N0), 0\ (N1)^6$
ADuM263N						
	$I_{DD1(Q)}$		3.0	4.26	mA	$V_I^5 = 0\ (N0), 1\ (N1)^6$
	$I_{DD2(Q)}$		2.8	3.92	mA	$V_I^5 = 0\ (N0), 1\ (N1)^6$
	$I_{DD1(Q)}$		11.8	18.9	mA	$V_I^5 = 1\ (N0), 0\ (N1)^6$

## SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current	$I_{DD2(Q)}$		14.6	23	mA	$V_I^5 = 1$ (N0), 0 (N1) <sup>6</sup>
Dynamic Input	$I_{DDI(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO(D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive $V_{DDx}$ Threshold	$V_{DDxUV+}$		1.6		V	
Negative $V_{DDx}$ Threshold	$V_{DDxUV-}$		1.5		V	
$V_{DDx}$ Hysteresis	$V_{DDxUVH}$		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	$t_R/t_F$		2.5		ns	10% to 90%
Common-Mode Transient Immunity <sup>7</sup>	$ CM_H $	75	100		kV/ $\mu$ s	$V_{Ix} = V_{DDx}$ , $V_{CM} = 1000$ V, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ $\mu$ s	$V_{Ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

<sup>1</sup> 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

<sup>2</sup>  $I_{Ox}$  is the Channel x output current, where x = A, B, C, D, E, or F.

<sup>3</sup>  $V_{IxH}$  is the input side logic high.

<sup>4</sup>  $V_{IxL}$  is the input side logic low.

<sup>5</sup>  $V_I$  is the voltage input.

<sup>6</sup> N0 refers to the ADuM260N0/ADuM261N0/ADuM262N0/ADuM263N0 models. N1 refers to the ADuM260N1/ADuM261N1/ADuM262N1/ADuM263N1 models. See the [Ordering Guide](#) section.

<sup>7</sup>  $|CM_H|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output ( $V_O$ ) > 0.8  $V_{DDx}$ .  $|CM_L|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8$  V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM260N											
Supply Current Side 1	$I_{DD1}$		10.8	15.8		12.3	19.2		18.3	26	mA
Supply Current Side 2	$I_{DD2}$		3.6	5.5		5.63	9.0		12.8	20.9	mA
ADuM261N											
Supply Current Side 1	$I_{DD1}$		9.27	14.5		10.9	17.2		17.3	25.6	mA
Supply Current Side 2	$I_{DD2}$		5.33	9.0		7.39	12		14.5	22.2	mA
ADuM262N											
Supply Current Side 1	$I_{DD1}$		8.53	13.0		10.2	15.6		16.4	25.5	mA
Supply Current Side 2	$I_{DD2}$		6.83	10.5		8.64	13.1		14.6	22.3	mA
ADuM263N											
Supply Current Side 1	$I_{DD1}$		7.47	12.3		9.35	14.5		15.9	23	mA
Supply Current Side 2	$I_{DD2}$		8.75	14.0		10.5	16.0		17.0	23.3	mA

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.3\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>SWITCHING SPECIFICATIONS</b>						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate <sup>1</sup>		150			Mbps	Within PWD limit
Propagation Delay	$t_{PHL}$ , $t_{PLH}$	4.8	6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	4.5	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/ $^\circ\text{C}$	
Propagation Delay Skew	$t_{PSK}$			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	$t_{PSKCD}$		0.7	4.0	ns	
Opposing Direction	$t_{PSKOD}$		0.7	4.5	ns	
Jitter			580		ps p-p	See the <a href="#">Jitter Measurement</a> section
			120		ps rms	See the <a href="#">Jitter Measurement</a> section
<b>DC SPECIFICATIONS</b>						
Input Threshold Voltage						
Logic High	$V_{IH}$	$0.7 \times V_{DDx}$			V	
Logic Low	$V_{IL}$			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{Ox}^2 = -20\ \mu\text{A}$ , $V_{Ix} = V_{IxH}^3$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox}^2 = -2\ \text{mA}$ , $V_{Ix} = V_{IxH}^3$
Logic Low	$V_{OL}$		0.0	0.1	V	$I_{Ox}^2 = 20\ \mu\text{A}$ , $V_{Ix} = V_{IxL}^4$
			0.2	0.4	V	$I_{Ox}^2 = 2\ \text{mA}$ , $V_{Ix} = V_{IxL}^4$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Quiescent Supply Current						
ADuM260N						
	$I_{DD1(Q)}$		2.2	3.4	mA	$V_I^5 = 0\text{ (N0)}, 1\text{ (N1)}^6$
	$I_{DD2(Q)}$		3.1	4.1	mA	$V_I^2 = 0\text{ (N0)}, 1\text{ (N1)}^6$
	$I_{DD1(Q)}$		19	27.7	mA	$V_I^2 = 1\text{ (N0)}, 0\text{ (N1)}^6$
	$I_{DD2(Q)}$		3.4	4.7	mA	$V_I^2 = 1\text{ (N0)}, 0\text{ (N1)}^6$
ADuM261N						
	$I_{DD1(Q)}$		2.3	3.6	mA	$V_I^2 = 0\text{ (N0)}, 1\text{ (N1)}^6$
	$I_{DD2(Q)}$		3.0	4.0	mA	$V_I^2 = 0\text{ (N0)}, 1\text{ (N1)}^6$
	$I_{DD1(Q)}$		15.8	24.6	mA	$V_I^2 = 1\text{ (N0)}, 0\text{ (N1)}^6$
	$I_{DD2(Q)}$		7.0	11	mA	$V_I^2 = 1\text{ (N0)}, 0\text{ (N1)}^6$
ADuM262N						
	$I_{DD1(Q)}$		2.6	3.8	mA	$V_I^2 = 0\text{ (N0)}, 1\text{ (N1)}^6$
	$I_{DD2(Q)}$		2.8	4.0	mA	$V_I^2 = 0\text{ (N0)}, 1\text{ (N1)}^6$
	$I_{DD1(Q)}$		13.9	22.2	mA	$V_I^2 = 1\text{ (N0)}, 0\text{ (N1)}^6$
	$I_{DD2(Q)}$		10.3	16.5	mA	$V_I^2 = 1\text{ (N0)}, 0\text{ (N1)}^6$
ADuM263N						
	$I_{DD1(Q)}$		2.8	4.16	mA	$V_I^2 = 0\text{ (N0)}, 1\text{ (N1)}^6$
	$I_{DD2(Q)}$		2.6	3.82	mA	$V_I^2 = 0\text{ (N0)}, 1\text{ (N1)}^6$
	$I_{DD1(Q)}$		11.5	18.5	mA	$V_I^2 = 1\text{ (N0)}, 0\text{ (N1)}^6$

## SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current	$I_{DD2(Q)}$		14.3	22.5	mA	$V_I^2 = 1 (N0), 0 (N1)^6$
Dynamic Input	$I_{DD1(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive $V_{DDx}$ Threshold	$V_{DDxUV+}$		1.6		V	
Negative $V_{DDx}$ Threshold	$V_{DDxUV-}$		1.5		V	
$V_{DDx}$ Hysteresis	$V_{DDxUVH}$		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	$t_R/t_F$		2.5		ns	10% to 90%
Common-Mode Transient Immunity <sup>7</sup>	$ CM_H $	75	100		kV/ $\mu$ s	$V_{ix} = V_{DDx}, V_{CM} = 1000$ V, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ $\mu$ s	$V_{ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

<sup>1</sup> 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

<sup>2</sup>  $I_{Ox}$  is the Channel x output current, where x = A, B, C, D, E, or F.

<sup>3</sup>  $V_{ixH}$  is the input side logic high.

<sup>4</sup>  $V_{ixL}$  is the input side logic low.

<sup>5</sup>  $V_I$  is the voltage input.

<sup>6</sup> N0 refers to the ADuM260N0/ADuM261N0/ADuM262N0/ADuM263N0 models. N1 refers to the ADuM260N1/ADuM261N1/ADuM262N1/ADuM263N1 models. See the Ordering Guide section.

<sup>7</sup>  $|CM_H|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output ( $V_O$ ) > 0.8  $V_{DDx}$ .  $|CM_L|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O$  > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput

Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM260N											
Supply Current Side 1	$I_{DD1}$		10.5	15.5		11.7	18.6		16.6	24.6	mA
Supply Current Side 2	$I_{DD2}$		3.4	5.4		5.4	7.8		11.8	19.9	mA
ADuM261N											
Supply Current Side 1	$I_{DD1}$		9.0	14.2		10.4	16.6		15.7	24.1	mA
Supply Current Side 2	$I_{DD2}$		5.1	8.8		7.0	11.6		13.1	20.8	mA
ADuM262N											
Supply Current Side 1	$I_{DD1}$		8.3	12.8		9.8	14.8		15.2	24.3	mA
Supply Current Side 2	$I_{DD2}$		6.6	10.3		8.3	12.6		13.8	21.5	mA
ADuM263N											
Supply Current Side 1	$I_{DD1}$		7.3	12		8.9	14.2		14.9	22	mA
Supply Current Side 2	$I_{DD2}$		8.5	13.7		9.9	15.6		16	22.3	mA

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 2.5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $2.25\text{ V} \leq V_{DD1} \leq 2.75\text{ V}$ ,  $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>SWITCHING SPECIFICATIONS</b>						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate <sup>1</sup>		150			Mbps	Within PWD limit
Propagation Delay	$t_{PHL}$ , $t_{PLH}$	5.0	7.0	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	5.0	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/ $^\circ\text{C}$	
Propagation Delay Skew	$t_{PSK}$			6.8	ns	Between any two units at the same temperature, voltage, load
Channel Matching						
Codirectional	$t_{PSKCD}$		0.7	5.0	ns	
Opposing Direction	$t_{PSKOD}$		0.7	5.0	ns	
Jitter			800		ps p-p	See the <a href="#">Jitter Measurement</a> section
			190		ps rms	See the <a href="#">Jitter Measurement</a> section
<b>DC SPECIFICATIONS</b>						
Input Threshold Voltage						
Logic High	$V_{IH}$	$0.7 \times V_{DDx}$			V	
Logic Low	$V_{IL}$			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{Ox}^2 = -20\ \mu\text{A}$ , $V_{Ix} = V_{IxH}^3$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox}^2 = -2\ \text{mA}$ , $V_{Ix} = V_{IxH}^3$
Logic Low	$V_{OL}$		0.0	0.1	V	$I_{Ox}^2 = 20\ \mu\text{A}$ , $V_{Ix} = V_{IxL}^4$
			0.2	0.4	V	$I_{Ox}^2 = 2\ \text{mA}$ , $V_{Ix} = V_{IxL}^4$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Quiescent Supply Current						
ADuM260N						
	$I_{DD1(Q)}$		2.1	3.3	mA	$V_I^5 = 0\ (N0)$ , $1\ (N1)^6$
	$I_{DD2(Q)}$		3.1	4.1	mA	$V_I^5 = 0\ (N0)$ , $1\ (N1)^6$
	$I_{DD1(Q)}$		19	27.7	mA	$V_I^5 = 1\ (N0)$ , $0\ (N1)^6$
	$I_{DD2(Q)}$		3.3	4.6	mA	$V_I^5 = 1\ (N0)$ , $0\ (N1)^6$
ADuM261N						
	$I_{DD1(Q)}$		2.2	3.5	mA	$V_I^5 = 0\ (N0)$ , $1\ (N1)^6$
	$I_{DD2(Q)}$		2.9	3.9	mA	$V_I^5 = 0\ (N0)$ , $1\ (N1)^6$
	$I_{DD1(Q)}$		15.7	24.5	mA	$V_I^5 = 1\ (N0)$ , $0\ (N1)^6$
	$I_{DD2(Q)}$		6.9	10.9	mA	$V_I^5 = 1\ (N0)$ , $0\ (N1)^6$
ADuM262N						
	$I_{DD1(Q)}$		2.5	3.7	mA	$V_I^5 = 0\ (N0)$ , $1\ (N1)^6$
	$I_{DD2(Q)}$		2.7	3.9	mA	$V_I^5 = 0\ (N0)$ , $1\ (N1)^6$
	$I_{DD1(Q)}$		13.8	22.1	mA	$V_I^5 = 1\ (N0)$ , $0\ (N1)^6$
	$I_{DD2(Q)}$		10.2	16.4	mA	$V_I^5 = 1\ (N0)$ , $0\ (N1)^6$
ADuM263N						
	$I_{DD1(Q)}$		2.7	4.08	mA	$V_I^5 = 0\ (N0)$ , $1\ (N1)^6$
	$I_{DD2(Q)}$		2.55	3.72	mA	$V_I^5 = 0\ (N0)$ , $1\ (N1)^6$
	$I_{DD1(Q)}$		11.5	18.4	mA	$V_I^5 = 1\ (N0)$ , $0\ (N1)^6$



## SPECIFICATIONS

Table 5. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current	$I_{DD2(Q)}$		14.3	22.3	mA	$V_I^5 = 1 (N0), 0 (N1)^6$
Dynamic Input	$I_{DDI(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout						
Positive $V_{DDx}$ Threshold	$V_{DDxUV+}$		1.6		V	
Negative $V_{DDx}$ Threshold	$V_{DDxUV-}$		1.5		V	
$V_{DDx}$ Hysteresis	$V_{DDxUVH}$		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	$t_R/t_F$		2.5		ns	10% to 90%
Common-Mode Transient Immunity <sup>7</sup>	$ CM_H $	75	100		kV/ $\mu$ s	$V_{IX} = V_{DDx}, V_{CM} = 1000$ V, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ $\mu$ s	$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

<sup>1</sup> 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

<sup>2</sup>  $I_{Ox}$  is the Channel x output current, where x = A, B, C, D, E, or F.

<sup>3</sup>  $V_{IXH}$  is the input side logic high.

<sup>4</sup>  $V_{IXL}$  is the input side logic low.

<sup>5</sup>  $V_I$  is the voltage input.

<sup>6</sup> N0 refers to the ADuM260N0/ADuM261N0/ADuM262N0/ADuM263N0 models. N1 refers to the ADuM260N1/ADuM261N1/ADuM262N1/ADuM263N1 models. See the [Ordering Guide](#) section.

<sup>7</sup>  $|CM_H|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output ( $V_O$ ) > 0.8  $V_{DDx}$ .  $|CM_L|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O$  > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM260N											
Supply Current Side 1	$I_{DD1}$		10.4	15.4		11.2	18.4		16	24	mA
Supply Current Side 2	$I_{DD2}$		3.3	5.3		4.8	7.2		9.8	17.9	mA
ADuM261N											
Supply Current Side 1	$I_{DD1}$		8.9	14.1		10.1	16.3		14.8	23.6	mA
Supply Current Side 2	$I_{DD2}$		5.0	8.7		6.5	11.1		11.4	20.1	mA
ADuM262N											
Supply Current Side 1	$I_{DD1}$		8.1	12.6		9.4	14.4		14.1	23.2	mA
Supply Current Side 2	$I_{DD2}$		6.5	10.2		7.8	12.1		12.4	20.1	mA
ADuM263N											
Supply Current Side 1	$I_{DD1}$		7.1	11.9		8.5	13.9		13.6	21	mA
Supply Current Side 2	$I_{DD2}$		8.3	13.4		9.7	15.2		14.8	21.3	mA

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 1.8\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range:  $1.7\text{ V} \leq V_{DD1} \leq 1.9\text{ V}$ ,  $1.7\text{ V} \leq V_{DD2} \leq 1.9\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>SWITCHING SPECIFICATIONS</b>						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate <sup>1</sup>		150			Mbps	Within PWD limit
Propagation Delay	$t_{PHL}$ , $t_{PLH}$	5.8	8.7	15	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	5.0	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/ $^\circ\text{C}$	
Propagation Delay Skew	$t_{PSK}$			7.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	$t_{PSKCD}$		0.7	5.0	ns	
Opposing Direction	$t_{PSKOD}$		0.7	5.0	ns	
Jitter			470		ps p-p	See the <a href="#">Jitter Measurement</a> section
			70		ps rms	See the <a href="#">Jitter Measurement</a> section
<b>DC SPECIFICATIONS</b>						
Input Threshold Voltage						
Logic High	$V_{IH}$	$0.7 \times V_{DDx}$			V	
Logic Low	$V_{IL}$			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	$V_{OH}$	$V_{DDx} - 0.1$	$V_{DDx}$		V	$I_{Ox}^2 = -20\ \mu\text{A}$ , $V_{Ix} = V_{IxH}^3$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox}^2 = -2\ \text{mA}$ , $V_{Ix} = V_{IxH}^3$
Logic Low	$V_{OL}$		0.0	0.1	V	$I_{Ox}^2 = 20\ \mu\text{A}$ , $V_{Ix} = V_{IxL}^4$
			0.2	0.4	V	$I_{Ox}^2 = 2\ \text{mA}$ , $V_{Ix} = V_{IxL}^4$
Input Current per Channel	$I_I$	-10	+0.01	+10	$\mu\text{A}$	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Quiescent Supply Current						
ADuM260N						
	$I_{DD1(Q)}$		2.0	3.2	mA	$V_I^5 = 0\text{ (NO)}$ , $1\text{ (N1)}^6$
	$I_{DD2(Q)}$		3.0	4.0	mA	$V_I^5 = 0\text{ (NO)}$ , $1\text{ (N1)}^6$
	$I_{DD1(Q)}$		18.7	27.4	mA	$V_I^5 = 1\text{ (NO)}$ , $0\text{ (N1)}^6$
	$I_{DD2(Q)}$		3.3	4.6	mA	$V_I^5 = 1\text{ (NO)}$ , $0\text{ (N1)}^6$
ADuM261N						
	$I_{DD1(Q)}$		2.1	3.4	mA	$V_I^5 = 0\text{ (NO)}$ , $1\text{ (N1)}^6$
	$I_{DD2(Q)}$		2.9	3.9	mA	$V_I^5 = 0\text{ (NO)}$ , $1\text{ (N1)}^6$
	$I_{DD1(Q)}$		15.5	24.3	mA	$V_I^5 = 1\text{ (NO)}$ , $0\text{ (N1)}^6$
	$I_{DD2(Q)}$		6.8	10.8	mA	$V_I^5 = 1\text{ (NO)}$ , $0\text{ (N1)}^6$
ADuM262N						
	$I_{DD1(Q)}$		2.4	3.6	mA	$V_I^5 = 0\text{ (NO)}$ , $1\text{ (N1)}^6$
	$I_{DD2(Q)}$		2.7	3.9	mA	$V_I^5 = 0\text{ (NO)}$ , $1\text{ (N1)}^6$
	$I_{DD1(Q)}$		13.7	22	mA	$V_I^5 = 1\text{ (NO)}$ , $0\text{ (N1)}^6$
	$I_{DD2(Q)}$		10.1	16.3	mA	$V_I^5 = 1\text{ (NO)}$ , $0\text{ (N1)}^6$
ADuM263N						
	$I_{DD1(Q)}$		2.6	4.03	mA	$V_I^5 = 0\text{ (NO)}$ , $1\text{ (N1)}^6$
	$I_{DD2(Q)}$		2.5	3.72	mA	$V_I^5 = 0\text{ (NO)}$ , $1\text{ (N1)}^6$
	$I_{DD1(Q)}$		11.3	18.3	mA	$V_I^5 = 1\text{ (NO)}$ , $0\text{ (N1)}^6$

## SPECIFICATIONS

Table 7. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current	$I_{DD2(Q)}$		14	22	mA	$V_I^5 = 1$ (N0), 0 (N1) <sup>6</sup>
Dynamic Input	$I_{DD1(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive $V_{DDx}$ Threshold	$V_{DDxUV+}$		1.6		V	
Negative $V_{DDx}$ Threshold	$V_{DDxUV-}$		1.5		V	
$V_{DDx}$ Hysteresis	$V_{DDxUVH}$		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	$t_R/t_F$		2.5		ns	10% to 90%
Common-Mode Transient Immunity <sup>7</sup>	$ CM_H $	75	100		kV/ $\mu$ s	$V_{IX} = V_{DDx}$ , $V_{CM} = 1000$ V, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ $\mu$ s	$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

<sup>1</sup> 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

<sup>2</sup>  $I_{Ox}$  is the Channel x output current, where x = A, B, C, D, E, or F.

<sup>3</sup>  $V_{ixH}$  is the input side logic high.

<sup>4</sup>  $V_{ixL}$  is the input side logic low.

<sup>5</sup>  $V_I$  is the voltage input.

<sup>6</sup> N0 refers to the ADuM260N0/ADuM261N0/ADuM262N0/ADuM263N0 models. N1 refers to the ADuM260N1/ADuM261N1/ADuM262N1/ADuM263N1 models. See the [Ordering Guide](#) section.

<sup>7</sup>  $|CM_H|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output ( $V_O$ ) > 0.8  $V_{DDx}$ .  $|CM_L|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O$  > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 8. Total Supply Current vs. Data Throughput

Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM260N											
Supply Current Side 1	$I_{DD1}$		10.2	15.2		11.3	18.2		15.9	23.9	mA
Supply Current Side 2	$I_{DD2}$		3.3	5.3		4.8	7.2		9.8	17.9	mA
ADuM261N											
Supply Current Side 1	$I_{DD1}$		8.7	13.9		10	16.2		14.6	23.4	mA
Supply Current Side 2	$I_{DD2}$		4.9	8.6		6.4	11		11.4	20.1	mA
ADuM262N											
Supply Current Side 1	$I_{DD1}$		8.0	12.5		9.2	14.2		13.9	23	mA
Supply Current Side 2	$I_{DD2}$		6.4	10.1		7.7	12		12.4	20.1	mA
ADuM263N											
Supply Current Side 1	$I_{DD1}$		7.0	11.8		8.3	13.7		13.3	20.7	mA
Supply Current Side 2	$I_{DD2}$		8.2	13.3		9.5	15		14.5	21	mA

## SPECIFICATIONS

## INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see [www.analog.com/icouplersafety](http://www.analog.com/icouplersafety).

Table 9.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V <sub>RMS</sub>	1-minute duration
Minimum External Air Gap (Clearance) <sup>1, 2</sup>	L (I01)	8.7	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage) <sup>1</sup>	L (I02)	8.7	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		29	μm	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index) <sup>3</sup>	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

<sup>1</sup> In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

<sup>2</sup> Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

<sup>3</sup> CTI rating for the ADuM260N/ADuM261N/ADuM262N/ADuM263N is >400 V and a Material Group II isolation group.

## PACKAGE CHARACTERISTICS

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>13</sup>		Ω	
Capacitance (Input to Output) <sup>1</sup>	C <sub>I-O</sub>		2.2		pF	f = 1 MHz
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ <sub>JA</sub>		45		°C/W	Thermocouple located at center of package underside

<sup>1</sup> The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

## SPECIFICATIONS

## REGULATORY INFORMATION

See the [Insulation Lifetime](#) section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

The ADuM260N/ADuM261N/ADuM262N/ADuM263N certification approvals are listed in [Table 11](#).

**Table 11.**

UL	CSA	VDE	CQC
UL 1577 <sup>1</sup> Single Protection, 5000 V <sub>RMS</sub>	IEC/EN/CSA 62368-1 Basic insulation, 870 V <sub>RMS</sub> Reinforced insulation, 435 V <sub>RMS</sub> IEC/CSA 60601-1 Reinforced insulation (2 MOPP), 276 V <sub>RMS</sub> IEC/CSA 61010-1 Basic insulation, 600 V <sub>RMS</sub> , overvoltage category IV Reinforced insulation, 300 V <sub>RMS</sub>	DIN EN IEC 60747-17 (VDE 0884-17) <sup>2</sup> Reinforced insulation, 849 V <sub>PEAK</sub>	CQC GB4943.1 Basic insulation, 830 V <sub>RMS</sub> Reinforced insulation, 415 V <sub>RMS</sub>
File E214100	File No. 205078	Certificate No. 40051926	Certificate No. CQC18001192420

<sup>1</sup> In accordance with UL 1577, each ADuM260N/ADuM261N/ADuM262N/ADuM263N in the RI-16 wide body (SOIC\_IC) package is proof tested by applying an insulation test voltage  $\geq 6000$  V<sub>RMS</sub> for 1 sec.

<sup>2</sup> In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM260N/ADuM261N/ADuM262N/ADuM263N in the RI-16 wide body (SOIC\_IC) package is proof tested by applying an insulation test voltage  $\geq 1592$  V<sub>PEAK</sub> for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

**SPECIFICATIONS**

**DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS**

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The \* marking on packages denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

**Table 12.**

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110			I to IV	
For Rated Mains Voltage ≤ 150 V <sub>RMS</sub>			I to IV	
For Rated Mains Voltage ≤ 300 V <sub>RMS</sub>			I to III	
For Rated Mains Voltage ≤ 600 V <sub>RMS</sub>			40/125/21	
Climatic Classification			2	
Pollution Degree per DIN VDE 0110, Table 1				
Maximum Repetitive Isolation Voltage		V <sub>IORM</sub>	849	V <sub>PEAK</sub>
Maximum Working Isolation Voltage		V <sub>IOWM</sub>	600	V <sub>RMS</sub>
Input to Output Test Voltage, Method B1	V <sub>IORM</sub> × 1.875 = V <sub>pd(m)</sub> , 100% production test, t <sub>ini</sub> = t <sub>m</sub> = 1 sec, partial discharge < 5 pC	V <sub>pd(m)</sub>	1592	V <sub>PEAK</sub>
Input to Output Test Voltage, Method A		V <sub>pd(m)</sub>		
After Environmental Tests Subgroup 1	V <sub>IORM</sub> × 1.6 = V <sub>pd(m)</sub> , t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec, partial discharge < 5 pC		1358	V <sub>PEAK</sub>
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V <sub>IORM</sub> × 1.2 = V <sub>pd(m)</sub> , t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec, partial discharge < 5 pC		1019	V <sub>PEAK</sub>
Maximum Transient Isolation Voltage	V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1s (100% production)	V <sub>IOTM</sub>	8000	V <sub>PEAK</sub>
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V <sub>IMP</sub>	8000	V <sub>PEAK</sub>
Maximum Surge Isolation Voltage	V <sub>TEST</sub> ≥ 1.3 × V <sub>IMP</sub> (sample test), tested in oil, waveform per IEC 61000-4-5	V <sub>IOSM</sub>	10,000	V <sub>PEAK</sub>
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 5)			
Maximum Junction Temperature		T <sub>S</sub>	150	°C
Total Power Dissipation at 25°C		P <sub>S</sub>	2.78	W
Insulation Resistance at T <sub>S</sub>		R <sub>S</sub>	>10 <sup>9</sup>	Ω

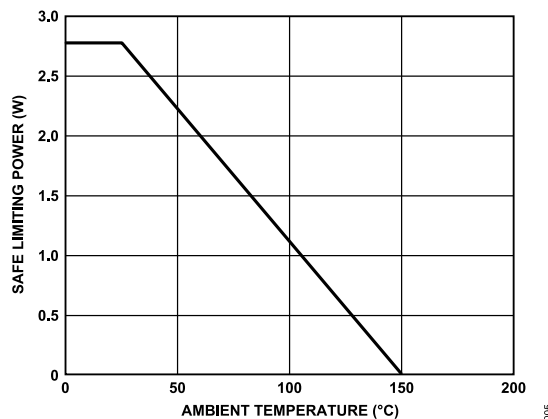


Figure 5. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

## SPECIFICATIONS

## RECOMMENDED OPERATING CONDITIONS

Table 13.

Parameter	Symbol	Rating
Operating Temperature	$T_A$	-40°C to +125°C
Supply Voltages	$V_{DD1}, V_{DD2}$	1.7 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 14.**

Parameter	Rating
Storage Temperature ( $T_{ST}$ ) Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Ambient Operating Temperature ( $T_A$ ) Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Supply Voltages ( $V_{DD1}$ , $V_{DD2}$ )	$-0.5\text{ V}$ to $+7.0\text{ V}$
Input Voltages ( $V_{IA}$ , $V_{IB}$ , $V_{IC}$ , $V_{ID}$ , $V_{IE}$ , $V_{IF}$ )	$-0.5\text{ V}$ to $V_{DD1}^1 + 0.5\text{ V}$
Output Voltages ( $V_{OA}$ , $V_{OB}$ , $V_{OC}$ , $V_{OD}$ , $V_{OE}$ , $V_{OF}$ )	$-0.5\text{ V}$ to $V_{DDO}^2 + 0.5\text{ V}$
Average Output Current per Pin <sup>3</sup>	
Side 1 Output Current ( $I_{O1}$ )	$-10\text{ mA}$ to $+10\text{ mA}$
Side 2 Output Current ( $I_{O2}$ )	$-10\text{ mA}$ to $+10\text{ mA}$
Common-Mode Transients <sup>4</sup>	$-150\text{ kV}/\mu\text{s}$ to $+150\text{ kV}/\mu\text{s}$

<sup>1</sup>  $V_{DD1}$  is the input side supply voltage.

<sup>2</sup>  $V_{DDO}$  is the output side supply voltage.

<sup>3</sup> See [Figure 5](#) for the maximum rated current values for various temperatures.

<sup>4</sup> Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## MAXIMUM CONTINUOUS WORKING VOLTAGE

**Table 15. Maximum Continuous Working Voltage<sup>1</sup>**

Parameter	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	849 $V_{PEAK}$	50-year minimum insulation lifetime
Reinforced Insulation	819 $V_{PEAK}$	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Unipolar Waveform		
Basic Insulation	1698 $V_{PEAK}$	50-year minimum insulation lifetime
Reinforced Insulation	943 $V_{PEAK}$	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
DC Voltage		
Basic Insulation	1157 $V_{PEAK}$	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Reinforced Insulation	579 $V_{PEAK}$	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1

<sup>1</sup> Refers to the continuous voltage magnitude imposed across the isolation barrier. See the [Insulation Lifetime](#) section for more details.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## ABSOLUTE MAXIMUM RATINGS

## TRUTH TABLE

Table 16. ADuM260N/ADuM261N/ADuM262N/ADuM263N Truth Table (Positive Logic)

$V_{IX}$ Input <sup>1, 2</sup>	$V_{DDI}$ State <sup>2</sup>	$V_{DDO}$ State <sup>2</sup>	Default Low (N0), $V_{Ox}$ Output <sup>1, 2, 3</sup>	Default High (N1), $V_{Ox}$ Output <sup>1, 2, 3</sup>	Test Conditions/Comments
L	Powered	Powered	L	L	Normal operation
H	Powered	Powered	H	H	Normal operation
L	Unpowered	Powered	L	H	Fail-safe output
X <sup>4</sup>	Powered	Unpowered	Indeterminate	Indeterminate	Output Unpowered

<sup>1</sup> L means low, H means high, and X means don't care.

<sup>2</sup>  $V_{IX}$  and  $V_{OX}$  refer to the input and output signals of a given channel (A, B, C, D, E or F).  $V_{DDI}$  and  $V_{DDO}$  refer to the supply voltages on the input and output sides of the given channel, respectively.

<sup>3</sup> N0 refers to the ADuM260N0/ADuM261N0/ADuM262N0/ADuM263N0 models. N1 refers to the ADuM260N1/ADuM261N1/ADuM262N1/ADuM263N1 models. See the Ordering Guide section.

<sup>4</sup> Input pins ( $V_{IX}$ ) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

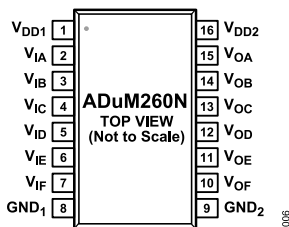


Figure 6. ADuM260N Pin Configuration

Table 17. ADuM260N Pin Function Descriptions

Pin No. <sup>1</sup>	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	V <sub>IA</sub>	Logic Input A.
3	V <sub>IB</sub>	Logic Input B.
4	V <sub>IC</sub>	Logic Input C.
5	V <sub>ID</sub>	Logic Input D.
6	V <sub>IE</sub>	Logic Input E.
7	V <sub>IF</sub>	Logic Input F.
8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	V <sub>OF</sub>	Logic Output F.
11	V <sub>OE</sub>	Logic Output E.
12	V <sub>OD</sub>	Logic Output D.
13	V <sub>OC</sub>	Logic Output C.
14	V <sub>OB</sub>	Logic Output B.
15	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

<sup>1</sup> Reference the [AN-1109](#) Application Note for specific layout guidelines.

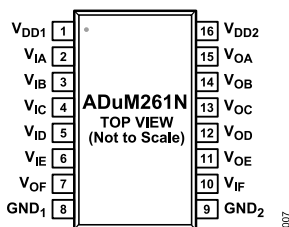


Figure 7. ADuM261N Pin Configuration

Table 18. ADuM261N Pin Function Descriptions

Pin No. <sup>1</sup>	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	V <sub>IA</sub>	Logic Input A.
3	V <sub>IB</sub>	Logic Input B.
4	V <sub>IC</sub>	Logic Input C.
5	V <sub>ID</sub>	Logic Input D.
6	V <sub>IE</sub>	Logic Input E.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 18. ADuM261N Pin Function Descriptions (Continued)

Pin No. <sup>1</sup>	Mnemonic	Description
7	V <sub>OF</sub>	Logic Output F.
8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	V <sub>IF</sub>	Logic Input F.
11	V <sub>OE</sub>	Logic Output E.
12	V <sub>OD</sub>	Logic Output D.
13	V <sub>OC</sub>	Logic Output C.
14	V <sub>OB</sub>	Logic Output B.
15	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

<sup>1</sup> Reference the AN-1109 Application Note for specific layout guidelines.

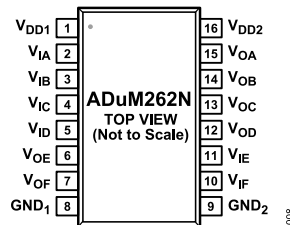


Figure 8. ADuM262N Pin Configuration

Table 19. ADuM262N Pin Function Descriptions

Pin No. <sup>1</sup>	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	V <sub>IA</sub>	Logic Input A.
3	V <sub>IB</sub>	Logic Input B.
4	V <sub>IC</sub>	Logic Input C.
5	V <sub>ID</sub>	Logic Input D.
6	V <sub>OE</sub>	Logic Output E.
7	V <sub>OF</sub>	Logic Output F.
8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	V <sub>IF</sub>	Logic Input F.
11	V <sub>IE</sub>	Logic Input E.
12	V <sub>OD</sub>	Logic Output D.
13	V <sub>OC</sub>	Logic Output C.
14	V <sub>OB</sub>	Logic Output B.
15	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

<sup>1</sup> Reference the AN-1109 Application Note for specific layout guidelines.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

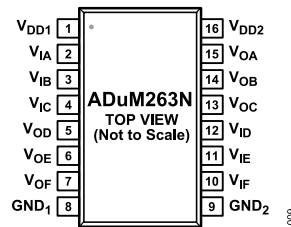


Figure 9. ADuM263N Pin Configuration

Table 20. ADuM263N Pin Function Descriptions

Pin No. <sup>1</sup>	Mnemonic	Description
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1.
2	V <sub>IA</sub>	Logic Input A.
3	V <sub>IB</sub>	Logic Input B.
4	V <sub>IC</sub>	Logic Input C.
5	V <sub>OD</sub>	Logic Output D.
6	V <sub>OE</sub>	Logic Output E.
7	V <sub>OF</sub>	Logic Output F.
8	GND <sub>1</sub>	Ground 1. Ground reference for Isolator Side 1.
9	GND <sub>2</sub>	Ground 2. Ground reference for Isolator Side 2.
10	V <sub>IF</sub>	Logic Input F.
11	V <sub>IE</sub>	Logic Input E.
12	V <sub>ID</sub>	Logic Input D.
13	V <sub>OC</sub>	Logic Output C.
14	V <sub>OB</sub>	Logic Output B.
15	V <sub>OA</sub>	Logic Output A.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 2.

<sup>1</sup> Reference the [AN-1109](#) Application Note for specific layout guidelines.

TYPICAL PERFORMANCE CHARACTERISTICS

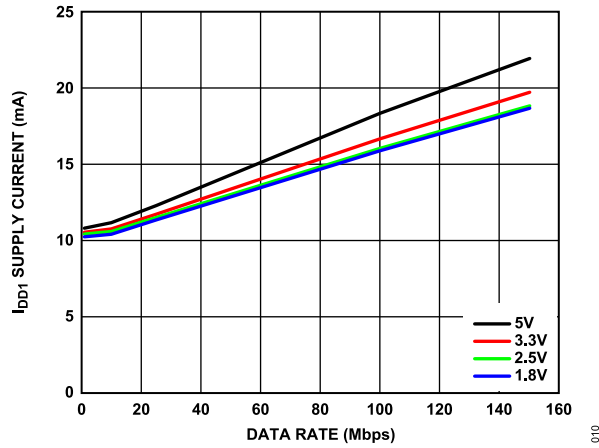


Figure 10. ADuM260N  $I_{DD1}$  Supply Current vs. Data Rate at Various Voltages

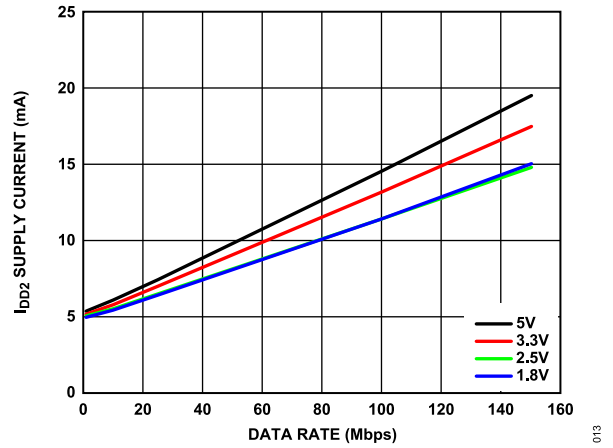


Figure 13. ADuM261N  $I_{DD2}$  Supply Current vs. Data Rate at Various Voltages

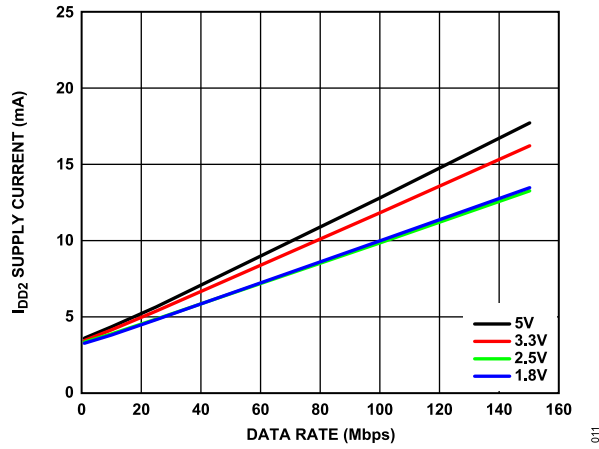


Figure 11. ADuM260N  $I_{DD2}$  Supply Current vs. Data Rate at Various Voltages

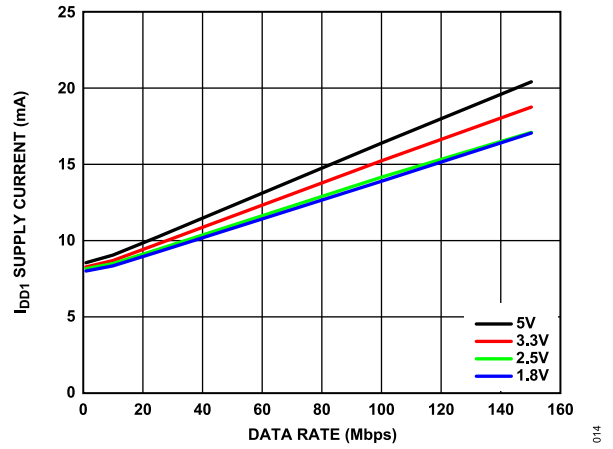


Figure 14. ADuM262N  $I_{DD1}$  Supply Current vs. Data Rate at Various Voltages

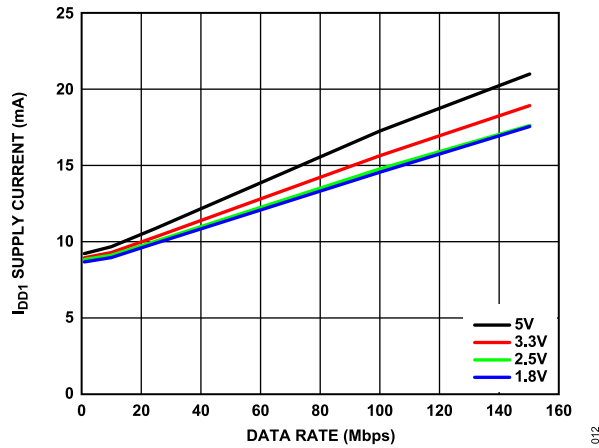


Figure 12. ADuM261N  $I_{DD1}$  Supply Current vs. Data Rate at Various Voltages

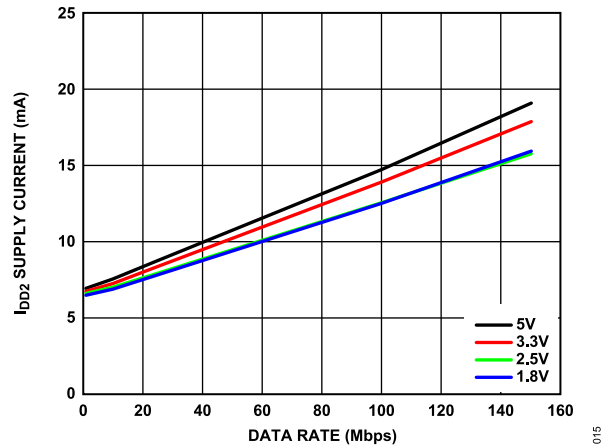


Figure 15. ADuM262N  $I_{DD2}$  Supply Current vs. Data Rate at Various Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

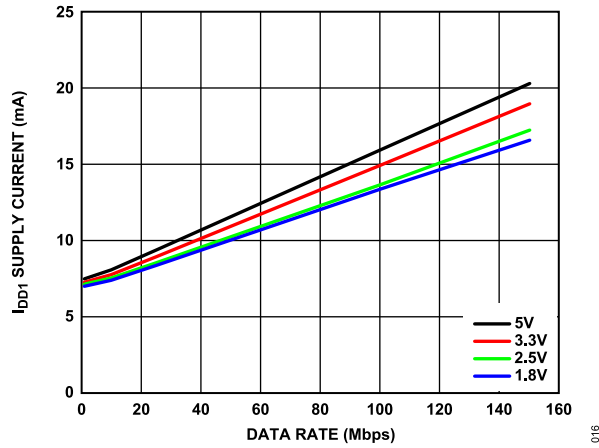


Figure 16. ADuM263N  $I_{DD1}$  Supply Current vs. Data Rate at Various Voltages

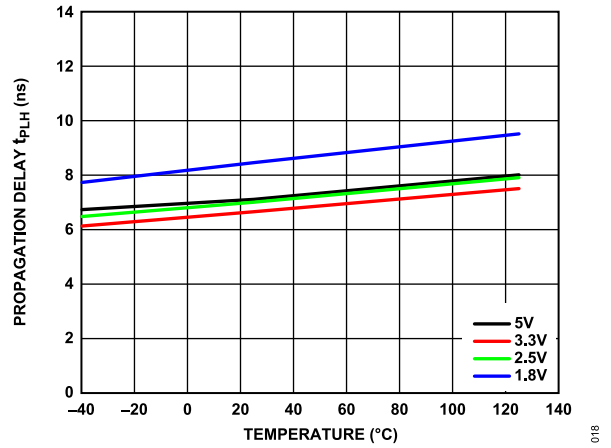


Figure 18. Propagation Delay,  $t_{PLH}$  vs. Temperature at Various Voltages

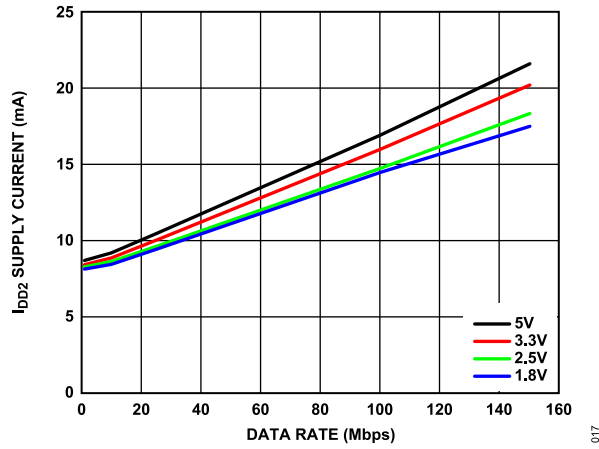


Figure 17. ADuM263N  $I_{DD2}$  Supply Current vs. Data Rate at Various Voltages

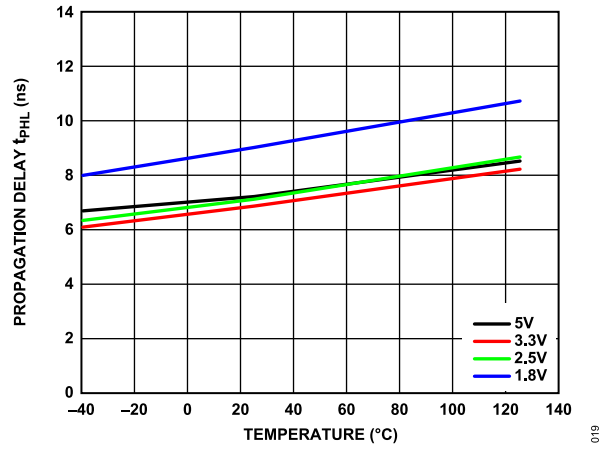


Figure 19. Propagation Delay,  $t_{PHL}$  vs. Temperature at Various Voltages

## THEORY OF OPERATION

The ADuM260N/ADuM261N/ADuM262N/ADuM263N use a high frequency carrier to transmit data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 20 and Figure 21, the ADuM260N/ADuM261N/ADuM262N/ADuM263N have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 20 shows the waveforms for models of the ADuM260N0/ADuM261N0/ADuM262N0/ADuM263N0 that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the fail-safe output state of low sets the output to low. For the ADuM260N1/ADuM261N1/ADuM262N1/ADuM263N1 that have a fail-safe output state of high, Figure 21 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the fail-safe output state of high sets the output to high. See the Ordering Guide for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

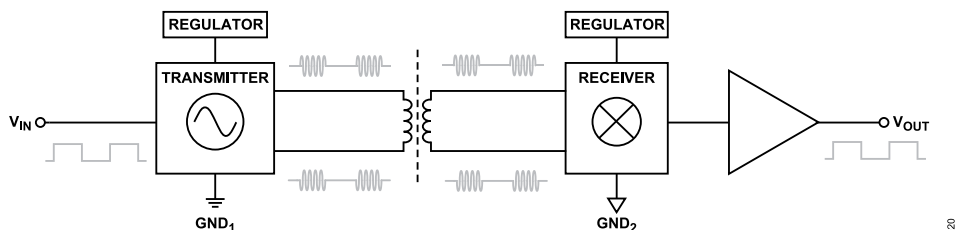


Figure 20. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

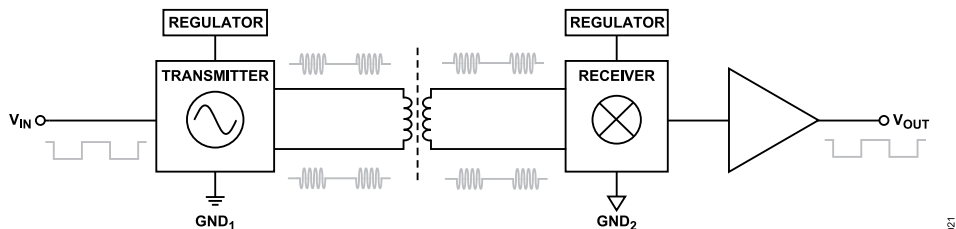


Figure 21. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

## APPLICATIONS INFORMATION

### PCB LAYOUT

The ADuM260N/ADuM261N/ADuM262N/ADuM263N digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 22). Bypass capacitors are connected between Pin 1 and Pin 8 for  $V_{DD1}$  and between Pin 9 and Pin 16 for  $V_{DD2}$ . The recommended bypass capacitor value is between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ . The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.

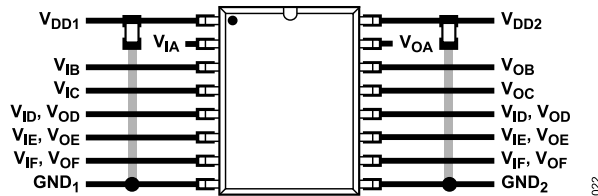


Figure 22. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the [Absolute Maximum Ratings](#) of the device, thereby leading to latch-up or permanent damage.

See the [AN-1109 Application Note](#) for board layout guidelines.

### PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

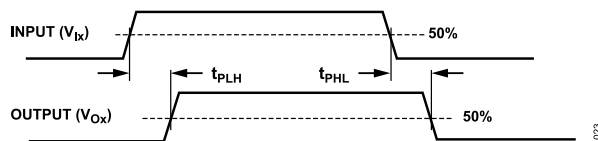


Figure 23. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single ADuM260N/ADuM261N/ADuM262N/ADuM263N component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple ADuM260N/ADuM261N/ADuM262N/ADuM263N components operating under the same conditions.

### JITTER MEASUREMENT

Figure 24 illustrates the eye diagram for the ADuM260N/ADuM261N/ADuM262N/ADuM263N. The measurement was taken using an Agilent 81110A pulse pattern generator at 150 Mbps with pseudorandom bit sequences (PRBS)  $2(n - 1)$ ,  $n = 14$ , for 5 V supplies. Jitter was measured with the Tektronix Model 5104B oscilloscope, 1 GHz, 10 GSPS with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the ADuM260N/ADuM261N/ADuM262N/ADuM263N with 490 ps p-p jitter.

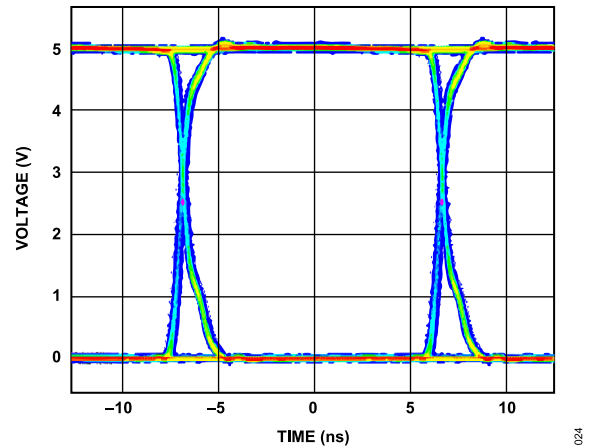


Figure 24. ADuM260N/ADuM261N/ADuM262N/ADuM263N Eye Diagram

### INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking, and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

#### Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in



## APPLICATIONS INFORMATION

each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM260N/ADuM261N/ADuM262N/ADuM263N isolators are presented in [Table 9](#).

### Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as: dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltages. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in [Equation 1](#). Because only the ac portion of the stress causes wear out, [Equation 1](#) can be rearranged to solve for the ac rms voltage, as is shown in [Equation 2](#). For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2} \quad (1)$$

or

$$V_{RMS} = \sqrt{V_{RMS}^2 + V_{DC}^2} \quad (2)$$

where:

$V_{AC\ RMS}$  is the time varying portion of the working voltage.

$V_{RMS}$  is the total rms working voltage.

$V_{DC}$  is the dc offset of the working voltage.

### Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240  $V_{AC\ RMS}$ , a 400  $V_{DC}$  bus voltage is present on the other side of the isolation barrier, and the isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance and lifetime of a device, see [Figure 25](#) and the following equations.

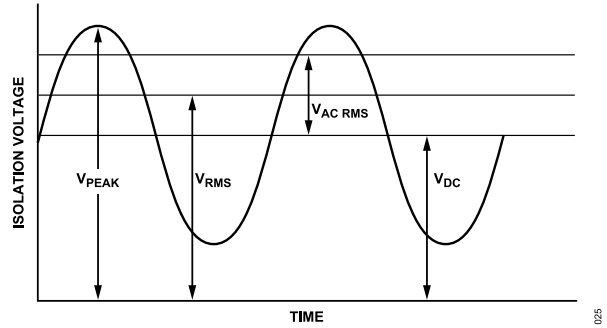


Figure 25. Critical Voltage Example

The working voltage across the barrier from [Equation 1](#) is

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{AC\ RMS} = 466\ V\ rms$$

This  $V_{RMS}$  value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use [Equation 2](#).

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 + V_{DC}^2}$$

$$V_{RMS} = \sqrt{466^2 + 400^2}$$

$$V_{AC\ RMS} = 240\ V_{RMS}$$

In this case, the ac rms voltage is simply the line voltage of 240  $V_{RMS}$ . This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in [Table 15](#) for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit in [Table 15](#) is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

## OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RI-16-2	SOIC_IC	16-Lead Standard Small Outline Package, with Increased Creepage

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

## ORDERING GUIDE

Model <sup>1,2</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM260N1BRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM260N1BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2
ADuM260N0BRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM260N0BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2
ADuM261N1BRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM261N1BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2
ADuM261N0BRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM261N0BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2
ADuM262N1BRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM262N1BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2
ADuM262N1WBRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM262N1WBRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2
ADuM262N0BRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM262N0BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2
ADuM263N1BRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM263N1BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2
ADuM263N0BRIZ	-40°C to +125°C	16-Lead SOIC_IC	Tube, 37	RI-16-2
ADuM263N0BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	Reel, 1000	RI-16-2

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications.

## NO. OF INPUTS, WITHSTAND VOLTAGE RATING, AND FAIL-SAFE OUTPUT STATE OPTIONS

Model <sup>1,2</sup>	No. of Inputs, V <sub>DD1</sub> Side	No. of Inputs, V <sub>DD2</sub> Side	Withstand Voltage Rating (kV <sub>RMS</sub> )	Fail-Safe Output State
ADuM260N1BRIZ	6	0	5.0	High
ADuM260N1BRIZ-RL	6	0	5.0	High
ADuM260N0BRIZ	6	0	5.0	Low
ADuM260N0BRIZ-RL	6	0	5.0	Low
ADuM261N1BRIZ	5	1	5.0	High
ADuM261N1BRIZ-RL	5	1	5.0	High
ADuM261N0BRIZ	5	1	5.0	Low
ADuM261N0BRIZ-RL	5	1	5.0	Low
ADuM262N1BRIZ	4	2	5.0	High
ADuM262N1BRIZ-RL	4	2	5.0	High
ADuM262N0BRIZ	4	2	5.0	Low
ADuM262N0BRIZ-RL	4	2	5.0	Low
ADuM263N1BRIZ	3	3	5.0	High
ADuM263N1BRIZ-RL	3	3	5.0	High
ADuM263N0BRIZ	3	3	5.0	Low
ADuM263N0BRIZ-RL	3	3	5.0	Low

## OUTLINE DIMENSIONS

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The ADuM262N1WBRIZ and the ADuM262N1BRIZ-RL models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the [Specifications](#) section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.