37.0 GHz to 43.5 GHz Transmit/Receive Dual Polarization Beamformer

Data Sheet

ADMV4928

FEATURES

- **RF range: 37.0 GHz to 43.5 GHz**
- **16 configurable transmit and receive channels**
- **Dual polarization, 8 horizontal and 8 vertical channels**
- **Fast TDD switching time using TRX_x pins**
- **Matched to 50 Ω, single-ended RF inputs and outputs**
- **Single transmitter channel power detector and temperature sensor**
- **Integrated individual receive channel overload detection circuit**
- **High resolution, 6-bit VM for phase control**
- **High resolution, 6-bit and 5-bit DVGAs for amplitude control**
- **Memory for 2048 shared transmit and receive beam positions**
- **NVM for phase and gain calibration**
- **Dual power supplies required: 1.8 V and 1.2 V with on-chip LDO voltage regulator for 1.0 V**
- **3-wire or 4-wire SPI that supports up to 133 MHz SPI clock speed (refer to the AN-2074 Application Note, *ADMV4928 Application Note*)**
- **239-ball, 10 mm × 7 mm CSP_BGA**

APPLICATIONS

- **mmW 5G application**
- **Broadband communication**

GENERAL DESCRIPTION

The ADMV4928 is a silicon on insulator (SOI), 37.0 GHz to 43.5 GHz, mmW 5G beamformer. The RF integrated circuit (RFIC) is highly integrated and contains 16 independent transmit and receive channels. The ADMV4928 supports eight horizontal and eight vertical polarized antennas via independent RFV and RFH input/outputs.

In transmit mode, both the RFV input and RFH input signals feed into separate amplifiers. Each path after the amplifiers splits into eight independent channels via the 1:8 power splitters. In receive mode, input signals pass through either the vertical or horizontal receive channels and combine via two independent 8:1 combiners to the common RFV pin or RFH pin. In either mode, each transmit and receive channel includes a vector modulator (VM) to control the phase, and two digital variable gain amplifiers (DVGAs) to control the amplitude. The VM provides a full 360° phase adjustment range in either transmit or receive mode to provide 6 bits of resolution for 5.625° phase steps. A phase step policy for the transmit and receive VM is provided to ensure optimum phase step performance. The total DVGA dynamic range in transmit mode is 34.5, which provides 6 bits of resolution that results in 0.5 dB amplitude steps and 5 bits of resolution that results in 1 dB amplitude steps. In receive mode, the total dynamic range is 28 dB, which provides 5 bits of resolution that results in 0.5 dB amplitude steps and 5 bits of resolution that results in 1 dB amplitude steps. The DVGAs provide a flat phase response across the full gain range. A gain policy for DVGA1 and DVGA2 is provided in the AN-2074 Application Note, *ADMV4928 Application Note* to ensure optimized performance across the attenuation range with 0.5 dB step resolution from 0 dB to 34.5 dB attenuation for transmit mode and 0.5 dB step resolution from 0 dB to 28 dB attenuation for receive mode. The transmit channels contain individual transmit power detectors to detect either modulated or continuous wave signals to calibrate for each channel gain as well as channel to channel gain mismatch. Each receive channel contains an RF power overload circuit (receive channel overload detection circuit) to prevent potential damage to the device as a result of blocker instances. The ADMV4928 RF ports can be connected directly to a patch antenna to create a dual polarization mmW 5G subarray.

The ADMV4928 can be programmed using a 3-wire or 4-wire serial port interface (SPI). An integrated, on-chip low dropout (LDO) voltage regulator generates the 1.0 V supply for the SPI circuitry to reduce the number of supply domains required. Various SPI modes are available to enable fast startup and control during normal operation. The amplitude and phase for each channel can be set individually or multiple channels can be programmed simultaneously using the on-chip memory for beamforming. The on-chip memory can store up to 2048 beam positions that can be allocated for either transmit mode or receive mode for the horizontal channels and vertical channels. On-chip nonvolatile memory (NVM) is used to store the calibrated gain and phase offset coefficients and the reference values for each individual channel from the factory. These values are used to perform channel to channel or chip to chip calibration. In addition, four address pins (CHIP_ADDx) allow independent SPI control of up to 16 devices on the same serial lines. To control multiple devices via the same serial lines with the same instructions, activate broadcast mode via the external enable pin (BR_EN). Dedicated horizontal and vertical polarization load pins (LOAD_V and LOAD_H) provide the synchronization of all devices in the same array. A horizontal and vertical polarization transmit mode and receive mode control pin (TRX_H or TRX_V) is provided for fast switching between transmit mode and receive mode.

The ADMV4928 comes in a compact, 239-ball, 10 mm × 7 mm chip scale package ball grid array (CSP_BGA). The ADMV4928 operates over the −40°C to +95°C case temperature (T_C) range. This CSP_BGA package enables the ability to heatsink the ADMV4928 from the topside of the package for the most efficient thermal heatsinking and to allow flexible antenna placement on the opposite side of the printed circuit board (PCB).

Rev. Sp0 Document Feedback

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FUNCTIONAL BLOCK DIAGRAM

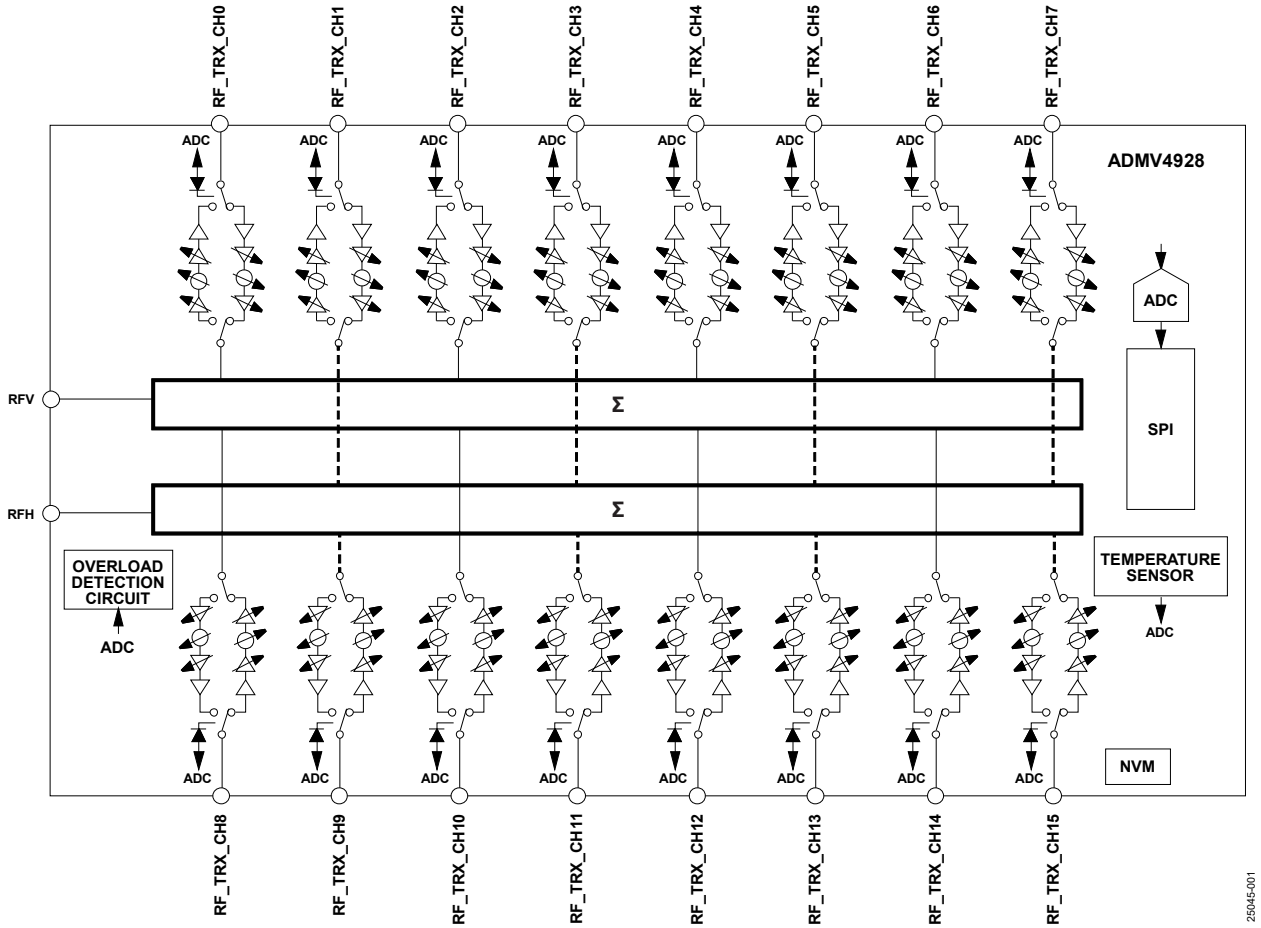

Figure 1. Functional Block Diagram

NOTES

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