16-Channel, 16-Bit Voltage Output denseDAC

Known Good Die

AD5766-KGD

FEATURES

Complete 16-channel, 16-bit DAC
8 software-programmable output ranges: −20 V to 0 V, −16 V to 0 V, −10 V to 0 V, −10 V to +6 V, −12 V to +14 V, −16 V to +10 V, ±5 V and ±10 V
Integrated DAC output buffers with ±20 mA output current capability
Integrated reference buffers
2 dither signal input pads
Channel monitoring multiplexer
1.8 V logic compatibility
Temperature range: −40°C to +105°C

APPLICATIONS

Mach-Zehnder modulator bias control
Optical networking
Instrumentation
Industrial automation
Data acquisition systems
Analog output modules

GENERAL DESCRIPTION

The AD5766-KGD is a 16-channel, 16-bit, voltage output denseDAC® digital-to-analog converter (DAC).

The DAC generates output voltage ranges from an external 2.5 V reference. Depending on the voltage range selected, the midpoint of the output span can be adjusted, allowing a minimum output voltage as low as −20 V or a maximum output voltage of up to +14 V. Each of the 16 channels can be monitored with an integrated output voltage multiplexer.

The AD5766-KGD has integrated output buffers that can sink or source up to 20 mA. In conjunction with these buffers, a low frequency signal can be superimposed onto each DAC output via dedicated dither pads. These dedicated dither pads simplify the system design by reducing the number of external components required for a similar external implementation, like operational amplifiers or resistors. The reduction of external components makes the AD5766-KGD suitable for indium phosphide (InP) Mach-Zehnder modulator (MZM) biasing applications.

The device incorporates a power-on reset (POR) circuit that ensures that the DAC outputs are clamped to ground on power-up and remain at this level until the output range of the DAC is configured. The outputs of all DACs are updated through register configuration, with the added functionality of user-selectable DAC channels to be simultaneously updated.

The AD5766-KGD uses a versatile 4-wire serial interface that operates at clock rates of up to 50 MHz for write mode and is compatible with serial peripheral interface (SPI), QSPI™, MICROWIRE™, and DSP interface standards. The AD5766-KGD also contains a V_{LOGIC} pad intended for 1.8 V/3.3 V/5 V logic.

Additional application and technical information can be found in the AD5766 data sheet.

Known good die (KGD): these die are fully guaranteed to data sheet specifications.

FUNCTIONAL BLOCK DIAGRAM

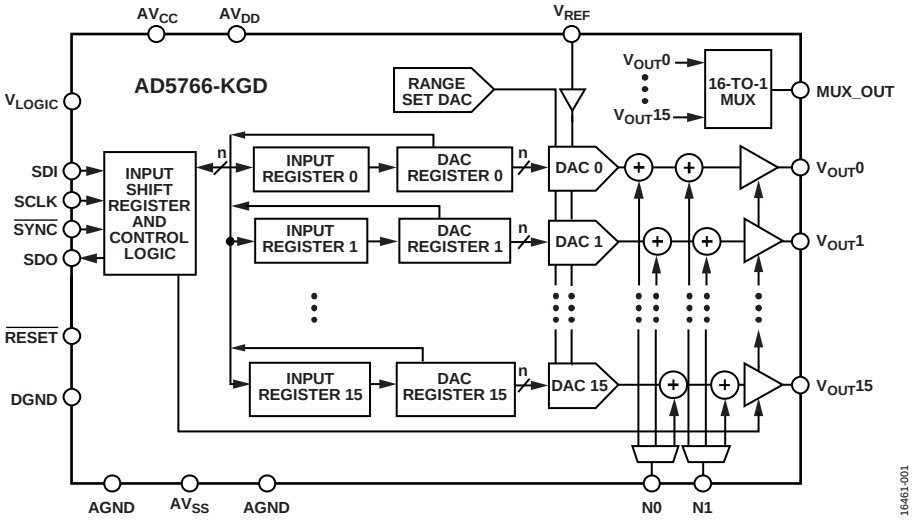

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

2/2018—Revision 0: Initial Version

SPECIFICATIONS

AV_{CC} = 2.97 V to 3.6 V, V_{LOGIC} = 1.7 V to 5.5 V, AV_{DD} = 2.97 V to 16 V, AV_{SS} = −22 V to −7 V, AGND = DGND = 0 V, V_{REF} = 2.5 V, output range = ±5 V, V_{OUT}x unloaded, all specifications T_{MIN} to T_{MAX}, typical specifications at T_A = 25°C, dither powered on, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	
Relative Accuracy (INL)	−16		+16	LSB	
Differential Nonlinearity	−1		+1	LSB	Guaranteed monotonic by design
Bipolar Zero Error	−85	±12	+85	mV	±5 V range
	−110	±13	+110	mV	−10 V to +6 V range
	−120	±15	+120	mV	±10 V range
	−145	±16	+145	mV	−12 V to +14 V range
	−145	±16	+145	mV	−16 V to +10 V range
Bipolar Zero Error Temperature Coefficient (TC)		±2		ppm FSR/°C	
Zero-Scale Error					All 0s loaded to DAC register
	−80	±25	+80	mV	−10 V to 0 V range
	−80	±25	+80	mV	±5 V range
	−110	±35	+110	mV	−16 V to 0 V range
	−110	±35	+110	mV	−10 V to +6 V range
	−130	±35	+130	mV	−20 V to 0 V range
	−130	±35	+130	mV	±10 V range
	−140	±45	+140	mV	−12 V to +14 V range
	−140	±45	+140	mV	−16 V to +10 V range
Zero-Scale Error TC		±2		ppm FSR/°C	
Full-Scale Error					All 1s loaded to DAC register.
	−0.9	±0.23	+0.9	% FSR	−10 V to 0 V range
	−0.9	±0.23	+0.9	% FSR	±5 V range
	−0.8	±0.2	+0.8	% FSR	−16 V to 0 V range
	−0.8	±0.2	+0.8	% FSR	−10 V to +6 V range
	−0.7	±0.18	+0.7	% FSR	−20 V to 0 V range
	−0.7	±0.18	+0.7	% FSR	±10 V range
	−0.6	±0.15	+0.6	% FSR	−12 V to +14 V range
	−0.6	±0.15	+0.6	% FSR	−16 V to +10 V range
Full-Scale Error Drift		±3		ppm FSR/°C	
Gain Error	−0.4	±0.07	+0.4	% FSR	
Gain Error TC		±2		ppm FSR/°C	
Offset Error	−80	±25	+80	mV	−10 V to 0 V range
	−80	±25	+80	mV	±5 V range
	−110	±35	+110	mV	−16 V to 0 V range
	−110	±35	+110	mV	−10 V to +6 V range
	−130	±35	+130	mV	−20 V to 0 V range
	−130	±35	+130	mV	±10 V range
	−140	±45	+140	mV	−12 V to +14 V range
	−140	±45	+140	mV	−16 V to +10 V range
Offset Error Drift		±2		µV/°C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total Unadjusted Error	−0.9	±0.18	+0.9	% FSR	−10 V to 0 V range
	−0.9	±0.18	+0.9	% FSR	±5 V range
	−0.8	±0.15	+0.8	% FSR	−16 V to 0 V range
	−0.8	±0.15	+0.8	% FSR	−10 V to +6 V range
	−0.7	±0.13	+0.7	% FSR	−20 V to 0 V range
	−0.7	±0.13	+0.7	% FSR	±10 V range
	−0.6	±0.12	+0.6	% FSR	−12 V to +14 V range
	−0.6	±0.12	+0.6	% FSR	−16 V to +10 V range
DC Crosstalk		30		µV	Due to output voltage change
		35		µV/mA	Due to load current change (1 LSB)
OUTPUT CHARACTERISTICS					
Output Voltage Ranges[1]	−20		0	V	
	−16		0	V	
	−10		0	V	
	−10		+6	V	
	−12		+14	V	
	−16		+10	V	
	−5		+5	V	
	−10		+10	V	
Output Current	−20		+20	mA	
Capacitive Load Stability			1	nF	
DC Output Impedance		0.2		Ω	
Short-Circuit Current		±60		mA	Single channel only
Output Amplifier Bandwidth		108		kHz	
REFERENCE INPUT					
Reference Input Voltage		2.5		V	±1% for specified performance
Reference Range	2.375		2.625	V	Functional performance only
DC Input Impedance	2.5			MΩ	
Input Current			1	µA	
DITHER INPUTS					
Dither Frequency		10		kHz	Lower −3 dB point
		100		kHz	Upper −3 dB point
Amplitude			0.25	V p-p	Peak-to-peak ac voltage
	0		AV_{CC}	V	Peak-to-peak ac and dc voltage
DC Shift	−2	±1	+2	LSB	
Dither Transient					Dither enabled/disabled, N0 and N1 floating
Dither Selected Channel		5		nV-sec	AV_{CC} = 2.97 V and AV_{CC} = 3.6 V
Dither Nonselected Channels		2		nV-sec	AV_{CC} =2.97 V and AV_{CC} = 3.6 V
Dither Crosstalk[1]		−70		dB	10 kHz dither frequency
		−55		dB	100 kHz dither frequency
LOGIC INPUTS					
Input High Voltage, V_{IH}	0.7 × V_{LOGIC}			V	
Input Low Voltage, V_{IL}			0.3 × V_{LOGIC}	V	
Input Current	−2		+2	µA	Per pad
	−6		+6	µA	$\overline{\text{RESET}}$ pad pulled high
	−57		+57	µA	$\overline{\text{RESET}}$ pad pulled low
Input Capacitance		2		pF	Per pad
LOGIC OUTPUT					
Output Low Voltage			0.4	V	Sinking 200 µA
Output High Voltage	V_{LOGIC} − 0.4			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		5		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE MONITOR PAD (MUX_OUT)					
Impedance		1.3		kΩ	
Three-State Leakage Current	−1	0.006	+1	µA	
Continuous Current	−1		+1	mA	Die temperature below 105°C
Glitch Impulse		0.2		nV-sec	V_{OUT}x glitch due to mux enable
Voltage Settling Time		12		µs	¼ to ¾ scale settling to ±0.5 LSB, ±5 V range and −10 V to 0 V range
POWER SUPPLIES					
AV_{DD}	2.97		16	V	AV_{DD} − AV_{SS} must be less than or equal to 30 V
AV_{SS}	−22		−7	V	AV_{DD} − AV_{SS} must be less than or equal to 30 V
AV_{CC}	2.97		3.6	V	
V_{LOGIC}	1.7		5.5	V	
Headroom/Footroom		±0.7		V	Output voltage offset to ±2 LSB for 20 mA output load; applies to AV_{DD} and AV_{SS}
		±2		V	Output voltage offset to ±1 LSB for 20 mA output load; applies to AV_{DD} and AV_{SS}
Normal Mode					
AI_{DD}		6	9	mA	All output ranges, −40°C to +105°C
AI_{SS}	−11	−9		mA	All output ranges, −40°C to +105°C
AI_{CC}		8.3	10	mA	All output ranges, −40°C to +105°C
I_{LOGIC}		0.02	1	µA	All output ranges, −40°C to +105°C, $V_{IH} = V_{LOGIC}$, V_{IL} = DGND
DC Power Supply Rejection Ratio (PSRR)		50		µV/V	AV_{DD} power supply
		50		µV/V	AV_{SS} power supply
		3		mV/V	AV_{CC} power supply
AC PSRR		−80		dB	AV_{DD} power supply, at 50 Hz
		−80		dB	AV_{SS} power supply, at 50 Hz
		−50		dB	AV_{CC} power supply, at 50 Hz

[1] Output amplifier headroom requirement is 2 V minimum.

AV_{CC} = 2.97 V to 3.6 V, V_{LOGIC} = 1.7 V to 5.5 V, AV_{DD} = 2.97 V to 16 V, AV_{SS} = −22 V to −7 V, AGND = DGND = 0 V, V_{REF} = 2.5 V, output range = ±5 V, $V_{OUT}x$ unloaded, all specifications T_{MIN} to T_{MAX}, typical specifications at T_A = 25°C, dither powered off, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BIPOLAR ZERO ERROR	−50	±11	+50	mV	±5 V range
	−75	±12	+75	mV	−10 V to +6 V range
	−90	±12	+90	mV	±10 V range
	−110	±13	+110	mV	−12 V to +14 V range
	−110	±13	+110	mV	−16 V to +10 V range
ZERO-SCALE ERROR					All 0s loaded to DAC register
	−50	±15	+50	mV	−10 V to 0 V range
	−50	±15	+50	mV	±5 V range
	−75	±20	+75	mV	−16 V to 0 V range
	−75	±20	+75	mV	−10 V to +6 V range
	−90	±25	+90	mV	−20 V to 0 V range
	−90	±25	+90	mV	±10 V range
	−110	±35	+110	mV	−12 V to +14 V range
	−110	±35	+110	mV	−16 V to +10 V range
FULL-SCALE ERROR	−0.5	±0.15	+0.5	% FSR	All 1s loaded to DAC register; all output ranges
GAIN ERROR	−0.3	±0.07	+0.3	% FSR	All output ranges
OFFSET ERROR	−50	±15	+50	mV	−10 V to 0 V range
	−50	±15	+50	mV	±5 V range
	−75	±20	+75	mV	−16 V to 0 V range
	−75	±20	+75	mV	−10 V to +6 V range
	−90	±25	+90	mV	−20 V to 0 V range
	−90	±25	+90	mV	±10 V range
	−110	±35	+110	mV	−12 V to +14 V range
	−110	±35	+110	mV	−16 V to +10 V range
TOTAL UNADJUSTED ERROR	−0.5	±0.12	+0.5	% FSR	All output ranges

AC PERFORMANCE CHARACTERISTICS

AV_{CC} = 2.97 V to 3.6 V, V_{LOGIC} = 1.7 V to 5.5 V, AV_{DD} = 2.97 V to 15 V, AV_{SS} = −22 V to −7 V, AGND = DGND = 0 V, V_{REF} = 2.5 V, output range = −10 V to 0 V, V_{OUT}x unloaded, all specifications T_{MIN} to T_{MAX}, typical specifications at T_A = 25°C, dither powered on, analog dither signals not applied, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]					
Output Voltage Settling Time		16			¼ to ¾ scale settling to ±0.5 LSB, ±5 V range and −10 V to 0 V range
		14			256 LSB step to ±0.5 LSB
Slew Rate		1		V/µs	
Digital-to-Analog Glitch Energy		10		nV-sec	1 LSB change around major carry for 10 V span
Glitch Impulse Peak Amplitude		8		mV	
Digital Feedthrough		1		nV-sec	
Digital Crosstalk		2		nV-sec	
Analog Crosstalk		15		nV-sec	
DAC-to-DAC Crosstalk		15		nV-sec	
Total Harmonic Distortion		−80		dB	V_{REF} = 2.5 V ± 0.1 V p-p, frequency = 10 kHz, AV_{CC} = 2.97 V and 3.6 V
		−75		dB	V_{REF} = 2.5 V ± 0.1 V p-p, frequency = 10 kHz, AV_{CC} = 3.6 V
Output Noise Spectral Density[1]		375		nV/√Hz	−10 V to 0 V and ±5 V ranges, frequency = 1 kHz
		605		nV/√Hz	−16 V to 0 V and −10 V to +6 V ranges, frequency = 1 kHz
		750		nV/√Hz	−20 V to 0 V and ±10 V ranges, frequency = 1 kHz
		835		nV/√Hz	−12 V to 14 V and −16 V to +10 V ranges, frequency = 1 kHz
		280		nV/√Hz	−10 V to 0 V and ±5 V ranges, frequency = 10 kHz
		440		nV/√Hz	−16 V to 0 V and −10 V to +6 V ranges, frequency = 10 kHz
		470		nV/√Hz	−20 V to 0 V and ±10 V ranges, frequency = 10 kHz
		610		nV/√Hz	−12 V to 14 V and −16 V to +10 V ranges, frequency = 10 kHz
Output Noise[2]					Dither disabled
		20		µV rms	±5 V range
		23		µV rms	−10 V to 0 V range
		33		µV rms	−10 V to +6 V range
		38		µV rms	−16 V to 0 V range
		36		µV rms	±10 V range
		45		µV rms	−20 V to 0 V range
		45		µV rms	−16 V to 10 V range
		45		µV rms	−12 V to 14 V range

[1] DAC code = midscale. $AV_{DD} = V_{OUT\_MAX} + 2$ V. $AV_{SS} = V_{OUT\_MIN} - 2$ V.
[2] 0.1 Hz to 10 Hz. $AV_{DD} = V_{OUT\_MAX} + 2$ V. $AV_{SS} = V_{OUT\_MIN} - 2$ V.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of AV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2, Figure 3, and Figure 4. AV_{CC} = 2.97 V to 3.6 V, V_{LOGIC} = 1.7 V to 5.5 V, V_{REF} = 2.5 V, all specifications −40°C to +105°C, dither powered on, unless otherwise noted.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1[1]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	15	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	15	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge time
t_6	20	ns min	Minimum $\overline{SYNC}$ high time (write mode)
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	4	µs typ	DAC output settling time, 32 code step to ±0.5 LSB at 12-bit resolution (see Table 3)
t_{10}	100	ns typ	$\overline{RESET}$[2] pulse width low
t_{11}	100	ns typ	$\overline{RESET}$[2] pulse activation time
t_{12}	10	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_{13}	40	ns max	SCLK rising edge to SDO valid (C_{L_SDO}[3] = 15 pF)
t_{14}	80	ns min	Minimum $\overline{SYNC}$ high time (readback/daisy-chain mode)
t_{15}	5	µs typ	$\overline{SYNC}$ rising edge to $\overline{SYNC}$ rising edge (DAC register updates)

[1] Maximum SCLK frequency is 50 MHz for write mode and 10 MHz for readback mode.
[2] Minimum time between a reset and the subsequent successful write is typically 25 ns.
[3] C_{L_SDO} is the capacitive load on the SDO output.

Timing Diagrams

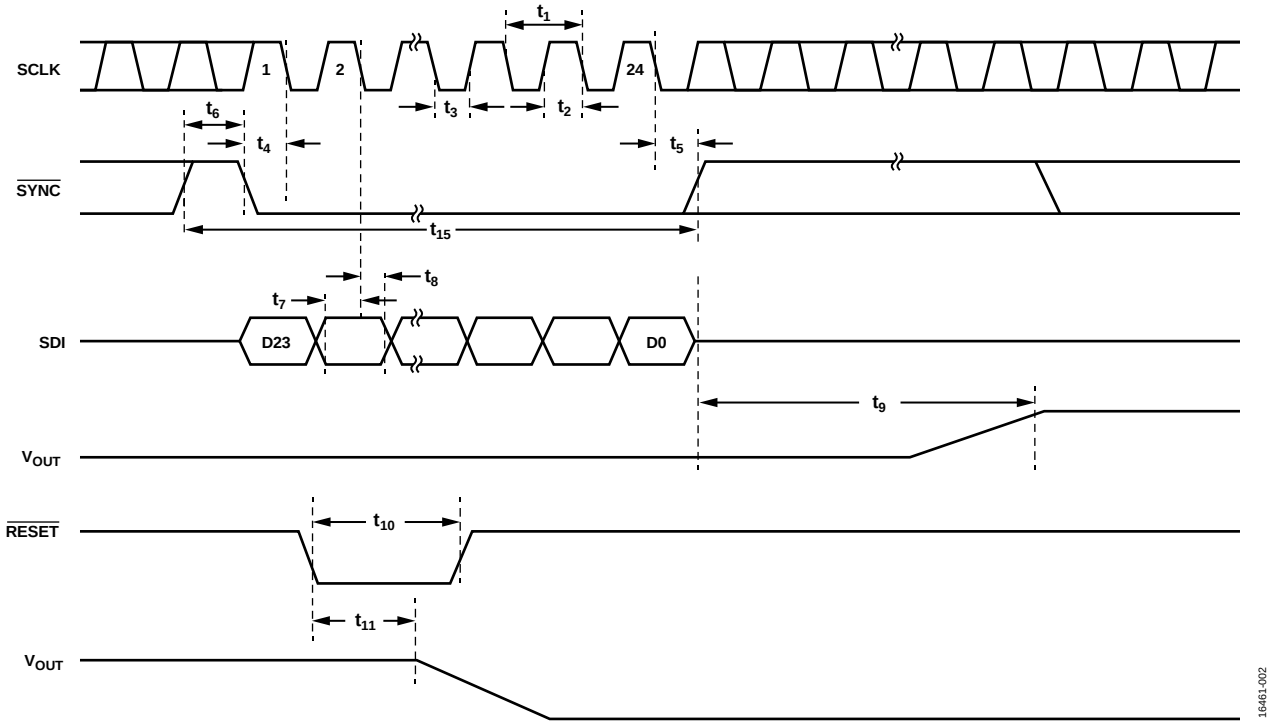

Figure 2. Serial Interface Timing Diagram

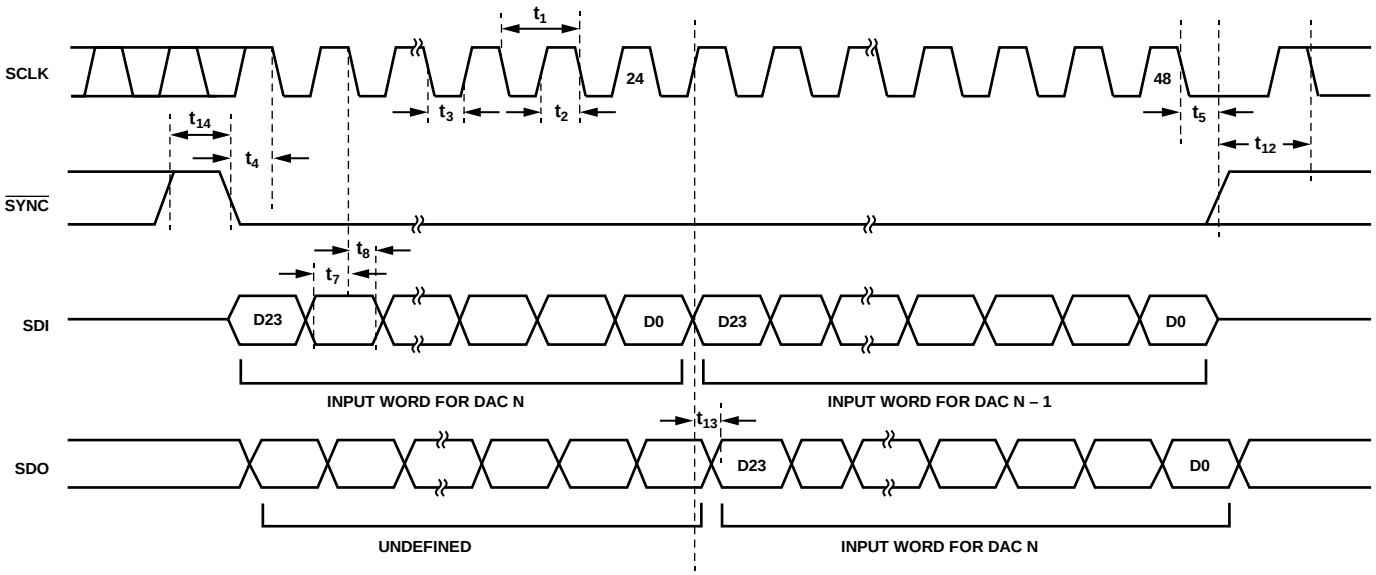

Figure 3. Daisy-Chain Timing Diagram

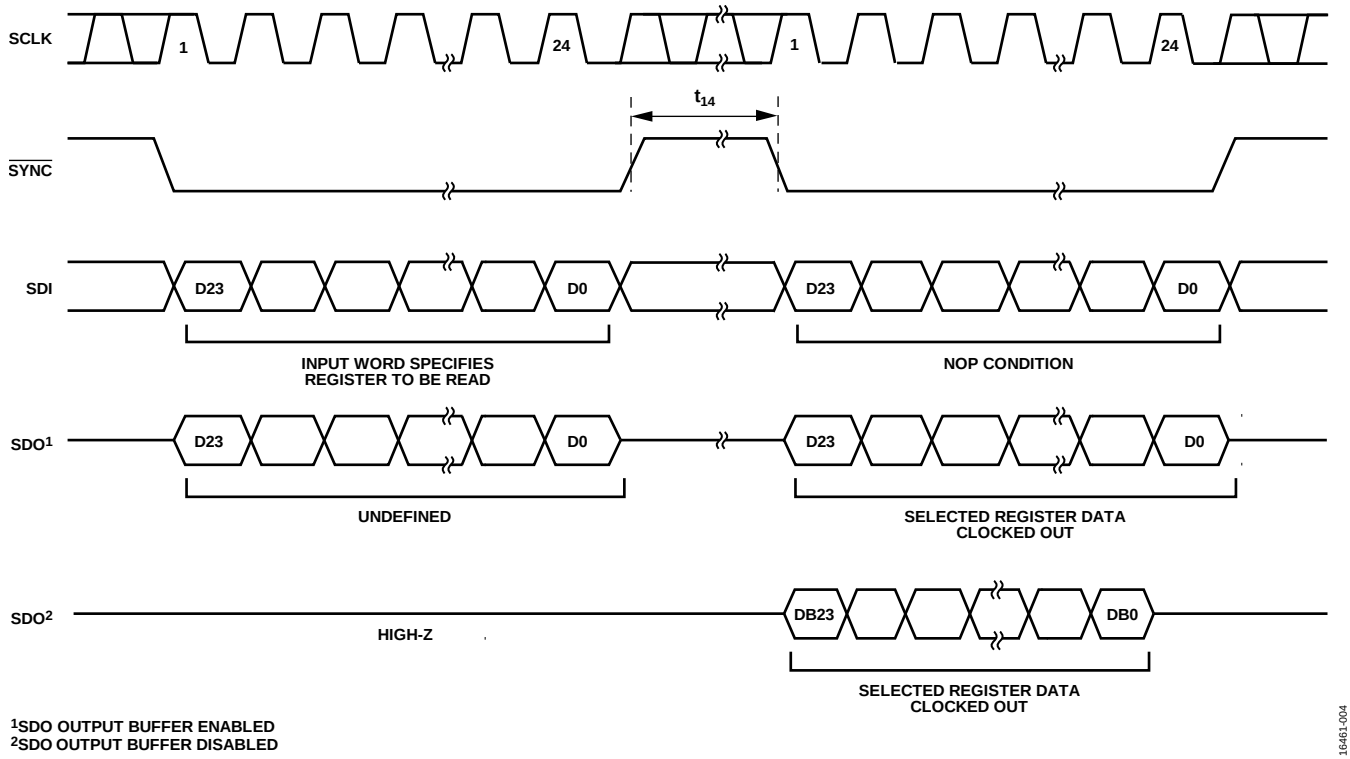

Figure 4. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 5.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +34 V
AV_{SS} to AGND	+0.3 V to −34 V
AV_{DD} to AV_{SS}	−0.3 V to +34 V
AV_{CC} to AGND	−0.3 V to +7 V
AV_{CC} to AGND	−0.3 V to AV_{DD} + 0.3 V
V_{LOGIC} to DGND	−0.3 V to +7 V
Digital Inputs[1] to DGND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output (SDO) to DGND	−0.3 V to V_{LOGIC} + 0.3 V
N0, N1 to AGND	−0.3 V to AV_{CC} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{CC} + 0.3 V
V_{OUT}x to AGND	AV_{SS} − 0.3 V to AV_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range, T_A Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature, $T_{J\,MAX}$	150°C
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
Lead Temperature	
Soldering Reflow	260°C, as per JEDEC J-STD-020

[1] The digital inputs include $\overline{\text{RESET}}$, SCLK, $\overline{\text{SYNC}}$, and SDI.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

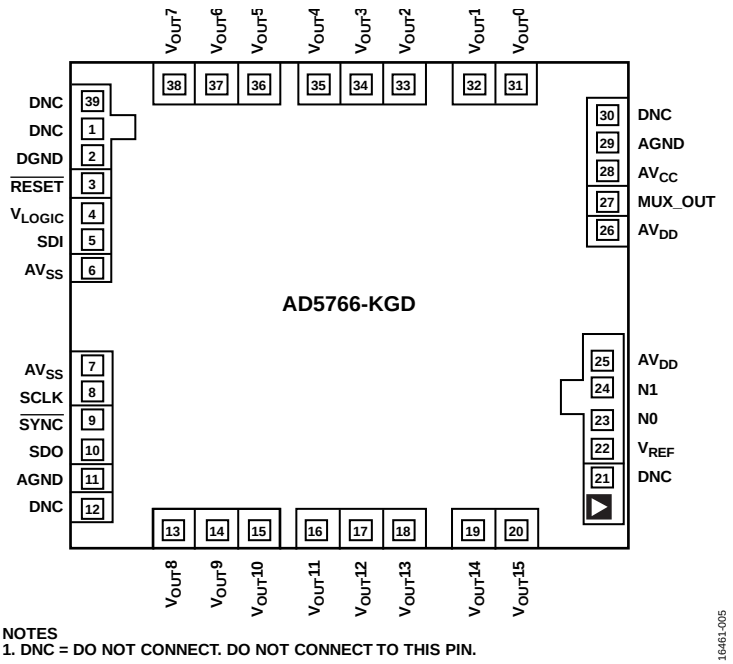

Figure 5. Pad Configuration

Table 6. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
Do Not Connect				
1	−1862.63	+1622.02	DNC	Do Not Connect. Do not connect to these pads.
12	−1857.46	−1682.62	DNC	Do Not Connect. Do not connect to these pads.
21	+1861.32	−1437.35	DNC	Do Not Connect. Do not connect to these pads.
30	+1861.32	+1646.88	DNC	Do Not Connect. Do not connect to these pads.
39	−1862.63	+1718.03	DNC	Do Not Connect. Do not connect to these pads.
Power Supplies and Reference Input				
2	−1862.63	+1520	DGND	Digital Ground.
4	−1878.06	+1165.93	V_{LOGIC}	Digital Power Supply.
6	−1857.13	−828.93	AV_{SS}	Output Amplifier Negative Analog Supply.
7	−1864.86	+897.51	AV_{SS}	Output Amplifier Negative Analog Supply.
11	−1862.63	−1415.57	AGND	Analog Ground.
22	+1862	−1296.25	V_{REF}	Reference Input Voltage. For specified performance, VREFIN = 2.5 V.
25	+1861.93	−962.93	AV_{DD}	Output Amplifier Positive Analog Supply.
26	+1862	+962.81	AV_{DD}	Output Amplifier Positive Analog Supply.
28	+1861.89	+1445.29	AV_{CC}	Power Supply Input. The AD5766-KGD operates from 2.97 V to 3.6 V. Decouple AVCC with a 10 µF capacitor in parallel with a 0.1 µF capacitor to analog ground.
29	+1862	+1550.99	AGND	Analog Ground.

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
Logic Inputs and Outputs				
3	−1880	+1319.88	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pad logic low returns the AD5766-KGD to its default power-on state. After this pad returns to logic high, the device comes out of the reset mode and is ready to accept a new SPI command. This pad can be left floating because there is a weak internal pull-up resistor.
5	−1880.01	+1039.88	SDI	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
8	−1880.01	−950.62	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz for write mode and 10 MHz for readback mode and daisy-chain mode.
9	−1880	−1125.02	$\overline{\text{SYNC}}$	Active Low Control Input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and SDI buffers and enables the input shift register. Data is transferred in on the falling edges of the next 24 clocks. If $\overline{\text{SYNC}}$ is taken high before the 24th falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the device.
10	−1852.98	−1242.64	SDO	Serial Data Output. This pad clocks data from the serial register in daisy-chain mode or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
Analog Outputs				
13	−1495.41	−1878.98	$V_{OUT}8$	Analog Output Voltage from DAC 8.
14	−1071.15	−1878.98	$V_{OUT}9$	Analog Output Voltage from DAC 9.
15	−639.89	−1878.98	$V_{OUT}10$	Analog Output Voltage from DAC 10.
16	−215.63	−1878.98	$V_{OUT}11$	Analog Output Voltage from DAC 11.
17	+215.63	−1878.98	$V_{OUT}12$	Analog Output Voltage from DAC 12.
18	+639.89	−1878.98	$V_{OUT}13$	Analog Output Voltage from DAC 13.
19	+1069.12	−1878.98	$V_{OUT}14$	Analog Output Voltage from DAC 14.
20	+1495.41	−1878.98	$V_{OUT}15$	Analog Output Voltage from DAC 15.
31	+1495.41	+1878.98	$V_{OUT}0$	Analog Output Voltage from DAC 0.
32	+1071.14	+1878.98	$V_{OUT}1$	Analog Output Voltage from DAC 1.
33	+639.88	+1878.98	$V_{OUT}2$	Analog Output Voltage from DAC 2.
34	+215.63	+1878.98	$V_{OUT}3$	Analog Output Voltage from DAC 3.
35	−215.63	+1878.98	$V_{OUT}4$	Analog Output Voltage from DAC 4.
36	−639.89	+1878.98	$V_{OUT}5$	Analog Output Voltage from DAC 5.
37	−1071.15	+1878.98	$V_{OUT}6$	Analog Output Voltage from DAC 6.
38	−1495.41	+1878.98	$V_{OUT}7$	Analog Output Voltage from DAC 7.
Dither				
23	+1862	−1191.72	N0	Dither Signal Input Pad 0. A signal connected to this pad can be added to the DAC outputs via register commands. If unused, connect this pad to ground.
24	+1862	−1087.19	N1	Dither Signal Input Pad 1. A signal connected to this pad can be added to the DAC outputs via register commands. If unused, connect this pad to ground.
Channel Monitoring				
27	+1861.98	+1190.26	MUX_OUT	Monitor Output. This pad acts as the output of a 16 to 1 channel multiplexer that can be programmed to multiplex one of 16 channels, Channel 0 to Channel 15, to the MUX_OUT pad.

OUTLINE DIMENSIONS

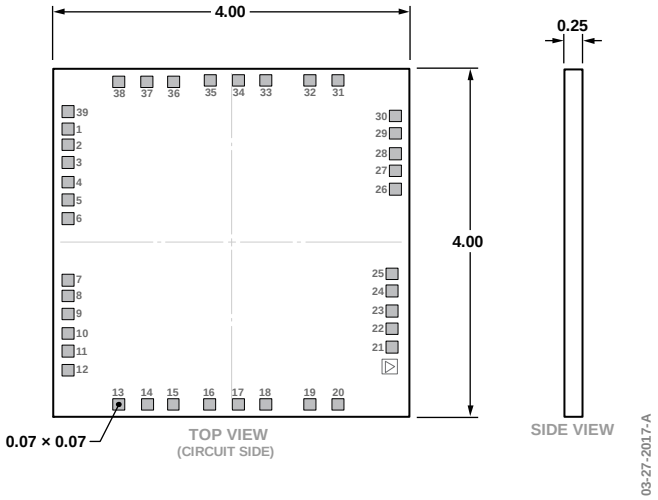

Figure 6. 39-Pad Bare Die [CHIP]
(C-39-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 7. Die Specifications

Parameter	Value	Unit
Die Size (Maximum)	4000 × 4000	µm
Bond Pad (Minimum)	70 × 70	µm
Thickness	250	µm
Scribe Line Width	80	µm
Bond Pad Composition	AlCu (0.5%)	%
Passivation Type	10 kÅ high density plasma, undoped silicate glass (HDP-USG)	Not applicable
	1.5 kÅ oxide + 6 kÅ nitride	Not applicable
Backside Bias	GND	Not applicable

Table 8. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy adhesive
Thermosonic Ball Bonding Method[1]	Ø 25 µm (1.0 mil), 2N gold wire[2]

[1] Wedge bonding not recommended.
[2] Evaluate gold wire diameter, material, and composition for suitability before use.

ORDERING GUIDE

Model	Resolution (Bits)	Temperature Range	Package Description	Package Option
AD5766-KGD-PT	16	−40°C to +105°C	39-Pad Bare Die [CHIP]	C-39-1