



Low Power Precision Analog Microcontroller, ARM Cortex-M3, with Dual Sigma-Delta ADCs

Silicon Anomaly

ADuCM360/ADuCM361

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuCM360/ADuCM361 MicroConverter® Revision D silicon. The anomalies listed apply to all ADuCM360/ADuCM361 packaged material branded as follows:

| | |
|-------------|---------------------------|
| First Line | ADuCM360 or ADuCM361 |
| Second Line | BCPZ |
| Third Line | D30 (revision identifier) |

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuCM360/ADuCM361 FUNCTIONALITY ISSUES

| Silicon Revision Identifier | Kernel Revision Identifier | Chip Marking | Silicon Status | Anomaly Sheet | No. of Reported Anomalies |
|-----------------------------|----------------------------|-------------------------|----------------|---------------|---------------------------|
| D | 0 | All silicon branded D30 | Release | Rev. A | 4 |

ADuCM360/ADuCM361 PERFORMANCE ISSUES

| Silicon Revision Identifier | Kernel Revision Identifier | Chip Marking | Silicon Status | Anomaly Sheet | No. of Reported Anomalies |
|-----------------------------|----------------------------|-------------------------|----------------|---------------|---------------------------|
| D | 0 | All silicon branded D30 | Release | Rev. A | 1 |

ADuCM360/ADuCM361 SILICON FUTURE ENHANCEMENTS

| Silicon Revision Identifier | Kernel Revision Identifier | Chip Marking | Silicon Status | Anomaly Sheet | No. of Reported Anomalies |
|-----------------------------|----------------------------|-------------------------|----------------|---------------|---------------------------|
| D | 0 | All silicon branded D30 | Release | Rev. A | 0 |

Rev. A

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PERFORMANCE ISSUES

Table 1. ADC Gain = 1, ADC Input Buffers Enabled [pr008]

| | |
|-----------------------|---|
| Background | When ADCs are configured for Gain = 1, the PGA is disabled. ADC input buffers may be enabled or disabled when ADC gain = 1. |
| Issue | The ADC data output accuracy is not linear and does not meet the ADC specifications when the ADC input buffers are enabled. |
| Workaround | The issue is not present when ADC gain ≥ 2 . When using Gain = 1, ensure the input buffers are bypassed and powered down, for example: ADCxCON[17:14] = [1111]. |
| Related Issues | None. |

FUNCTIONALITY ISSUES

Table 2. External Interrupts in Debug Mode and Cortex-M3 in Deep Sleep Mode [er007]

| | |
|-----------------------|---|
| Background | The ADuCM360/ADuCM361 has various low power modes. External interrupts can wake up the Cortex-M3 core from any of these low power modes. When in debug mode, placing the ADuCM360/ADuCM361 in Mode 4 or Mode 5 forces the Cortex-M3 core into deep sleep mode, however the high power LDO, oscillator, and clocks remain active. |
| Issue | The interrupt detection unit, external interrupt 0 to 7, will not wake the Cortex-M3 core from deep sleep (Mode 4 and Mode 5) when the debug logic is active, specifically if the debug software has set either the CDBGPWRUP or CSYSPWRUP bits in the CTRL/STAT register. These are Cortex-M3 debug logic bits not visible from user code; these bits can only be cleared by a write via the ARM serial wire download or a power on reset. |
| Workaround | None. |
| Related Issues | None. |

Table 3. Debug Mode and Deep Sleep Mode [er008]

| | |
|-----------------------|---|
| Background | The ADuCM360/ADuCM361 has various low power modes. When in debug mode, placing the ADuCM360/ADuCM361 in Mode 4 or Mode 5 forces the Cortex-M3 core into deep sleep mode; the rest of the device remains active. |
| Issue | After serial wire debug access, the serial wire logic may prevent a complete power down of the device. The debug logic is cleared by a power cycle. |
| Workaround | Power cycle the device after serial wire debug access. |
| Related Issues | None. |

Table 4. I²C Slave not Releasing the Bus [er009]

| | |
|-----------------------|---|
| Background | When an I ² C read request happens, if the TX FIFO of the slave is empty, the slave must NACK the request from the master. Then it must release the bus, allowing the master to generate a STOP condition. |
| Issue | If the TX FIFO of the slave is loaded with a byte with an MSB of 0, just on the rising edge of SCL for the ACK/NACK, the slave will pull the SDA low and hold the line until the device is reset. |
| Workaround | Make sure the TX FIFO is always loaded on time by preloading TX FIFO in the preceding RX interrupt. |
| Related Issues | None. |

Table 5. I²C Clock Stretch Issue [er010]

| | |
|-----------------------|--|
| Background | Clock stretching is a feature that allows a device to halt the I ² C bus temporarily by holding SCL low. Register I2CxSCON Bit 6 enables clock stretching in slave mode. Register I2CxMCON Bit 3 enables clock stretching in master mode. |
| Issue | Writing to I2CxSCON Bit 6 or to I2CxMCON Bit 3 on the rising edge of SCL can cause a glitch that can be interpreted by other devices as a real clock edge and might hang the bus. |
| Workaround | Do not enable clock stretching. |
| Related Issues | None. |

SECTION 1. ADuCM360/ADuCM361 PERFORMANCE ISSUES

| Reference Number | Description | Status |
|------------------|---|--------|
| pr001 | ADC0/ADC1 INL specification | Fixed |
| pr002 | ADC0/ADC1 noise specification | Fixed |
| pr003 | ADC0/ADC1 noise specification at sampling rates ≥ 500 Hz | Fixed |
| pr004 | Current specification | Fixed |
| pr005 | ADC1–internal channels issue | Fixed |
| pr006 | Current–power down specification | Fixed |
| pr007 | DAC–offset error (DAC output buffer enabled) | Fixed |
| pr008 | ADC gain = 1, ADC input buffers enabled | Open |

SECTION 2. ADuCM360/ADuCM361 FUNCTIONALITY ISSUES

| Reference Number | Description | Status |
|------------------|--|--------|
| er001 | ADC0/ADC1 input voltage–limitation on maximum input voltage | Fixed |
| er002 | ADC0/ADC1–step detection circuit | Fixed |
| er003 | External reference buffer–power down | Fixed |
| er004 | ADC0/ADC1– Both ADCs sampling the same input | Fixed |
| er005 | ADC0/ADC1– ADC output code issue | Fixed |
| er006 | Power supply monitor (PSM) | Fixed |
| er007 | External interrupts in debug mode and Cortex-M3 in deep sleep mode | Open |
| er008 | Debug mode and deep sleep mode | Open |
| er009 | I ² C slave not releasing the bus | Open |
| er010 | I ² C clock stretch issue | Open |

SECTION 3. ADuCM360/ADuCM361 SILICON FUTURE ENHANCEMENTS

| Reference Number | Description | Status |
|------------------|--|--------|
| fr001 | Ground switch–maximum current | Fixed |
| fr002 | ADC0/ADC1 PGA–output voltage from PGA limited to 1 V maximum | Fixed |
| fr003 | Change of pins used for UART downloader | Fixed |

NOTES