MicroConverter® Technical Note - uC009
Addressing 16MB of External Data Memory

1.0 INTRODUCTION :

Although a standard 8051 can only address up to 64kBytes of external data memory, a feature unique to MicroConverters with an external data memory interface allows addressing of up to 16MB of external data memory.

As is shown in section 2.0, the MicroConverter is still fully compatible with the standard 8051 for addressing up to 64kBytes of external data memory.

To implement the 24bit external data memory addressing, all that is required by the user is to add an addition latch to multiplex the data on Port 2 as described in section 2.1.

Although both the external program memory and the external data memory are accessed by some of the same pins, both the external data memory and external program memory can be used together. For simplicity, and especially considering that the MicroConverter family now supports parts with 62kBytes of internal code space, this tech note will assume that the user is running from internal code space.

2.0 ADDRESSING UP TO 64 KBYTES OF EXTERNAL DATA MEMORY

To address up to 64kBytes of external data memory then the hardware should be configured as shown in figure 1. This interface is standard to any 8051 compatible MCU.

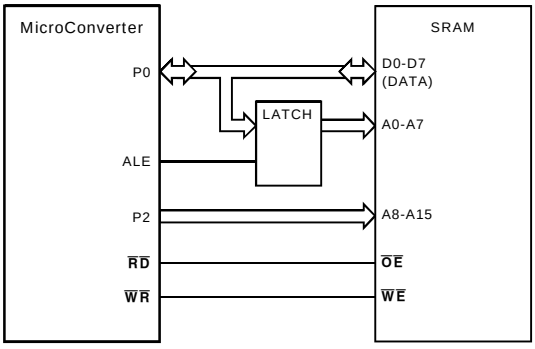

Fig 1: External Data Memory Interface (64kByte Address Space)

In this configuration Port 0 outputs the low address (A0→A7) while Port 2 outputs the high address (A8→A15). The falling edge of ALE is used to latch the low address for the external memory. The read ($\overline{RD}$) and ($\overline{WR}$) write strobes are used to activate the external memory. The timing diagrams in figure 3 and figure 4 are also relevant to this configuration except that the page address (DPP) on port 2 does not have to be latched by an external latch.

2.1 ADDRESSING UP TO 16 MBYTES OF EXTERNAL DATA MEMORY

To address up to 16MBytes of external data memory then the hardware should be configured as shown in figure 2.

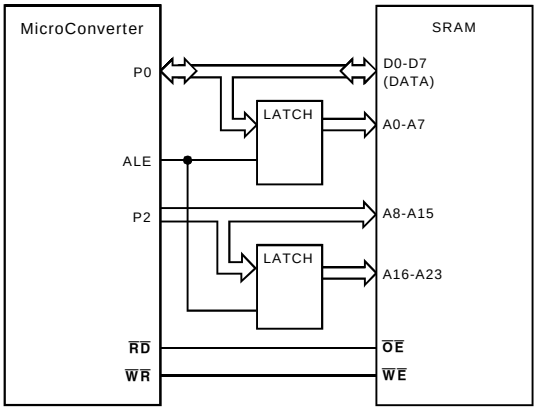

Fig 2: External Data Memory Interface (16MByte Address Space)

In this configuration Port 0 outputs the low address (A0→A7) while Port 2 outputs the high address (A8→A15) and the page address (A16→A23). As shown in figure 3 and figure 4 the falling edge of ALE is used to latch the low address and the page address for the external memory requiring an extra latch for the multiplexing of Port 2. The read ($\overline{RD}$) and ($\overline{WR}$) write strobes are used as normal to activate the external memory.

As shown in figure 3 if the MicroConverter is writing data to the external memory, the data (D0→D7) will be automatically outputted at Port 0 after the falling edge of ALE has been used to latch the address. The falling edge of the $\overline{WR}$ strobe is used to enable the write to the XRAM. Refer to the timing specifications in the relevant datasheet for more details on external data memory interface timings.

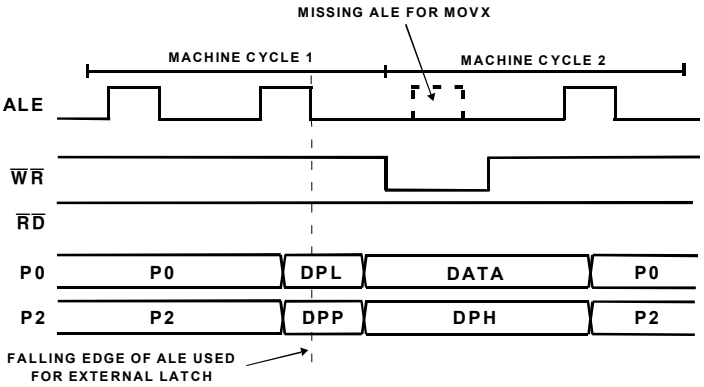

Fig 3: XRAM Write Operation (e.g. MOVX @DPTR, A)

If the MicroConverter is performing a read operation, port 0 will be left to float after the falling edge of ALE. The falling edge of the $\overline{RD}$ strobe will enable the read operation of the XRAM which must output the data (D0→D7) at Port 0 and give it time to settle before the read strobe returns high. Again refer to the timing specifications in the relevant datasheet for more details on external data memory interface timings.

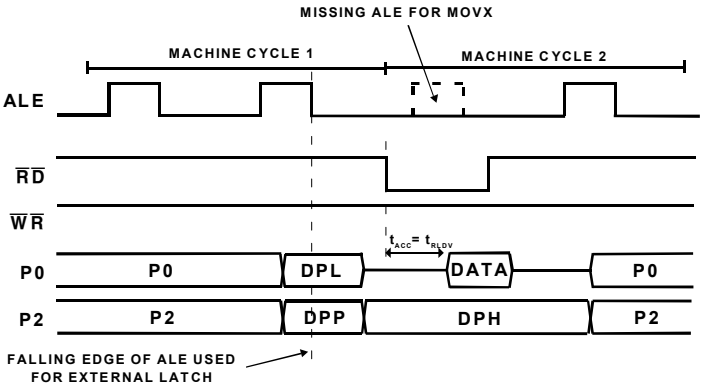

Fig 4: XRAM Read Operation (e.g. MOVX A, @DPTR)

Notes:

1. The toggling of the ALE can be diabled by setting PCON.4. This is often used to save power and to reduce EMI. By default ALE is enabled.
   In both of the implementations above make sure that ALE has not been disabled by a previous write to the PCON SFR. If ALE has been disabled then the low address or the page address will not be latched for the external data memory.

2. Because the high address (A8→A15) is present at the time of the $\overline{RD}$ or $\overline{WR}$ strobe then this MicroConverter interface is 100% backward compatible with any standard 8051 interface as shown in section 2.0.

3. On the big memory parts as well as 62kBytes of flash/EE program memory an extra 2kBytes of internal XRAM is available to the user. While accesses to this memory are made, none of the P0, P2, $\overline{RD}$ or $\overline{WR}$ pins will change during the access to internal XRAM.