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Estimating Power for ADSP-SC57x/ADSP-2157x SHARC+® Processors

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Introduction

This EE-note describes how to estimate power consumption on ADSP-SC57x/ADSP-2157x SHARC+® processors (hereafter referred to collectively as "ADSP-SC57x processors"), which are multi-core high-performance processors with a multitude of peripherals, accelerators, and high-speed Direct Memory Access (DMA) channels. These processors have multiple power and clock domains, and the intent of this application note is to provide a simplified methodology for estimating the total System-on-Chip (SoC) power consumption, depending on the level of processor activity.

Power estimates are based on design simulations and characterization data measured across power supply voltage, core and system clock frequency, and junction temperature (T_J) and can vary widely depending on how the on-chip ADSP-SC57x processor resources are used. Thus, power consumption cannot be estimated accurately without an understanding of the components in use and the usage patterns for those components. By providing the usage parameters that describe how and what is being used, accurate consumption estimates can be obtained for use by board designers to consider when developing their ADSP-SC57x processor-based power supply and thermal relief designs.

Please consult the following sections of the *ADSP-SC570/571/572/573/ADSP-21571/21573 SHARC+ Dual Core DSP with ARM Cortex®-A5 Embedded Processor Datasheet*[1] for details specific to discussions throughout this EE-Note:

- See the *Recommended Operating Conditions* section for details regarding supported power supply ranges.
- See the *Electrical Characteristics* and subsequent *Total Internal Power Dissipation* sections for details regarding current specifications.

In the *associated ZIP file*[2] furnished with this EE-note is a convenient *Power Calculator Tool* that allows users to obtain a total power profile by populating the cells in a spreadsheet with data found both in the processor datasheet and as a result of calculations specific to the intended application. For cases where information in the power calculator is not also in the datasheet, it is explained in this document. This EE-note also describes how to provide the appropriate input to the power calculator such that the full power profile for the application can be obtained and details regarding how the calculations are made and how the results contribute to the overall power profile.

Power Domains

There are multiple power domains associated with the ADSP-SC57x processor, and total power consumption is the sum of the power consumed across all of them. There are four (4) major power domains that are significant contributors to the overall power profile:

- V_{DD_INT}: most internal on-chip logic (e.g., cores, accelerators, DMA engines, etc.)
- V_{DD_EXT}: I/O pad ring, JTAG, etc.
- V_{DD_DMC}: DDR controller, DDR PHY logic
- V_{DD_USB}: USB PHY logic

The V_{DD_HADC} (for the Housekeeping ADC) power domain is a marginal contributor to total power and can be ignored when calculating the full power profile for an application.

Estimating Internal Power Consumption ($P_{DD\_INT\_TOT}$)

The total power consumption associated with the on-chip logic (on the V_{DD_INT} supply) is the sum of the static (leakage) and dynamic (switching) power components. The dynamic component depends on processor activity, which includes the instruction execution sequence, the data operands involved, and the instruction rate on each core, as well as the number of active peripherals/accelerators, their clock rates, and any associated DMA data traffic. The static component is independent of processor activity and is a function of temperature and voltage.

The internal current ($I_{DD\_INT\_TOT}$) consumed by ADSP-SC57x processors is comprised of:

- $I_{DD\_INT\_STATIC}$: leakage current
- $I_{DD\_INT\_CCLK\_A5\_DYN}$: dynamic current in CCLK domain for ARM Cortex-A5 (core0)
- $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$: dynamic current in CCLK domain for SHARC+ (core1)
- $I_{DD\_INT\_CCLK\_SHARC2\_DYN}$: dynamic current in CCLK domain for SHARC+ (core2)
- $I_{DD\_INT\_DCLK\_DYN}$: dynamic current in DCLK domain (no other activity)
- $I_{DD\_INT\_SYSCLK\_DYN}$: dynamic current in SYSCLK domain (no other activity)
- $I_{DD\_INT\_SCLK0\_DYN}$: dynamic current in SCLK0 domain (no other activity)
- $I_{DD\_INT\_SCLK1\_DYN}$: dynamic current in SCLK1 domain (no other activity)
- $I_{DD\_INT\_OCLK\_DYN}$: dynamic current in OCLK domain (no other activity)
- $I_{DD\_INT\_USB\_DYN}$: dynamic current in USB domain (no other activity)
- $I_{DD\_INT\_GIGE\_DYN}$: dynamic current consumed by GigE block
- $I_{DD\_INT\_MLB\_DYN}$: dynamic current consumed by MLB block (only applies to automotive models)
- $I_{DD\_INT\_DMA\_DR\_DYN}$: dynamic current consumed due to DMA activity

Therefore, the total current can be expressed as the sum of each of the above components, where there is a single static power component and several dynamic power components that must be included in the overall power profile.

Typical and maximum specifications for I_{DD_INT} are provided in the processor datasheet at specific voltages, frequencies, and temperatures, and the following sections describe how to use this data to calculate the application's overall power and thermal needs.

Estimating Total I_{DD_INT} Dynamic Current

Due to the multi-featured clock and power designs of the ADSP-SC57x processors, there are many contributors to the overall dynamic component associated with the power consumed by the core. While there is opportunity to disable clocks to the various domains, each must be scrutinized to determine what needs to be accounted for with respect to power dissipation when any combination of these domains is active in the system.

Core Dynamic Current ($I_{DD\_INT\_CCLK\_A5\_DYN}$, $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$, and $I_{DD\_INT\_CCLK\_SHARC2\_DYN}$)

The ADSP-SC57x processor datasheet provides baseline dynamic current consumption specifications, which are obtained with the processor running what is defined to be a "typical" application and is represented in the datasheet by the I_{DD_TYP} specification. However, these conditions do not represent all possible application code and ignore the concept of silicon process variation, which also influences the power profile because the transistor physics are not uniform across it. When making decisions regarding the power supply design, the worst-case scenario must always be considered, and the above assumptions are addressed in two places in the datasheet in order to facilitate extrapolation to obtain the maximum requirements for the power supply design:

- *Dynamic Current* tables – provide the maximum (across process) core dynamic current spec for each core as a function of voltage (V_{DD_INT}) and frequency (f_{CCLK}) while running "typical" application code
- *Activity Scaling Factor (ASF)* tables – describe discrete dynamic activity levels for each processor core to provide insight as to how the dynamic current scales with changing loads on the core

The data in the *Dynamic Current* tables for the two types of cores on the ADSP-SC57x processor were obtained based on the following equations, which include a scaling factor unique to each type of core representing the currents consumed per MHz per Volt in each core clock domain; therefore, V_{DD_INT} is in terms of Volts, and f_{XXX} is in terms of MHz in the following core clock dynamic current equations:

- $I_{DD\_INT\_CCLK\_SHARC1\_DYN} = 0.63 \times V_{DD\_INT} \times f_{CCLK\_SHARC1}$
- $I_{DD\_INT\_CCLK\_SHARC2\_DYN} = 0.63 \times V_{DD\_INT} \times f_{CCLK\_SHARC2}$
- $I_{DD\_INT\_CCLK\_A5\_DYN} = 0.16 \times V_{DD\_INT} \times f_{CCLK\_A5}$

Using these combined specifications, the dynamic component of core power consumption can be estimated for each core by multiplying the baseline spec obtained from the *Dynamic Current* tables by the associated ASF, as further explored in the following sections.

ARM Cortex-A5 Activity Scaling Factor (ASF) Vectors

The *Activity Scaling Factors for ARM Cortex-A5 Core* table in the datasheet defines the following vectors:

- **$I_{DD\text{-}PEAK}$**: ARM core continuously thrashing cache memory with maximum data changes ("peak activity")
- **$I_{DD\text{-}IDLE}$**: ARM core executing only the IDLE instruction ("idle activity")
- **$I_{DD\text{-}DHRYSTONE}$**: ARM core executing Dhrystone benchmark algorithm

The test code used to measure $I_{DD\text{-}PEAK}$ represents worst-case core operation and is not sustainable under normal application conditions.

In addition to the ASFs above, the power calculator defines the following vectors on the *Core Activity Factors* tab:

- $I_{DD\text{-}7525}$: ARM core executing 75% peak activity and 25% idle activity (used for I_{DD_TYP} spec)
- $I_{DD\text{-}5050}$: ARM core executing 50% peak activity and 50% idle activity
- $I_{DD\text{-}2575}$: ARM core executing 25% peak activity and 75% idle activity
- $I_{DD\text{-}CLOCK\_GATED}$: ARM core clock disabled (no dynamic power)

SHARC+® Core Activity Scaling Factor (ASF) Vectors

The *Activity Scaling Factors for SHARC+ Core1 and Core2* table in the datasheet defines the following vectors:

- **$I_{DD\text{-}IDLE}$:** SHARC+ core executing only the IDLE instruction
- **$I_{DD\text{-}NOP}$:** SHARC+ core executing 100% NOPs
- **$I_{DD\text{-}TYP\_3070}$:** SHARC+ core executing 30% floating-point (FP) multiply/add/subtract and store instructions and 70% NOPs
- **$I_{DD\text{-}TYP\_5050}$:** SHARC+ core executing 50% FP multiply/add/subtract and store instructions and 50% NOPs
- **$I_{DD\text{-}TYP\_7030}$:** SHARC+ core executing 70% FP multiply/add/subtract and store instructions and 30% NOPs (used for I_{DD_TYP} spec)
- **$I_{DD\text{-}PEAK\_100}$:** SHARC+ core executing 100% FP multiply/add/subtract and store instructions

The test code used to measure $I_{DD\text{-}PEAK\_100}$ represents worst-case core operation and is not sustainable under normal application conditions.

In addition to the ASFs above, the power calculator defines the following vector on the *Core Activity Factors* tab:

- $I_{DD\text{-}CLOCK\_GATED}$: SHARC+ core clock disabled (no dynamic power)

Using ASFs to Establish Application-Specific Total Average Power Profile

Once the baseline dynamic current specification from the *Dynamic Current* tables is obtained from the cell associated with the CCLK frequency (f_{CCLK}) and input voltage (V_{DD_INT}) of interest, the next step is to analyze the application to identify and apply the proper ASFs. To do so, the application needs to be broken down into percentages of time spent in states associated with one of these standard power vectors. With knowledge of the program flow and an estimate as to the percentage of time spent at each activity level, the baseline dynamic current and the corresponding ASF can be used to determine the average dynamic current consumption for each core.

For example, $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ for the SHARC+ core1 in a specific application can be calculated according to Equation 1, where "%" is the percentage of the overall time that the application spends in that state:

$$
\begin{aligned}
I_{DD\_INT\_CCLK\_SHARC1\_DYN} = {} & (\%\ \text{Peak activity level} \times I_{DD\text{-}PEAK}\ \text{ASF} \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + \\
& (\%\ \text{High activity level} \times I_{DD\text{-}TYP\_7030}\ \text{ASF} \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + \\
& (\%\ \text{Moderate activity level} \times I_{DD\text{-}TYP\_5050}\ \text{ASF} \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + \\
& (\%\ \text{Low activity level} \times I_{DD\text{-}TYP\_3070}\ \text{ASF} \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + \\
& (\%\ \text{NOP activity level} \times I_{DD\text{-}NOP}\ \text{ASF} \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + \\
& (\%\ \text{IDLE activity level} \times I_{DD\text{-}IDLE}\ \text{ASF} \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + \\
& (\%\ \text{CCLK disabled} \times I_{DD\text{-}CLOCK\_GATED}\ \text{ASF} \times I_{DD\_INT\_CCLK\_SHARC1\_DYN})
\end{aligned}
$$

Equation 1. Total Individual Core Dynamic Current

Note that the $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ output is the average current, whereas the $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ inputs are with ASF = 1.0. Consider a SHARC+ core1 application that is continuously running and never idles, where core activity is:

- $I_{DD\text{-}PEAK}$ activity level – 10%
- $I_{DD\text{-}TYP\_7030}$ activity level – 20%
- $I_{DD\text{-}TYP\_5050}$ activity level – 50%
- $I_{DD\text{-}TYP\_3070}$ activity level – 10%
- $I_{DD\text{-}NOP}$ activity level – 10%
- $I_{DD\text{-}IDLE}$ and $I_{DD\text{-}CLOCK\_GATED}$ activity level – 0%

Applying Equation 1 to this profile yields:

$$I_{DD\_INT\_CCLK\_SHARC1\_DYN} = (0.1 \times I_{DD\text{-}PEAK}\ ASF \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + (0.2 \times I_{DD\text{-}TYP\_7030}\ ASF \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + (0.5 \times I_{DD\text{-}TYP\_5050}\ ASF \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + (0.1 \times I_{DD\text{-}TYP\_3070}\ ASF \times I_{DD\_INT\_CCLK\_SHARC1\_DYN}) + (0.1 \times I_{DD\text{-}NOP}\ ASF \times I_{DD\_INT\_CCLK\_SHARC1\_DYN})$$

The above process must then be repeated for the SHARC+ core2 and ARM Cortex-A5 cores to obtain the appropriate values for $I_{DD\_INT\_CCLK\_SHARC2\_DYN}$ and $I_{DD\_INT\_CCLK\_A5\_DYN}$, respectively, to be used in the $I_{DD\_INT\_TOT}$ calculation.

Estimating System Clock Tree Currents

ADSP-SC57x processors have multiple system clock domains to clock the system buses, various peripherals, DMA controllers, L2 memory, and DDR controllers. Each of these clock domains consume power that dissipates in the internal power domain due to its respective clock toggling inside the chip. Additional power consumed by the peripherals and DMA when turned on is attributed to individual peripherals/DMAs running in the system, which is estimated separately and added to this baseline system power when the total power profile is calculated.

There are four major system clock domains on ADSP-SC57x processors: SYSCLK, SCLK0, SCLK1, and DCLK.

SYSCLK, SCLK0 and SCLK1 are generated by the Clock Generation Unit 0 (CGU0). DCLK is selected via the Clock Distribution Unit (CDU). Please see the *ADSP-SC57x SHARC+ Processor Hardware Reference Manual*[3] for details.

There is also a programmable output clock (OCLK), which can be generated by one of the CGUs and routed to an external pin on the processor via the CDU, that has a small influence on the overall power profile as well.

To estimate the impact to the current consumed in the V_{DD_INT} domain as a result of each of these system clocks, unique scaling factors are furnished in the processor datasheet, representing the currents consumed per MHz per Volt in each system clock domain; therefore, V_{DD_INT} is in terms of Volts, and f_{XXX} is in terms of MHz in the system clock dynamic current equations:

- $I_{DD\_INT\_DCLK\_DYN} = 0.08 \times V_{DD\_INT} \times f_{DCLK}$
- $I_{DD\_INT\_SYSCLK\_DYN} = 0.520 \times V_{DD\_INT} \times f_{SYSCLK}$
- $I_{DD\_INT\_SCLK0\_DYN} = 0.280 \times V_{DD\_INT} \times f_{SCLK0}$
- $I_{DD\_INT\_SCLK1\_DYN} = 0.013 \times V_{DD\_INT} \times f_{SCLK1}$
- $I_{DD\_INT\_OCLK\_DYN} = 0.015 \times V_{DD\_INT} \times f_{OCLK}$

The scaling factor for each of the above system clock dynamic current equations is in units of mA/MHz/V; therefore, the result for each is in terms of mA.

Estimating USB Contribution to Internal Dynamic Current ($I_{DD\_INT\_USB\_DYN}$)

If the USB controller is used, it contributes to the V_{DD_INT} domain's dynamic current consumption ($I_{DD\_INT\_USB\_DYN}$). While the datasheet provides a single addend to be included in the total dynamic power dissipation calculation, the value carries with it the worst-case assumption that the USB is operating in high-speed mode (HS-MODE). Table 1, from the *USB* tab in the power calculator, defines the current consumed by the USB module. Beyond what is found in the processor datasheet, this table also defines $I_{DD\_INT\_USB\_DYN}$ values for both the full-speed (FS-MODE) and suspend (SUSPEND-ON) modes of operation. These values were obtained through design simulations and are included in the power calculator to properly model the system when considering the impact to the overall system power from the USB blocks.

USB Mode	$I_{DD\_INT\_USB\_DYN}$ (mA)
NOT USED	0
SUSPEND-ON	0.31
FS-MODE	6.78
HS-MODE	9.6

Table 1. Dynamic USB Current Dissipated in the V_{DD_INT} Domain ($I_{DDINT\_USB\_DYN}$)

Estimating Gigabit Ethernet Contribution to Internal Dynamic Current ($I_{DD\_INT\_GIGE\_DYN}$)

Table 2 can be found on the *GigE* tab of the power calculator and shows the current consumed in the V_{DD_INT} domain by the Gigabit Ethernet block if it is enabled. It simply reflects the addend identified in the datasheet as the $I_{DD\_INT\_GIGE\_DYN}$ component to include in the calculation for the total internal power ($I_{DD\_INT\_TOT}$) estimation when Gigabit Ethernet is used.

GigE used?	$I_{DD\_INT\_GIGE\_DYN}$ (mA)
NOT USED	0
USED	10

Table 2. Dynamic Gigabit Ethernet Current Dissipated in the V_{DD_INT} Domain ($I_{DD\_INT\_GIGE\_DYN}$)

Estimating MLB Contribution to Internal Dynamic Current ($I_{DD\_INT\_MLB\_DYN}$)

On automotive models, the Media Local Bus (MLB) is available to enable communication with a MOST network. Table 3 can be found on the *MLB* tab of the power calculator and shows the current consumed in the V_{DD_INT} domain by the MLB if it is enabled. It simply reflects the addend identified in the datasheet as the $I_{DD\_INT\_MLB\_DYN}$ component to include in the calculation for the total internal power ($I_{DD\_INT\_TOT}$) estimation when MLB is used.

MLB used?	$I_{DD\_INT\_MLB\_DYN}$ (mA)
NOT USED	0
USED	10

Table 3. Dynamic Media Local Bus Current Dissipated in the V_{DD_INT} Domain ($I_{DD\_INT\_MLB\_DYN}$)

Estimating DMA Contribution to Internal Dynamic Current ($I_{DD\_INT\_DMA\_DR\_DYN}$)

Different types of DMA transactions in the system will result in additional power consumption:

- DMA transfers between the various memory spaces
- DMA transfers from memory to peripherals
- DMA transfers from peripherals to memory

Power consumption varies with the number of running DMA channels and the rate at which they move data through the system. To estimate DMA power consumption, three power profiles are available in the power calculator in the *DMA/Peripheral Usage* pull-down in the V_{DD_INT} *Clock Domains & DMA Rates* table on the *Power Estimation* tab:

1) **HIGH**: comprised of high-speed MDMA, multiple low-speed MDMAs, and several high-speed peripheral DMAs (e.g., MSI, Link Port, PPI, etc.) running simultaneously in the system for a combined throughput of ~3300 MBPS.
2) **MEDIUM**: comprised of medium-speed MDMA, multiple low-speed MDMAs, and several low-speed peripheral DMAs (e.g., SPI, SPORT, etc.) running simultaneously in the system for a combined throughput of ~1500 MBPS.
3) **LOW**: comprised of low-speed MDMA and several low-speed peripheral DMAs (e.g., SPI, SPORT, etc.) running simultaneously in the system for a combined throughput of ~600 MBPS.

To estimate the DMA dynamic current ($I_{DD\_INT\_DMA\_DR\_DYN}$) in the application, the combined data bandwidth of all the DMAs running in the system will determine which of these profiles should be selected as a closest match to the actual application and used as the $I_{DD\_INT\_DMA\_DR\_DYN}$ component for the $I_{DD\_INT\_TOT}$ calculation.

High DMA Configuration

The following peripheral and memory DMAs are active in this configuration:

- 8 SPORTS @56.5MHz in RX mode with PRI/SEC enabled (Writing Data to L2)
- 8 SPORTS @56.5MHz in TX mode with PRI/SEC enabled (Reading Data from L2)
- SPI2 in Quad mode, SPI0/SPI1 in Dual mode TX operation @56.5MHz (Reading Data from L2)
- PPI 16-bit in RX mode @56.5MHz (Writing Data to L2)
- LP TX mode @112.5MHz (Reading Data from L2)
- 1x Low Speed MDMA transferring data from SHARC0 L1 to DMC0 (1175MBPS)
- 1x Medium Speed MDMA transferring data from SHARC0 L1 to DMC0 (1081MBPS)
- 1x High speed DMA transferring data from SHARC1 L1 to DMC0 (585 MBPS)

In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the *DMA_Usage* tab of the power calculator) is 74 mA.

Medium DMA Configuration

The following peripheral and memory DMAs are active in this configuration:

- 8 SPORTS @56.5MHz in RX mode with PRI/SEC enabled (Writing Data to L2)
- 8 SPORTS @56.5MHz in TX mode with PRI/SEC enabled (Reading Data from L2)
- SPI2 in Quad mode, SPI0/SPI1 in Dual mode TX operation @56.5MHz (Reading Data from L2)
- PPI 16-bit in RX mode @56.5MHz (Writing Data to L2)
- LP TX mode @112.5MHz (Reading Data from L2)
- 1x Low Speed MDMA transferring data from SHARC0 L1 to DMC0 (410 MBPS)
- 1x Medium Speed MDMA transferring data from SHARC1 L1 to DMC0 (745MBPS)

In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the *DMA_Usage* tab of the power calculator) is 47 mA.

Low DMA Configuration

The following peripheral and memory DMAs are active in this configuration:

- 8 SPORTS @56.5MHz in RX mode with PRI/SEC enabled (Writing Data to L2)
- 8 SPORTS @56.5MHz in TX mode with PRI/SEC enabled (Reading Data from L2)
- SPI2 in Quad mode, SPI0/SPI1 in Dual mode TX operation @56.5MHz (Reading Data from L2)
- 1x Low Speed MDMA transferring data from SHARC0 L1 to DMC0 (424 MBPS)
-

In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the *DMA_Usage* tab of the power calculator) is 23 mA.

The $I_{DD\_INT\_DMA\_DR\_DYN}$ component value specified for each of the configurations above is the delta between I_{DD_INT} current measurements obtained empirically on the ADSP-SC573 EZ-KIT Lite® evaluation platform before and after enabling the indicated DMA activity.

Estimating Total Static Current ($I_{DD\_INT\_STATIC}$)

The static current ($I_{DD\_INT\_STATIC}$) dissipated across the entire device in the V_{DD_INT} power domain is due to transistor leakage and is present when power is applied to the power domains, even when all the internal clocks are shut off (by gating/cutting the CLKIN to the ADSP-SC57x processor) and the device is held in reset. As such, static current is solely a function of junction temperature (T_J) and voltage (V_{DD_INT}) and, unlike dynamic current, need not be adjusted for discrete core activity levels. $I_{DD\_INT\_STATIC}$ can be obtained by looking up the value corresponding to the application conditions (i.e., at a specific V_{DD_INT} and T_J) in the *Static Current* table in the processor datasheet.

The $I_{DD\_INT\_STATIC}$ specifications in the *Static Current* table in the datasheet are maximum specifications that account for the wafer fabrication process.

Since the static power component is constant for a given voltage and temperature, it is simply added to the total estimated dynamic current when calculating the total power consumption due to the core logic of the processor. When developing power supply and thermal relief designs, care should be taken to ensure that the highest expected junction temperature and voltage is used when extracting data from the *Static Current* table.

Estimating External Power Consumption (P_{DD_EXT} and P_{DD_DMC})

Total external power consumption ($P_{DD\_EXT\_TOT}$, dissipated in the V_{DD_EXT} and V_{DD_DMC} power domains) is dependent on several parameters:

- O – number of output pins associated with the interface
- TR – toggle ratio (percentage of pins that switch any given cycle)
- f – maximum frequency at which the output pins can switch
- V_{DD_EXT} or V_{DD_DMC} – voltage swing of the output pins
- C_L – load capacitance of the output pins
- U – utilization factor (percentage of time that the peripheral is on and running)

In addition to the input capacitance of each device connected to an output, the total capacitance (C_L) should include the capacitance of the processor pin itself (C_{OUT}), which is driving the load.

The worst-case external pin power scenario occurs when the load capacitor charges and discharges continuously, requiring the pin to toggle each cycle In terms of external supply power, over the maximum V_{DD_EXT} voltage swing (as specified in the datasheet). Since the state of the pin can change only once per cycle, the maximum toggling frequency is f/2. When considering the full current profile for the V_{DD_EXT} power domain, there are a number of peripherals that can contribute to it, and each must be considered separately and then summed together to form the single I_{DD_EXT} component of the total estimated power dissipation.

Equation 2 shows how to calculate the average external current (I_{DD_EXT}) using the above parameters:

$$I_{DD\_EXT} = O \times f/2 \times V_{DD\_EXT} \times C_L \times U \times TR$$

Equation 2. Total External Current (I_{DD_EXT}) Calculation

Estimated average external power consumption (P_{DD_EXT}) can then be calculated as:

$$P_{DD\_EXT} = V_{DD\_EXT} \times I_{DD\_EXT}$$

Substituting from Equation 2, this calculation becomes:

$$P_{DD\_EXT} = V_{DD\_EXT}^2 \times O \times f/2 \times C_L \times U \times TR$$

Table 4 is an excerpt from the example application use case contained on the *VDD_EXT Power Domain* tab in the power calculator and shows the Link Port interface portion to illustrate the concept more clearly.

Peripheral	Frequency (Hz)	# of Pins	C/pin (F)	Toggle Ratio	Utilization Factor	V_{DD_EXT} (V)	P_{DD_EXT} (mW)
Link Ports	5.650E+7	9	3.00E-11	0.5	1.00	3.30	41.8

Table 4. V_{DD_EXT} Power Consumption Example

Beyond the peripheral pins, there is one additional output pin on ADSP-SC57x processors that may contribute to the V_{DD_EXT} supply domain's power profile. Specifically, if the system design uses a crystal to provide the CLKIN signal to the processor, the XTAL output pin will be driven when the PLL is active. When this is the case, the XTAL pin must be added as a unique 1-pin entry in the table on the *VDD_EXT Power Domain* tab in the power calculator. The output drive frequency is exactly the CLKIN rate, and the pin capacitance value can be obtained from the crystal datasheet.

For most crystals, the voltage swing will likely be less than V_{DD_EXT}; therefore, using V_{DD_EXT} in computations would be a worst-case model in terms of power dissipation profiling.

Similar to estimating the I_{DD_EXT} current, the I_{DD_DMC} current consumption for the on-chip LPDDR1/DDR2/DDR3 controller can be estimated depending on the number of pins toggling and the toggle rate. V_{DD_DMC} is used for the voltage swing (obtain the maximum V_{DD_DMC} specification from the datasheet), and the designer only needs to consider the pins of the employed DMC. The *VDD_DMC Power Domain* tab in the power calculator includes a table similar to the one referenced by Table 4, with the DDR pins grouped by function (e.g., address, data, control, and clock) for the user to customize based on the application.

Power Consumption in the USB Power Domain (P_{DD_USB})

The amount of current consumed in the V_{DD_USB} domain varies with the USB mode of operation. Table 5 can be found on the *USB* tab in the power calculator, depicting the current consumption for different modes of operation.

USB Mode	I_{DD_USB} (mA)
NOT USED	0
SUSPEND-ON	0.055
FS-MODE	14.68
HS-MODE	36.33

Table 5. I_{DD_USB} Current

General Guidelines for Power Supply and Thermal Relief Designs

While estimating average total power associated with a given application, power supply and thermal relief designs must always consider the worst-case scenario in order to prevent operational failures due to the processor being operated out-of-spec as a result of a sagging power rail or an out-of-bounds junction temperature. The following sections provide some advice supporting this methodology.

Power Supply Sizing

DO:

- Use the maximum expected voltages associated with all of the influencing power domains involved in each of the look-ups and computations discussed throughout this application note
- Use the junction temperature associated with the maximum ambient temperature (T_A) that the application is expected to be subjected to for all temperature-related look-ups and computations discussed throughout this application note
- Use the highest ASF possible for the application being run
- Calculate each unique voltage domain separately

DO NOT:

- Use typical I_{DD}, nominal voltage, or room temperature specifications
- Use total device power alone

Thermal Relief

DO:

- Use nominal voltages
- Use the junction temperature associated with the maximum ambient temperature (T_A) that the application is expected to be subjected to
- Use the Full-on-Typical (or lower) ASF to match realistic application code activity levels

- Calculate total thermal power for all voltage domains

DO NOT:

- Use typical I_{DD} specifications or room temperature when calculating thermal power
- Use maximum voltage (this is not realistic, as any transient will exceed the maximum voltage specification)

Example Application Using the Power Calculator

This section walks through an example application to illustrate how to use the associated power calculator tool described throughout this EE-note. There are three tabs in the power calculator that contain color-coded cells along with the guidance to populate the yellow cells with the needed system settings and let the calculator automatically populate the green cells with either data from other tabs on the spreadsheet or with a calculated result from the user inputs. Some of the yellow cells are free form, whereas others are selectable via a pull-down, and the following sections describe what user input is required on each tab to arrive at the overall power dissipation estimation.

Power Estimation Tab

The first tab in the power calculator spreadsheet is the *Power Estimation* tab. This is the main interface for the power calculator, where input is required to properly model the intended system. On this tab, the user must provide all the information regarding the power supplies and intended clock rates throughout the system, as well as the other influences on the overall power dissipation discussed throughout this application note (e.g., core activity, DMA rates, etc.). This tab works in conjunction with the other tabs in the spreadsheet to provide the total power dissipation for the application as a function of all the configurable system-dependent parameters.

Set the Power Domains and Junction Temperature

The first step is to set the power domains and temperature to the maximum levels expected by the application. For example, consider a design that utilizes the following:

- V_{DD_INT} = 1.1 V
- V_{DD_EXT} = V_{DD_USB} = 3.3 V
- V_{DD_DMC} = 1.8 V
- T_J = 70 °C

Since the V_{DD_INT} domain and T_J values are used as inputs to look-up tables on other tabs in the power calculator to extract the needed current dissipation data for the calculation, they are selectable via pull-downs in the *Operating Conditions* table on the *Power Estimation* tab based on the discrete levels defined in the *Static* and *Dynamic Current* tables in the processor datasheet.

The *Static* and *Dynamic Current* tables included in the power calculator are from the referenced processor datasheet. Always verify that the data in the calculator matches what is in the **current** datasheet to ensure that the proper specifications are being included.

The other relevant power domains must also be configured on the *Power Estimation* tab. Manually input the appropriate values for the V_{DD_EXT} (in the *V_{DD_EXT}* section), V_{DD_DMC} (in the *V_{DD_DMC}* section), and V_{DD_USB} (in the *V_{DD_USB}* section) domains into the relevant yellow cells, and the calculator will compute the current and/or power in the associated green cells.

There is no error checking built into the calculator for the range of these power domains. A *Configuration Warning* is associated with each of these yellow cells indicating that the values input must be verified against the processor datasheet for validity.

The V_{DD_EXT} and V_{DD_DMC} cells will be influenced by activity on the *VDD_EXT* and *VDD_DMC Power Domain* tabs, respectively.

Set the Clocks

With the power domains and temperature set, the next step is to input all the clocking information that will define the dynamic currents expected throughout the system. For example, consider a design that utilizes the following:

- f_{CCLK_A5} = 450 MHz
- f_{CCLK_SHARC1} = 450 MHz
- f_{CCLK_SHARC2} = 450 MHz
- f_{DCLK} = 400 MHz
- f_{SYSCLK} = 225 MHz
- f_{SCLK0} = 112.5 MHz
- f_{SCLK1} = 56.25 MHz
- f_{OCLK} = 225 MHz

Manually input the above eight values into the corresponding yellow cells in the *Clock Domains & DMA Rates* table, and the calculator will compute the associated dynamic current in the adjacent green cells.

There is no error checking built into the calculator for the range of these operating frequencies. A *Configuration Warning* is associated with each of these yellow cells indicating that the values input must be verified against the processor datasheet for validity.

Set the Activity Scaling Factors (ASFs)

As discussed in Using ASFs to Establish Application-Specific Total Average Power Profile, the next step is to analyze the application to determine what sort of core loads to associate with the application in order to establish the dynamic power dissipation component for each core, which is handled in the yellow cells in the *COREx Average ASF* tables in the V_{DD_INT} section of the *Power Estimation* tab. The proper input for these cells is a fractional number from 0.0 to 1.0 indicating the percentage of time spent by the application at that discrete ASF level, and the calculator outputs the *Average ASF* (as described by Equation 1) in the green cell based on the data on the *Core Activity Factors* tab.

There is no error checking built into the calculator for the sum of these percentages. A hover message indicating that the "*Sum of these fractions should be 1*" appears to advise the user when inputting data in this section.

The *ASF* tables included in the power calculator are from the referenced processor data sheet. Always verify that the data in the calculator matches what is in the **current** datasheet to ensure that the proper specifications are being included.

Generally speaking, a power supply design should use a maximum power dissipation profile accounting for the worst-case scenario, in which case the peak activity value should always be used for all cores used in the system. In this case, it is sufficient to simply input a 1 in the *100 (Peak)* cell for all three cores. However, to establish an average power profile, the calculator is built to account for all the discrete ASF levels defined by the processor datasheet, and the yellow cells can be populated to reflect the actual system model.

For example, after analyzing the application, it is determined that the following describes the core activity levels:

- CORE0 (ARM Cortex-A5): 35% Idle, 65% Peak
- CORE1 (SHARC+ Core1): 16% Idle, 84% Peak
- CORE2 (SHARC+ Core2): 100% Typical

When input into the calculator, the corresponding average ASFs are computed, as follows:

- ASF_{A5} = 0.868
- ASF_{SHARC1} = 1.000
- ASF_{SHARC2} = 1.000

These ASFs are then used by the calculator to compute the dynamic current component for each core in the green cells in the *Contribution (mA)* column in the *Clock Domains & DMA Rates* table.

Set the Peripheral Resource Usage

As discussed in this EE-note, the more complex peripherals (i.e., USB, MLB, and GigE) dissipate dynamic power in the V_{DD_INT} domain as part of the total internal dynamic current ($I_{DD\_INT\_TOT}$) equation in the processor datasheet. This is accounted for in the V_{DD_INT} section of the *Power Estimation* tab in a series of pull-down yellow cells in the *Resource Usage* table, and the selectable mode options for each row provide a look-up value into an associated table on another tab in the calculator, as follows:

- USB0: extracts data from the $I_{DD\_INT\_USB\_DYN}$ column on the *USB* tab
- MLB: extracts data from the $I_{DD\_INT\_MLB\_DYN}$ column on the *MLB* tab
- GigE: extracts data from the $I_{DD\_INT\_GIGE\_DYN}$ column on the *GigE* tab

For the MLB and GigE blocks, it is simply a case of selecting whether the peripheral block is used or not used from the pull-down, in which case the calculator will link in the respective addend for the total internal dynamic current calculation ($I_{DD\_INT\_TOT}$). For the USB block, the supported modes of operation are selectable so that the calculator can extract the appropriate data from the design simulations available on the USB tab.

For example, if the system had the following characteristics:

- USB: enabled in High-Speed mode
- MLB: unused
- GigE: enabled

Then the *Resource Usage* table would be populated as shown in Table 6.

Resource Usage		Contribution (mA)
USB0	HS-MODE	9.60
MLB-6 Pin	NOT USED	0.00
Gigabit Ethernet	USED	10.00
Dynamic Current (A2)		**19.60**

Table 6. Example Resource Usage

In Table 6, the green cells are populated by the calculator based on the pull-downs, where all values were obtained from associated look-up tables.

Select Appropriate DMA Activity Level

The final user input required on the *Power Estimation* tab is the *DMA/Peripheral Usage* row in the *Clock Domains & DMA Rates* table in the V_{DD_INT} section. It is here that the user must select from the three defined profiles discussed in Estimating DMA Dynamic Current ($I_{DD\_INT\_DMA\_DR\_DYN}$) (HIGH, MEDIUM, or LOW) as the closest match to the data activity in the system. When selected via the yellow pull-down, the corresponding look-up value from the $I_{DD\_INT\_DMA\_DR\_DYN}$ column on the *DMA_Usage* tab will be populated in the corresponding green cell in the *Contribution (mA)* column. For example, if the *MEDIUM* profile is selected (1500 MBPS), the value for $I_{DD\_INT\_DMA\_DR\_DYN}$ is 47.20 mA.

Select the Desired Static Power Profile

Next to the *Operating Conditions* table on the *Power Estimation* tab, there is one final user-configurable yellow cell called *Desired Static Power Profile*. As described in this EE-note, sizing a power supply requires that the worst-case scenario be considered, so the default setting is *Maximum*. With this setting, the static current values are extracted from the maximum static current specifications on the *VDD_INT Maximum Static Current* tab (which is a duplicate of the *Static Current* table in the referenced datasheet). There is, however, the option to choose *Typical* from this pull-down, which will instead take the static current data from the equivalent typical static current table on the *VDD_INT Typical Static Current* tab. With *Typical* selected, the associated red bold text warning is output by the calculator:

Warning: Typical current is in the middle of the process distribution. A significant number of devices will exceed typical currents. For system analysis, use maximum power numbers.

While not recommended for doing power supply sizing, typical numbers may be preferred for other analyses and are therefore furnished for reference.

VDD_EXT Power Domain Tab

The next tab requiring user input is the *VDD_EXT Power Domain* tab. It is here that the user must identify each V_{DD_EXT} power domain peripheral that is in use in the system and model its power profile as a function of how often it is on, how many pins are switching, the load capacitance associated with those pins, the voltage swing on the pins, and the frequency at which the pins can switch. As was the case with the *Power Estimation* tab, the yellow cells are those requiring user input, and the green cells are those populated by the calculator.

The V_{DD_EXT} column is automatically populated from the *Power Estimation* tab, and it is on the user to fill in all the yellow cells. Consider an application that uses the link port, two serial ports (SPORTs), one SPI, and a UART. While most of the columns are straightforward in terms of populating them with the appropriate clock frequencies, the

pin capacitance from the design, and the application's use of the peripheral (see Estimating External Power Consumption (P_{DD_EXT} and P_{DD_DMC})), the *Number of Output* pins and *Utilization Factor* are going to be a function of how the peripheral itself is configured. For example, if the following configuration settings apply to the listed peripherals:

- Link port is an 8-bit host interface→one output clock pin and eight output data pins
- SPI0 is enabled as a master transmitter in dual-I/O mode→one output clock pin and two output data pins
- Both SPORTs are single-channel transmitters→one output clock pin and one output data pin

With the above peripheral configuration information, Table 7 could represent such a system after the user inputs the proper number of output pins (O), makes a reasonable guess as to the number of pins switching any given cycle (TR), and supplies information about the percentage of the time the peripheral is enabled (U) after having populated the frequency (f) and load capacitance (C_L).

Peripheral	Frequency in Hz (f)	Number of Output Pins (O)	Pin Capacitance in Farads (C_L)	Toggle Ratio (TR)	Utilization Factor (U)	V_{DD_EXT} (V)	P_{DD_EXT} (mW)
Link Port	5.65E+07	9	3.00E-11	0.55	1.00	3.30	45.685
SPORT0	4.00E+06	2	3.00E-11	1	1.00	3.30	1.307
SPORT1	4.00E+06	2	3.00E-11	1	1.00	3.30	1.307
SPI0	1.20E+07	3	3.00E-11	0.5	0.5	3.30	1.470
UART0	1.15E+05	1	3.00E-11	1	0.25	3.30	0.005
Total Peripheral Power Dissipation (estimated)						**P_{DD_EXT} = 49.77 mW**	

Table 7. Example V_{DD_EXT} Peripheral Usage

The *P_{DD_EXT} (mW)* column contains the results of the calculator applying Equation 2 to the input data in the other columns, and the sum of the power contributions from each of the individual peripheral components is calculated at the bottom of the column. Peripherals can be added/deleted from this profile by inserting/removing rows, as needed.

VDD_DMC Power Domain Tab

The final tab requiring user input is the *VDD_DMC Power Domain* tab. The concepts from VDD_EXT Power Domain Tab apply to this tab as well, except the table is slightly different because it is modeling a single interface that has numerous groups of pins that need to be treated differently based on factors that do not remain consistent across the interface. As was the case on the *VDD_EXT Power Domain* tab, there are green cells that are either populated by the calculator from elsewhere or are the output of a computation, and it is on the user to populate the yellow cells with information regarding the configuration of the DDR controller.

As for the green cells on the *VDD_DMC Power Domain* tab, the power supply information for the *V_{DD_DDR} (V)* column is automatically extracted from the *Power Estimation* tab, as is the *Frequency in Hz (f)* column. Note that the calculator automatically applies the f_{DCLK} rate to the clock (*CLK*) and *Address pins [15:0]* rows, as these pins can switch

at this rate in a worst-case scenario. Due to the double data rate nature of the DDR interface, where data can switch on each clock edge, the data pins must be set to twice the f_{DCLK} rate; therefore, the calculator doubles f_{DCLK} for the *Data pins [15:0]* row. Finally, the control (*CTRL* row) pins can only switch outside of a burst transfer, which means they can only switch at 1/4 or 1/8 the f_{DCLK} rate, as governed by the yellow *Burst Mode* pull-down, so the calculator also accounts for this.

As was indicated in Set the Clocks, the DDR clock was configured to be 400 MHz on the *Power Estimation* tab, so Table 8 could be an example model for the DDR interface for this application after the pin capacitance and other inputs are finalized by the user.

Peripheral		Frequency in Hz (f)	Number of Output Pins (O)	Pin Capacitance in Farads (C_L)	Toggle Ratio (TR)	Utilization Factor (U)	V_{DD_DMC} (V)	P_{DD_DMC} (mW)
DDR2	Address pins [15:0]	4.00E+08	16	5.00E-12	0.25	1.00	1.80	12.96
	Data pins [15:0]	8.00E+08	16	5.00E-12	1	1.00	1.80	103.68
	CTRL	1.00E+08	15	5.00E-12	1	1.00	1.80	12.15
	CLK	4.00E+08	2	5.00E-12	1	1.00	1.80	6.48
						Total DDR Power Dissipation (mW)		**135.27**

Table 8. Example V_{DD_DMC} Use Case

As typical DDR accesses are sequential in nature, it is unlikely that the number of address pins toggling any cycle would exceed 25% (four pins), and a worst-case model assumes the interface is always running (U = 1.00). For average power dissipation, there could be low-power modes employed, making a fractional *Utilization Factor* possible and supported by the calculator.

Summarizing the Process of Estimating Power

With the concepts described and the guidance provided for using the power calculator tool itself, the following is a summary of the steps required to estimate total overall power in an example ADSP-SC57x processor design, using the examples given throughout this EE-note as a reference.

Step 1: Obtain the Internal Static Current Component ($I_{DD\_INT\_STATIC}$)

Use the maximum power rail (V_{DD_INT}) and junction temperature (T_J) values for the application to look up the appropriate maximum $I_{DD\_INT\_STATIC}$ spec from the *Static Current* table in the processor datasheet. In the example discussed in Set the Power Domains and Junction Temperature, V_{DD_INT} = 1.1 V and T_J = 70°C; therefore, the associated value from the *VDD_INT Maximum Static Current* tab is 84 mA.

Step 2: Obtain Baseline Core Dynamic Currents ($I_{DD\_INT\_CCLK\_A5\_DYN}$, $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$, $I_{DD\_INT\_CCLK\_SHARC2\_DYN}$)

Use the same V_{DD_INT} power rail and the expected core clock frequency (f_{CCLK}) to look up the appropriate values in the *Dynamic Current* tables in the processor datasheet for each core. In the example discussed in Set the Clocks, V_{DD_INT} = 1.1 V and all three cores are running at 450 MHz; therefore, the associated values from the equations in Core Dynamic Current (also in the *Dynamic Current* datasheet tables*)* are:

- $I_{DD\_INT\_CCLK\_SHARCx\_DYN}$ = 0.63 x V_{DD_INT} x f_{CCLK_SHARCx} →0.63 x 1.1 x 450 = 311.85 mA
- $I_{DD\_INT\_CCLK\_A5\_DYN}$ = 0.16 x V_{DD_INT} x f_{CCLK_A5} →0.16 x 1.1 x 450 = 79.2 mA

Step 3: Model Application to Establish Activity Scale Factors (ASF_{A5}, ASF_{SHARC1}, ASF_{SHARC2})

Using the definitions of the scale factors in the *Activity Scaling Factors* tables in the datasheet, model the application for each core to determine the processor load as a result of the code being executed. For a maximum calculation, the worst-case ASF at any given time should be used, but an average ASF can be calculated, as described in the Using ASFs section. From the example provided in Set the Activity Scaling Factors (ASFs):

- ASF_{A5} = 0.868
- ASF_{SHARC1} = 1.00
- ASF_{SHARC2} = 1.00

Step 4: Apply ASFs to Core Dynamic Components

The calculated average ASF or the worst-case ASF must then be applied to the core dynamic component for each core as a simple multiplication:

- $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ = $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ x ASF_{SHARC1} → 311.85 x 1.00 = 311.85 mA
- $I_{DD\_INT\_CCLK\_SHARC2\_DYN}$ = $I_{DD\_INT\_CCLK\_SHARC2\_DYN}$ x ASF_{SHARC2} → 311.85 x 1.00 = 311.85 mA
- $I_{DD\_INT\_CCLK\_A5\_DYN}$ = $I_{DD\_INT\_CCLK\_A5\_DYN}$ x ASF_{A5} → 79.2 x 0.868 = 68.71 mA

Step 5: Calculate the System Clock Tree Core Dynamic Currents

The dynamic current dissipated in the V_{DD_INT} domain as a result of the clocks toggling inside the processor are a function of the internal voltage (in Volts) and each clock's frequency (in MHz), as governed by the equations in the processor datasheet. Using the example from Estimating System Clock Tree Currents:

- $I_{DD\_INT\_DCLK\_DYN}$ = 0.08 x f_{DCLK} x V_{DD_INT} → 0.08 x 400.0 x 1.1 = 35.20 mA
- $I_{DD\_INT\_SYSCLK\_DYN}$ = 0.52 x f_{SYSCLK} x V_{DD_INT} → 0.52 x 225.0 x 1.1 = 128.70 mA
- $I_{DD\_INT\_SCLK0\_DYN}$ = 0.28 x f_{SCLK0} x V_{DD_INT} → 0.28 x 112.5 x 1.1 = 34.65 mA
- $I_{DD\_INT\_SCLK1\_DYN}$ = 0.013 x f_{SCLK1} x V_{DD_INT} → 0.013 x 56.25 x 1.1 = 0.80 mA
- $I_{DD\_INT\_OCLK\_DYN}$ = 0.015 x f_{OCLK} x V_{DD_INT} → 0.015 x 225.0 x 1.1 = 3.71 mA

Step 6: Choose a DMA Profile to Obtain Core Dynamic DMA Current ($I_{DD\_INT\_DMA\_DR\_DYN}$)

Calculate the total system DMA bandwidth during peak activity and select the profile that is the closest match. A reasonable $I_{DD\_INT\_DMA\_DR\_DYN}$ ratio beyond the *LOW* profile (~50 mA @ 600 MBPS) baseline is ~33 mA/1000 MBPS. The example in Select Appropriate DMA Activity Level sets the DMA profile to *MEDIUM*, therefore:

- $I_{DD\_INT\_DMA\_DR\_DYN}$ = 47.20 mA

Step 7: Account for Core Dynamic Currents from USB/MLB/GigE Blocks

Each of these blocks dissipates power in the V_{DD_INT} domain and must be considered when estimating the total core dynamic current.

USB Contribution ($I_{DD\_INT\_USB\_DYN}$)

This component can be obtained from either the mode-dependent data on the *USB* tab of the calculator or the worst-case constant addend defined in the processor datasheet. The example discussed in Set the Peripheral Resource Usage employs USB in high-speed mode (HS-MODE). From the *USB* tab in the calculator, this component is:

- $I_{DD\_INT\_USB\_DYN}$ = 9.6 mA

GigE Contribution ($I_{DD\_INT\_GIGE\_DYN}$)

This component is a constant addend detailed in the processor data sheet when the GigE block is enabled in any mode. The example discussed in Set the Peripheral Resource Usage has the GigE block enabled, therefore:

- $I_{DD\_INT\_GIGE\_DYN}$ = 10 mA

MLB Contribution ($I_{DD\_INT\_MLB\_DYN}$)

For automotive models, this component is a constant addend detailed in the processor data sheet when the MLB block is enabled in any mode. The example discussed in Set the Peripheral Resource Usage has the MLB block disabled, therefore:

- $I_{DD\_INT\_MLB\_DYN}$ = 0.0 mA

Step 8: Calculate Total Internal Power Dissipation ($P_{DD\_INT\_TOT}$)

Add the static internal current (Step 1) component to the sum of all the dynamic internal current components (Step 4 through Step 7) to get the total current in the V_{DD_INT} domain ($I_{DD\_INT\_TOT}$):

$$I_{DD\_INT\_TOT} = I_{DD\_INT\_STATIC} + I_{DD\_INT\_CCLK\_SHARC1\_DYN} + I_{DD\_INT\_CCLK\_SHARC2\_DYN} + I_{DD\_INT\_CCLK\_A5\_DYN} + I_{DD\_INT\_DCLK\_DYN} + I_{DD\_INT\_SYSCLK\_DYN} + I_{DD\_INT\_SCLK0\_DYN} + I_{DD\_INT\_SCLK1\_DYN} + I_{DD\_INT\_OCLK\_DYN} + I_{DD\_INT\_USB\_DYN} + I_{DD\_INT\_MLB\_DYN} + I_{DD\_INT\_GIGE\_DYN} + I_{DD\_INT\_DMA\_DR\_DYN}$$

$I_{DD\_INT\_TOT}$ = 84 + 311.85 + 311.85 + 68.71 + 35.2 + 128.7 + 34.65 + 0.80 + 3.71 + 9.6 + 10 + 47.20 = 1046.27 mA

With the total $I_{DD\_INT\_TOT}$ current calculated, the total power ($P_{DD\_INT\_TOT}$) can then be estimated:

- $P_{DD\_INT\_TOT} = I_{DD\_INT\_TOT} \times V_{DD\_INT}$ → 1046.27 mA x 1.10 V = 1150.9 mW

Step 9: Calculate External Power Dissipation ($P_{DD\_EXT\_TOT}$)

The total external power dissipation ($P_{DD\_EXT\_TOT}$) is comprised of the power dissipated in each of the other three critical power domains (V_{DD_EXT}, V_{DD_DMC}, and V_{DD_USB}).

Calculate Power Dissipated in the V_{DD_EXT} Domain (P_{DD_EXT})

Model the application using the concepts discussed in Estimating External Power Consumption (P_{DD_EXT} and P_{DD_DMC}) to estimate the power dissipated in the V_{DD_EXT} domain (P_{DD_EXT}). From the example discussed in VDD_EXT Power Domain Tab:

- P_{DD_EXT} = 49.77 mW

Calculate Power Dissipated in the V_{DD_DMC} Domain (P_{DD_DMC})

Model the application using the concepts discussed in Estimating External Power Consumption (P_{DD_EXT} and P_{DD_DMC}) to estimate the power dissipated in the V_{DD_DMC} domain (P_{DD_DMC}). From the example discussed in VDD_DMC Power Domain Tab:

- P_{DD_DMC} = 135.27 mW

Calculate Power Dissipated in the V_{DD_USB} Domain (P_{DD_USB})

This component is comprised of the power dissipated in the V_{DD_USB} domain by the USB controller. Since the example in Set the Peripheral Resource Usage employs USB in the high-speed (HS-MODE) mode of operation, the I_{DD_USB} current is 36.33 mA, therefore:

- $P_{DD\_USB} = I_{DD\_USB} \times V_{DD\_USB} \rightarrow$ 36.33 mA x 3.3 V = 119.89 mW

With all of the components for the total external power ($P_{DD\_EXT\_TOT}$) computed, they can be summed:

$$P_{DD\_EXT\_TOT} = P_{DD\_EXT} + P_{DD\_DMC} + P_{DD\_USB}$$

- $P_{DD\_EXT\_TOT}$ = 49.77 + 135.27 + 119.89 →304.93 mW

Step 10: Calculate Total Power Dissipation (P_{DD_TOT})

Finally, with all of the core and system elements properly modelled, the total power dissipation can be calculated as the sum of the internal ($P_{DD\_INT\_TOT}$) and external ($P_{DD\_EXT\_TOT}$) power dissipation components:

- $P_{DD\_TOT} = P_{DD\_INT\_TOT} + P_{DD\_EXT\_TOT} \rightarrow$ 1150.9 + 304.93 = 1455.83 mW

Due to rounding in the calculations in the example, the values output in the green cells of the power calculator may differ slightly from those presented.

References

[1] *ADSP-SC570/571/572/573/ADSP-21571/21573 Embedded Processor Data Sheet.* Rev 0, July 2017. Analog Devices, Inc.

[2] Associated ZIP File for *Estimating Power on ADSP-SC57x/ADSP-2157x SHARC+® Processors (EE-397)*. Rev 1, July 2017. Analog Devices, Inc.

[3] *ADSP-SC57x SHARC+® Processor Hardware Reference.* Preliminary Revision 0.2, May 2017. Analog Devices, Inc.

[4] *Estimating Power for ADSP-BF531/BF532/BF533 Blackfin® Processors (EE-229).* Rev 4. December 12, 2007. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – July 19th, 2017 *by Nabeel Shah and Joe B.*	*Initial Release.*