AN-1449
APPLICATION NOTE

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Full Hot Swap Support with the ADM3066E for Glitch Free PLC Module Insertion

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INTRODUCTION

Industrial automation programmable logic controller (PLC) communication ports, which commonly use RS-485 interfaces, can be subjected to electrostatic discharge (ESD) strikes and communication errors due to hot insertion of modules to the PLC rack. These hazards can either corrupt data communication or cause permanent damage to the RS-485 interface.

RS-485 is specified as a multipoint standard, which means that up to 32 transceivers can be connected on the same bus, and any of the 32 transceivers can drive signals onto the RS-485 bus. Some transceivers, such as the ADM3066E, can support up to 128 bus nodes. Full hot swap support in a multipoint system is important because it helps to ensure that only one RS-485 driver is active at any time. If more than one driver is active on an RS-485 bus, a bus contention situation exists, which can lead to data errors.

The ADM3066E full hot swap feature is designed to address unintentional bus contention due to unintended enabling of the RS-485 transceivers. RS-485 transceivers can be unintentionally enabled due to capacitive coupling of power or ground to the RS-485 driver and receiver enable inputs. RS-485 transceivers can also be enabled due to leakage currents from adjacent microcontrollers causing drift in the driver and receiver enable inputs.

ESD on the exposed RS-485 connectors and cabling for PLC module communications is a common phenomenon. The system level IEC 61131-2 standard for programmable controllers requires a minimum of ±6 kV contact and ±8 kV air IEC 61000-4-2 ESD protection. The ADM3066E exceeds this requirement with ±12 kV contact and ±12 kV air IEC 61000-4-2 ESD protection.

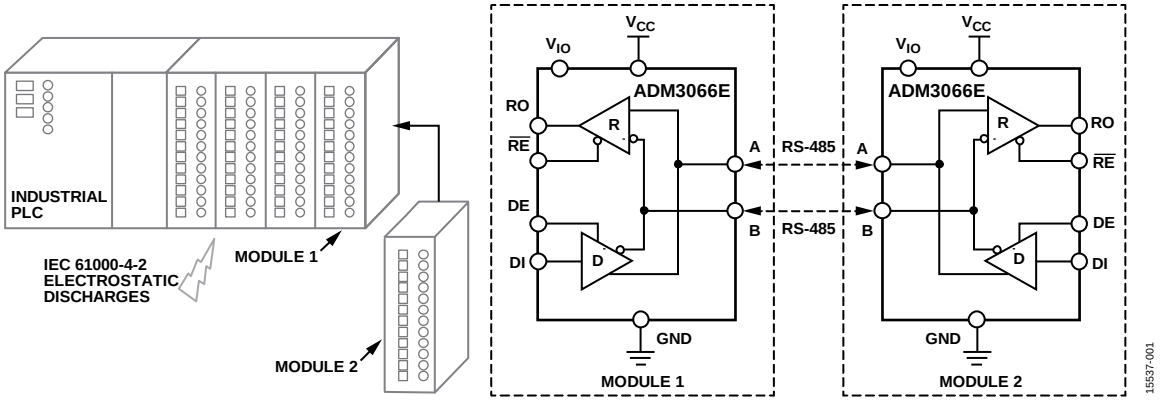

Figure 1. Adding Module 2 with an RS-485 Communications Port to a Live Industrial PLC Bus

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REVISION HISTORY

5/2017—Revision 0: Initial Version

FULL HOT SWAP SUPPORT

GLITCH FREE POWER UP AND POWER DOWN

When a module or printed circuit board (PCB) is inserted into a powered (or hot) backplane, differential disturbances to the data bus can lead to data errors. During this period, processor logic output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of the RS-485 transceivers to a defined logic level.

As shown in Figure 2, leakage currents up to ±100 µA from the high impedance state of the processor logic drivers can cause standard complementary metal-oxide semiconductor (CMOS) to enable the DE and $\overline{RE}$ inputs of a transceiver to drift to an incorrect logic level. Additionally, as shown in Figure 3, parasitic circuit board capacitance can cause coupling of V_{CC} or GND to the enabled inputs. Without hot swap capability, these factors can improperly enable the driver or receiver of the transceiver. To prevent improperly enabled drivers or receivers, the ADM3066E has integrated hot swap circuitry. This hot swap circuitry ensures that when V_{CC} rises, an internal pull-down circuit holds DE low and $\overline{RE}$ high. In this configuration, both driver and receiver are disabled for a short period of time. After the initial power-up sequence, the pull-down circuit becomes transparent, resetting the hot swap tolerable input.

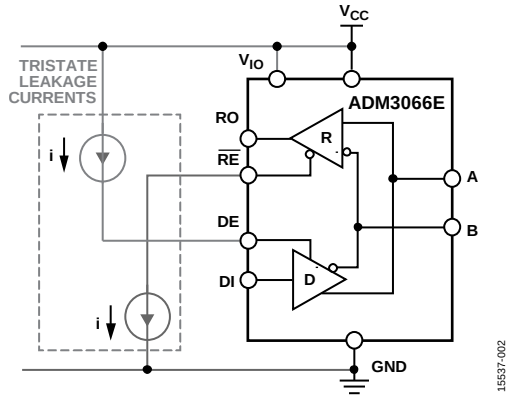

Figure 2. Tristate Leakage Currents can Drive Logic Pins to Incorrect Levels

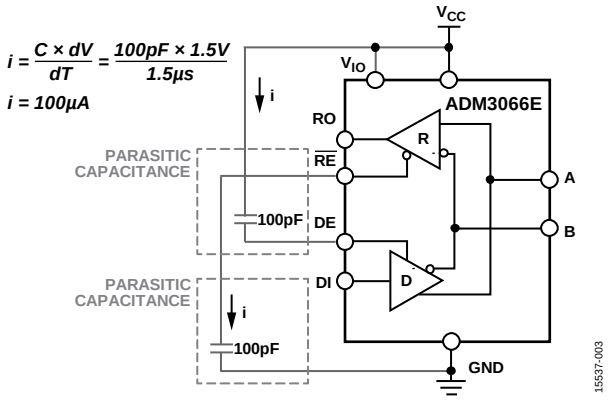

Figure 3. Parasitic Capacitances can Drive Logic Pins to Incorrect Levels

COMPREHENSIVE HOT SWAP SUPPORT

Table 1 shows the input and output pin state combinations used to test the ADM3066E hot swap capability. When an ADM3066E circuit board is inserted into a powered (or hot) backplane, any of the test conditions listed in Table 1 are possible. Because the ADM3066E has both a low voltage logic supply, V_{IO}, and a V_{CC} power supply pin, a number of different power supply sequences and conditions can occur.

The ADM3066E A and B outputs remain in a high impedance state during power up, and then default to the states described in Table 1. For example, when V_{IO} and V_{CC} power up at the same time and the $\overline{RE}$ pin is pulled low, with the DE and DI pins pulled high, the A and B outputs remain in high impedance until settling at an expected default high for the A pin, and expected default low for the B pin.

Table 1. Input and Output Pin State Combinations

V_{CC} and V_{IO}	Inputs During Power Up			Output Transitions at Power Up	
Supply Status	**RE**	**DE**	**DI**	**A**	**B**
V_{IO} and V_{CC} Power Up at the Same Time	L	V_{IO}	V_{IO}	Z to H	Z to L
	L	V_{IO}	L	Z to L	Z to H
	V_{IO}	V_{IO}	X	Z to H/L	Z to H/L
V_{CC} Powers On with V_{IO} Already Powered On	L	H	H	Z to H	Z to L
	L	H	L	Z to L	Z to H
	L	L	X	Z	Z
	H	H	X	Z to H/L	Z to H/L
V_{IO} is Not Powered On	Z	Z	X	Z	Z

X means don't care.
Z means high impedance.
L means low level on inputs/outputs.
H means high level on inputs/outputs.
H/L means high level or low level on outputs.

ROBUST IEC61000-4-2 ESD

ADM3066E SYSTEM LEVEL SOLUTION

ESD on the exposed RS-485 connectors and cabling for PLC module communications is a common phenomenon. The system level IEC 61131-2 standard for programmable controllers requires a minimum of ±6 kV contact and ±8 kV air IEC 61000-4-2 ESD protection. The ADM3066E exceeds this requirement with ±12 kV contact and ±12 kV air IEC 61000-4-2 ESD protection.

Figure 4 shows the 8 kV contact discharge current waveform from the IEC 61000-4-2 standard compared to the human body model (HBM) ESD 8 kV waveform. Figure 4 shows that the two standards specify different waveform shapes and peak currents. The peak current associated with a IEC 61000-4-2 8 kV pulse is 30 A, whereas the corresponding peak current for the HBM ESD is more than five times less, at 5.33 A. The other difference is the rise time of the initial voltage spike, with IEC 61000-4-2 ESD having a much faster rise time of 1 ns, compared to the 10 ns associated with the HBM ESD waveform. The amount of power associated with an IEC 61000-4-2 ESD waveform is much greater than that of a HBM ESD waveform. The HBM ESD standard requires the equipment under test to be subjected to 3 positive and 3 negative discharges; in comparison, the IEC 61000-4-2 ESD standard requires 10 positive and 10 negative discharge tests.

The ADM3066E with its IEC 61000-4-2 ESD ratings is better suited for operation in harsh environments compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

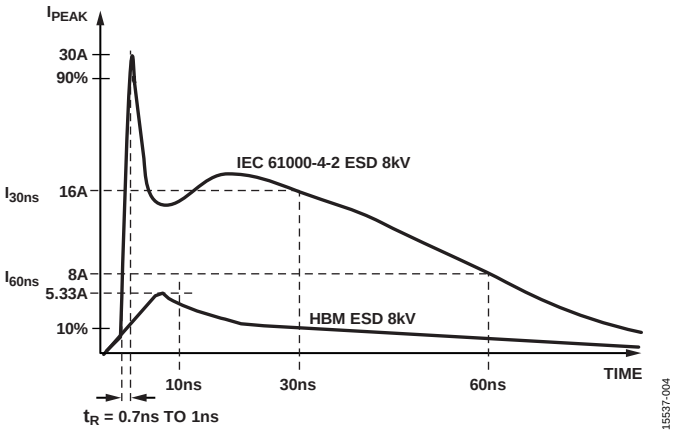

Figure 4. IEC 61000-4-2 ESD +8 kV Waveform Compared to HBM ESD +8 kV Waveform