

Powering the **AD9272** Octal Ultrasound ADC/LNA/VGA/AAF with the **ADP5020** Switching Regulator PMU for Increased Efficiency

CIRCUIT FUNCTION AND BENEFITS

This circuit utilizes the **ADP5020** power management unit to provide the individual power supply rails required for the **AD9272** octal LNA/VGA/AAF/ADC and crosspoint switch.

The **ADP5020** is a low noise power management unit (PMU) providing three outputs: two synchronous buck channels (600 mA and 250 mA, respectively) and one low dropout linear regulator (LDO) channel (150 mA). The input voltage to the circuit is a +5.5 V supply rail.

The **AD9272** is optimized for ultrasound applications and has a time-gain compression path that employs eight channels of low noise amplifiers (LNAs), variable-gain amplifiers (VGAs) with 42 dB of attenuation range, 8 MHz to 18 MHz antialiasing filters, and 12-bit 10 MSPS to 80 MSPS ADCs. The CW Doppler path contains an eight channel, fully differential crosspoint switch for current output summation. This is an ideal solution when using multiple **AD927x** devices for portable ultrasound applications where low power is key.

CIRCUIT DESCRIPTION

Table 1. Devices Connected/Referenced

Product	Description
AD9272	Octal LNA/VGA/AAF/ADC and crosspoint switch
ADP5020	Power management unit for imaging modules

Figure 1 shows this **ADP5020** power supply solution that supplies all the necessary input power rails to the **AD9272** octal LNA/VGA/AAF/ADC and crosspoint switch. The input to the **ADP5020** is a +5.5 V dc bus supply with low ripple. The **ADP5020** outputs are configured and connected to each of the **AD9272** required supplies, including AVDD2 (+3.0 V at 363 mA) supply, AVDD1 (+1.8 V at 209 mA) supply, and DRVDD (+1.8 V at 50 mA) supply. The switching frequency of the **ADP5020** is 3 MHz, which allows the use of smaller, less expensive inductors. The number of components used in this circuit is less than would be required using three separate low dropout (LDO) regulators with their supporting components.

A simple filter was used on each supply output—consisting of a surface-mount chip ferrite bead (FB) and a 10 μF capacitor in parallel with a 0.1 μF capacitor. After the filter, the voltages are distributed to the power planes on the PCB where there is additional localized decoupling at each IC. Using a 5 MHz analog input frequency and sample clock of 40 MSPS the test results were generated as shown in Figure 2. An FFT output spectrum with maximum gain setting (zero attenuation or +1.6 V) on the GAIN+ pin is shown.

Table 2 shows data taken on the **AD9272** using linear regulators (1.8 V and 3.0 V versions of the **ADP3339** family) and the **ADP5020**. Signal-to-noise with respect to full-scale (SNRFS) and spurious-free dynamic range (SFDR) is presented for two VGA gain settings (0 dB and -42 dB).

Another test shown in Table 2 is the dynamic range test. In this test no signal is applied, but the input is terminated so that the noise floor can be measured using the FFT.

In summary, there is no degradation in SNR, SFDR, or dynamic range when using the **ADP5020** switching regulator design. The FFT noise floor responses look nearly identical and do not have any measurable frequency components associated with the switching frequency.

The efficiency calculations in Table 3 compare the overall efficiency of an LDO regulator design to the switching regulator design. Both evaluation boards used for this experiment use the same in-line or bus voltage in order to calculate the power loss comparison appropriately from input to output for each regulator solution. The switching regulator (**ADP5020**) design provides an overall improvement in efficiency of 25%. This is roughly an 800 mW power savings for a single **AD9272**. This will quickly translate into further power savings when multiple devices are used in a system.

Proper layout and circuit partitioning are key to a successful design. Use tightly coupled PCB stackup (power and ground planes) to improve bypassing. Switcher inductors should be mounted on the opposite side of the PCB to help eliminate magnetic flux coupling to sensitive components. Adequate supply filtering is paramount. Use two-stage output filters to reduce ripple and attenuate noise. Take the time to understand current flow, as well as component or adjacent circuitry placement. Ensure good isolation between circuits.

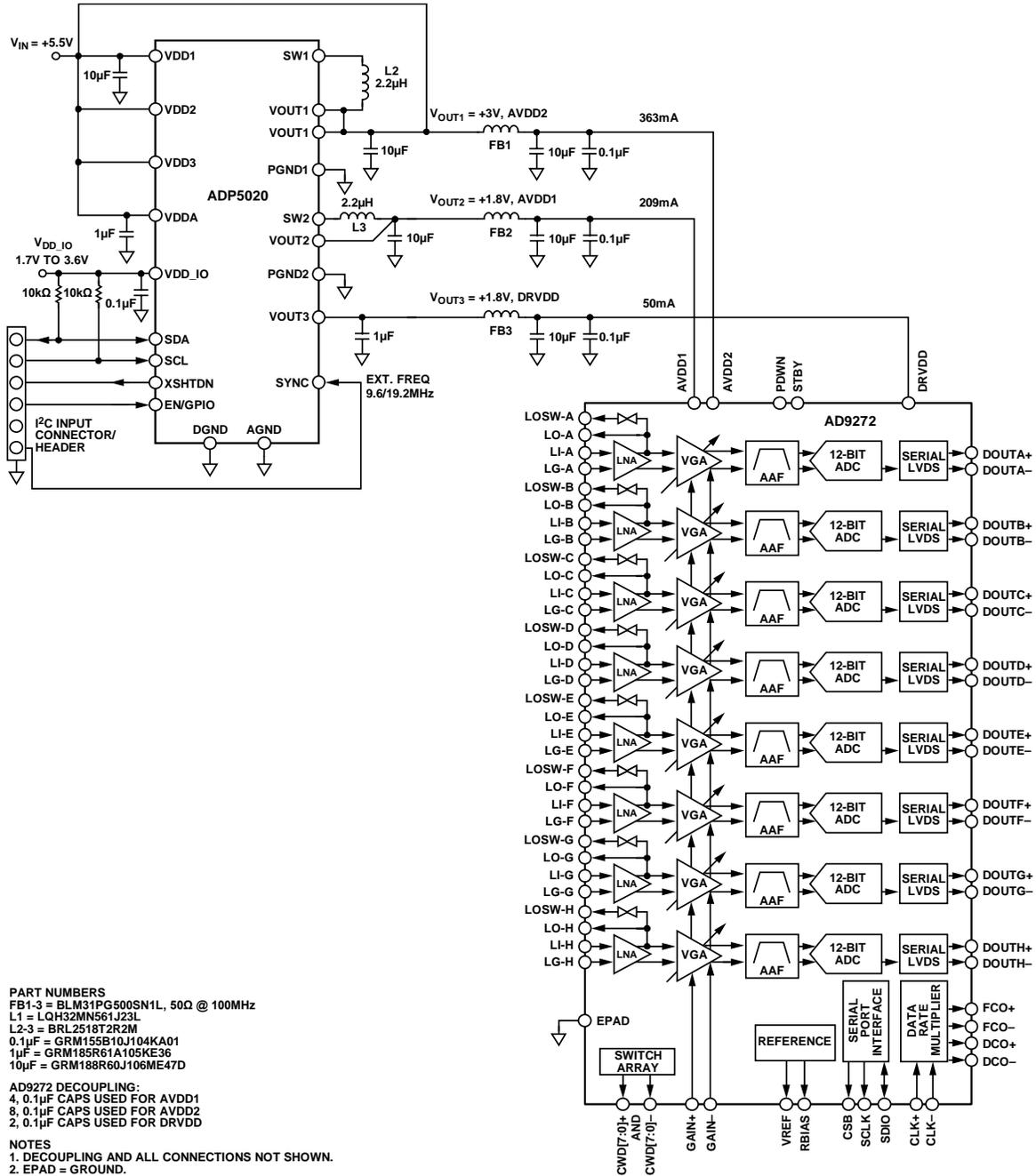


Figure 1. ADP5020 Connected to the AD9272 (Simplified Schematic: Decoupling and All Connections Not Shown)

Table 2. AD9272 Performance Using ADP3339 Family LDOs vs. ADP5020 PMU¹

Applied Signal Conditions	VGA Attenuator (dB)	ADP3339 LDOs		ADP5020 PMU	
		SNRFS (dBFS)	SFDR (dBc)	SNRFS (dBFS)	SFDR (dBc)
FFT Performance Test: 5 MHz Full-Scale Signal Applied	-42	62.9	52.0	62.9	51.3
FFT Performance Test: 5 MHz Full-Scale Signal Applied	0	54.2	53.8	54.3	50.7
Dynamic Range Test: No Full-Scale Signal Applied	-42	62.9	0.6	62.9	1.1
Dynamic Range Test: No Full-Scale Signal Applied	0	53.2	0.2	53.3	0.3

¹ Other test conditions: LNA gain = 21 dB, PGA gain = 30 dB, sampling frequency = 40 MSPS.

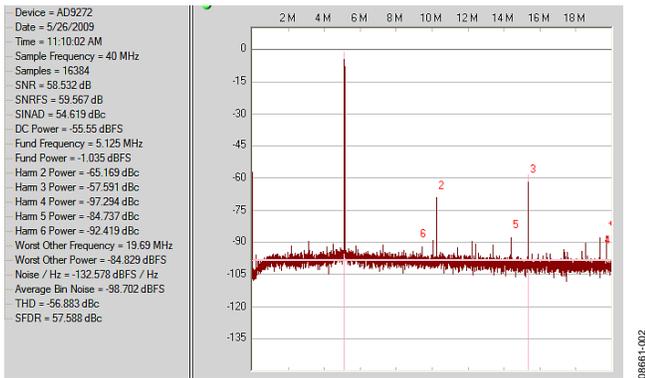


Figure 2. Output Spectrum with 5 MHz AIN at Full Gain (0 dB Attenuation), Sampling Rate = 40 MSPS, with ADP5020 Supplies

The ADC load current is essentially constant and proportional to the sampling clock frequency. Since the ADC load is essentially constant, the transient response of the switcher is not as important to the design as it would be in a stepped load application, such as driving an FPGA.

Layout of the switching regulator part of the circuit is especially critical; the ADP5020 evaluation board should be used as a guide.

Table 3. Linear vs. Switching Regulator Efficiency

	ADP3339 LDOs (BUS Voltage = 4.35 V)	ADP5020 PMU (BUS Voltage = 4.44 V)
Input Voltage/Current	3.0 V AVDD2: 4.35 V at 0.363 A = 1.58 W 1.8 V AVDD1: 4.35 V at 0.209 A = 0.909 W 1.8 V DRVDD: 4.35 V at 0.05 A = 0.218 W Total Power = 2.706 W	4.44 V at 0.425 A = 1.89 W
Output Voltage/Current	3.0 V AVDD2: 2.895 V at 0.363 A = 1.08 W 1.8 V AVDD1: 1.788 V at 0.209 A = 0.374 W 1.8 V DRVDD: 1.798 V at 0.05 A = 0.09 W Total Power = 1.547 W	Total Power = 1.89 W 3.0 V AVDD2: 2.985 V at 0.363 A = 1.08 W 1.8 V AVDD1: 1.788 V at 0.209 A = 0.374 W 1.8 V DRVDD: 1.798 V at 0.05 A = 0.09 W Total Power = 1.547 W
Overall Efficiency	57%	82%

Common Variations

The ADP5020 PMU must be programmed via the I²C interface if voltages other than the factory fuse set default values are required (VOUT1 = 3.3 V, VOUT2 = 1.2 V, VOUT3 = 1.8 V). The ADP5022 is a dual 3 MHz, 600 mA/300 mA buck regulator with a 150 mA LDO. This part has factory programmable default output voltages for all three channels. The buck channels can be programmed for voltages between 1.1 V and 3.3 V; the LDO channel can be programmed for voltages between 1.2 V and 3.3 V.

There are a few other variations to consider when using switching regulators with ADCs and AFEs in general. The AD9271, AD9273, AD9276, and AD9277 could be used as suitable alternatives to the AD9272. Similar circuits have also been verified in the lab using the ADP2114 dual output switching regulator and AD9268 16-bit, dual channel, 125 MSPS analog-to-digital converter. Both low dropout (LDO) regulators and switching circuit solutions work when powering ADCs and high performance analog front ends (AFE). LDO circuits suffer in efficiency. Switching solutions show increased efficiency and lower power dissipation without degradation to ADC performance. Further efficiency will be realized when using multiple devices.

LEARN MORE

[Analog Devices ADIsimPower™ Regulator Interactive Design Tool.](#)

Data Sheets and Evaluation Boards

[ADP5020 Data Sheet](#)

[ADP5020 Evaluation Board](#)

[ADP5022 Data Sheet](#)

[AD9272 Data Sheet](#)

[AD9272 Evaluation Board](#)

Revision History

6/13—Rev. A to Rev. B

Changed Document Title from CN-0135 to AN-1210	Universal
Changes to Circuit Description Section	1
Changes to Learn More Section	4

2/11—Rev. 0 to Rev. A

Changes to Figure 1	2
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10/09—Revision 0: Initial Version