ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

CIRCUITS FROM THE LAB REFERENCE DESIGNS

Selected Test and Measurement Solutions

Learn more at *analog.com /instrumentation*

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 •
www.analog.com

Circuits from the Lab® Reference Designs for Test and Measurement

INTRODUCTION

This anthology of circuit notes contains a hand-picked set of recent test and measurement reference designs for analog, mixed-signal, and radio frequency (RF) design challenges. Instrumentation engineers can use these circuit notes as standalone solutions, or as foundations for more complex circuits and subsystems.

Built and verified for function and performance by applications experts at Analog Devices, Inc., these circuit designs include:

- Comprehensive documentation for easier use with a variety of applications.
- Complete design and integration files to minimize system integration issues.
- Factory tested evaluation hardware and development platforms for rapid prototyping.

These designs help save time, lower risk, and improve time to market. Learn more about Analog Devices Reference Designs at the on-line Design Center, or visit the Instrumentation page to view the latest information on new products and solutions.

REFERENCE DESIGNS

The following reference designs are included in this anthology:

CN-0407
Ultrahigh Sensitivity Femtoamp Measurement Platform

CN-0399
Battery or USB Powered 9 kHz to 6 GHz RMS Power Measurement System

CN-0385
Isolated, Multichannel Data Acquisition System with PGIA for Single-Ended and Differential Industrial Level Signals

CN-0191
20-Bit, Linear, Low Noise, Precision, Bipolar ±10 V DC Voltage Source

DC2591A
LTC4316 EasySMU: I^2C Address Translator and Simple Multichannel Source Measurement Unit

DC2132A
24 V, 3 A Constant Voltage, Constant Current Bench Supply

CN-0387
Calibration-Free Return Loss Measurement System

CN-0375
Broadband Low Distortion Transmitter for 3G, 4G, and LTE

CN-0374
RF-to-Bits Solution Offers Precise Phase and Magnitude Data to 6 GHz

CN-0369
Translation Phase-Locked Loop with Low Phase Noise

TABLE OF CONTENTS

Introduction ... 1
Reference Designs ... 1
Revision History ... 2
CN-0407 Ultrahigh Sensitivity Femtoamp Measurement Platform ... 3
CN-0399 Battery or USB Powered 9 kHz to 6 GHz RMS Power Measurement System ... 11
CN-0385 Isolated, Multichannel Data Acquisition System with PGIA for Single-Ended and Differential Industrial Level Signals ... 18
CN-0191 20-Bit, Linear, Low Noise, Precision, Bipolar ±10 V DC Voltage Source ... 31
DC2591A Demo Manual: Easy SMU Arduino Shield ... 35
DC2132A Demo Manual: Constant Current Bench Supply ... 51
CN-0387 Calibration-Free Return Loss Measurement System ... 61
CN-0375 Broadband Low Distortion Transmitter for 3G, 4G, and LTE ... 70
CN-0374 RF-to-Bits Solution Offers Precise Phase and Magnitude Data to 6 GHz ... 80
CN-0369 Translation Phase-Locked Loop Synthesizer with Low Phase Noise ... 87

REVISION HISTORY

3/2019—Revision 0: Initial Version

ANALOG DEVICES

Circuit Note
CN-0407

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0407.

Devices Connected/Referenced	
ADA4530-1	Femtoampere Input Bias Current Electrometer Amplifier
AD7172-2	Low Power, 24-Bit, 31.25 kSPS, Sigma-Delta ADC with True Rail-to-Rail Buffers
ADR4525	Ultralow Noise, High Accuracy, Voltage Reference
ADP2442	36 V, 1 A, Synchronous, Step-Down, DC-to-DC Regulator with External Clock Synchronization
ADG1419	2.1 Ω On Resistance, ±15 V/+12 V/±5 V, *i*CMOS SPDT Switch
ADP7118	20 V, 200 mA, Low Noise, CMOS LDO Linear Regulator
ADP7182	−28 V, −200 mA, Low Noise, Linear Regulator
ADuM3151	3.75 kV, 7-Channel, SPIsolator Digital Isolators for SPI

Ultrahigh Sensitivity Femtoampere Measurement Platform

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

- **CN-0407 Circuit Evaluation Board (EVAL-CN0407-SDPZ), Consists of Two Boards**
  - **Low Leakage Mezzanine Board (EVAL-CN0407-1-SDPZ)**
  - **Data Acquisition Board (EVAL-CN0407-2-SDPZ)**
- **System Demonstration Platform (EVAL-SDP-CS1Z)**

Design and Integration Files

- **Schematics, Layout Files, Bill of Materials**

CIRCUIT FUNCTION AND BENEFITS

The system functional diagram in Figure 1 is a precision analog front end for measurement of current down to the femtoampere range. This industry-leading solution is ideal for chemical analyzers and laboratory grade instrument where an ultrahigh sensitivity analog front end is required for signal conditioning current output sensors such as photodiodes, photomultiplier tubes, and Faraday cups. Applications that can use this solution include mass spectrometry, chromatography, and coulometry.

The EVAL-CN0407-SDPZ provides a reference design for real-world application by partitioning the system into a low leakage mezzanine board and a data acquisition board. The input signal conditioning is implemented with the ADA4530-1 on the mezzanine board. The ADA4530-1 is an electrometer-grade amplifier with ultralow input bias current of 20 fA maximum at 85°C. A guard buffer is integrated on the chip to isolate the input pins from leakage to the printed circuit board (PCB). The default amplifier configuration is in the transimpedance mode with a 10 GΩ glass resistor and a metal shield that prevents leakage current from entering any of the high impedance paths on the board. In addition, the mezzanine board includes unpopulated resistor and capacitor pads to allow prototyping with surface-mount feedback resistors as well as other input configurations.

The data acquisition board uses an AD7172-2 24-bit Σ-Δ analog-to-digital-converter (ADC) and is powered from a single 9 V dc supply. The on-board supply generates all necessary voltages required to power both boards. The board connects to a PC via the SDP-S board (EVAL-SDP-CS1Z) and uses digital isolation to prevent noise from the USB bus or ground loops from degrading low current measurements.

Rev. A

Circuits from the Lab reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113
©2017–2019 Analog Devices, Inc. All rights reserved.

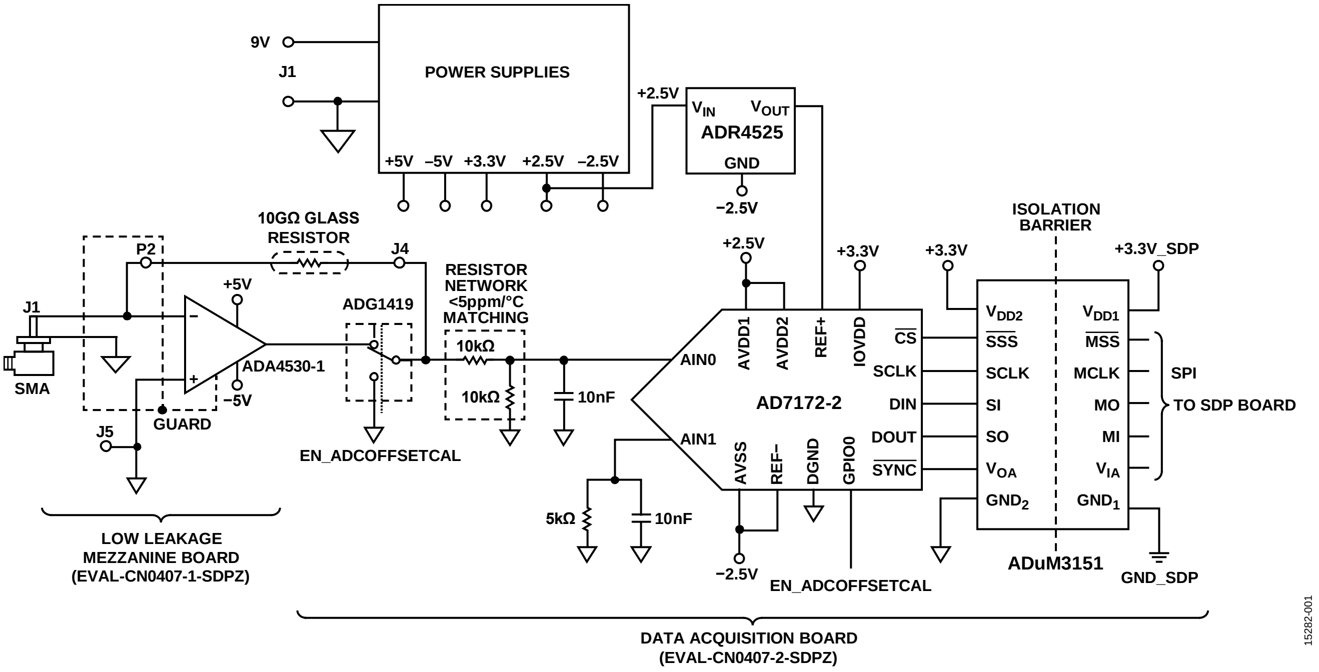

9V
J1
POWER SUPPLIES
+5V −5V +3.3V +2.5V −2.5V
+2.5V
V_{IN} V_{OUT}
ADR4525
GND
−2.5V
10GΩ GLASS RESISTOR
P2
J4
J1
SMA
+5V
ADA4530-1
−5V
J5
GUARD
ADG1419
RESISTOR NETWORK <5ppm/°C MATCHING
10kΩ
10kΩ
10nF
EN_ADCOFFSETCAL
+2.5V
+3.3V
AIN0
AIN1
AVDD1
AVDD2
REF+
IOVDD
CS
SCLK
DIN
DOUT
SYNC
AD7172-2
AVSS
REF−
DGND
GPIO0
5kΩ
10nF
−2.5V
EN_ADCOFFSETCAL
+3.3V
ISOLATION BARRIER
+3.3V_SDP
V_{DD2}
SSS
SCLK
SI
SO
V_{OA}
GND_2
V_{DD1}
MSS
MCLK
MO
MI
V_{IA}
GND_1
SPI
TO SDP BOARD
ADuM3151
GND_SDP
LOW LEAKAGE MEZZANINE BOARD (EVAL-CN0407-1-SDPZ)
DATA ACQUISITION BOARD (EVAL-CN0407-2-SDPZ)
15282-001

Figure 1. Femtoampere Measurement System Functional Diagram (All Connections and Decoupling Not Shown)

CIRCUIT DESCRIPTION

Low Leakage Mezzanine Board (EVAL-CN0407-1-SDPZ)

The mezzanine board (EVAL-CN0407-1-SDPZ) is built on a hybrid FR-4 and Rogers 4350B laminate for the lowest possible current leakage. The outer two layers are ceramic (Rogers 4350B), and the inner layer is a standard glass epoxy laminate (FR-4). The Rogers 4350B material provides superior insulation resistance in the presence of humidity when compared to glass or epoxy materials. It also minimizes current leakage and has much shorter dielectric relaxation times than glass or epoxy dielectrics. For more information on dielectric relaxation, see the ADA4530-1 data sheet.

Figure 2 shows the board layers stackup. All of the sensitive traces are on the top layer, surrounded by guard traces, vias, and planes.

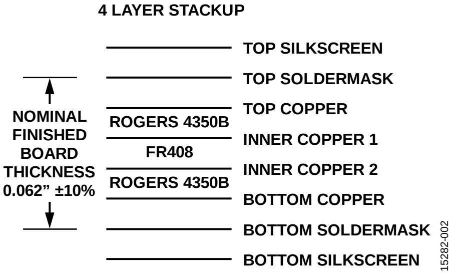

4 LAYER STACKUP
TOP SILKSCREEN
TOP SOLDERMASK
TOP COPPER
INNER COPPER 1
INNER COPPER 2
BOTTOM COPPER
BOTTOM SOLDERMASK
BOTTOM SILKSCREEN
ROGERS 4350B
FR408
ROGERS 4350B
NOMINAL FINISHED BOARD THICKNESS 0.062" ±10%
15282-002

Figure 2. Mezzanine Board Layers Stackup

Transimpedance Amplifier with Glass Resistor

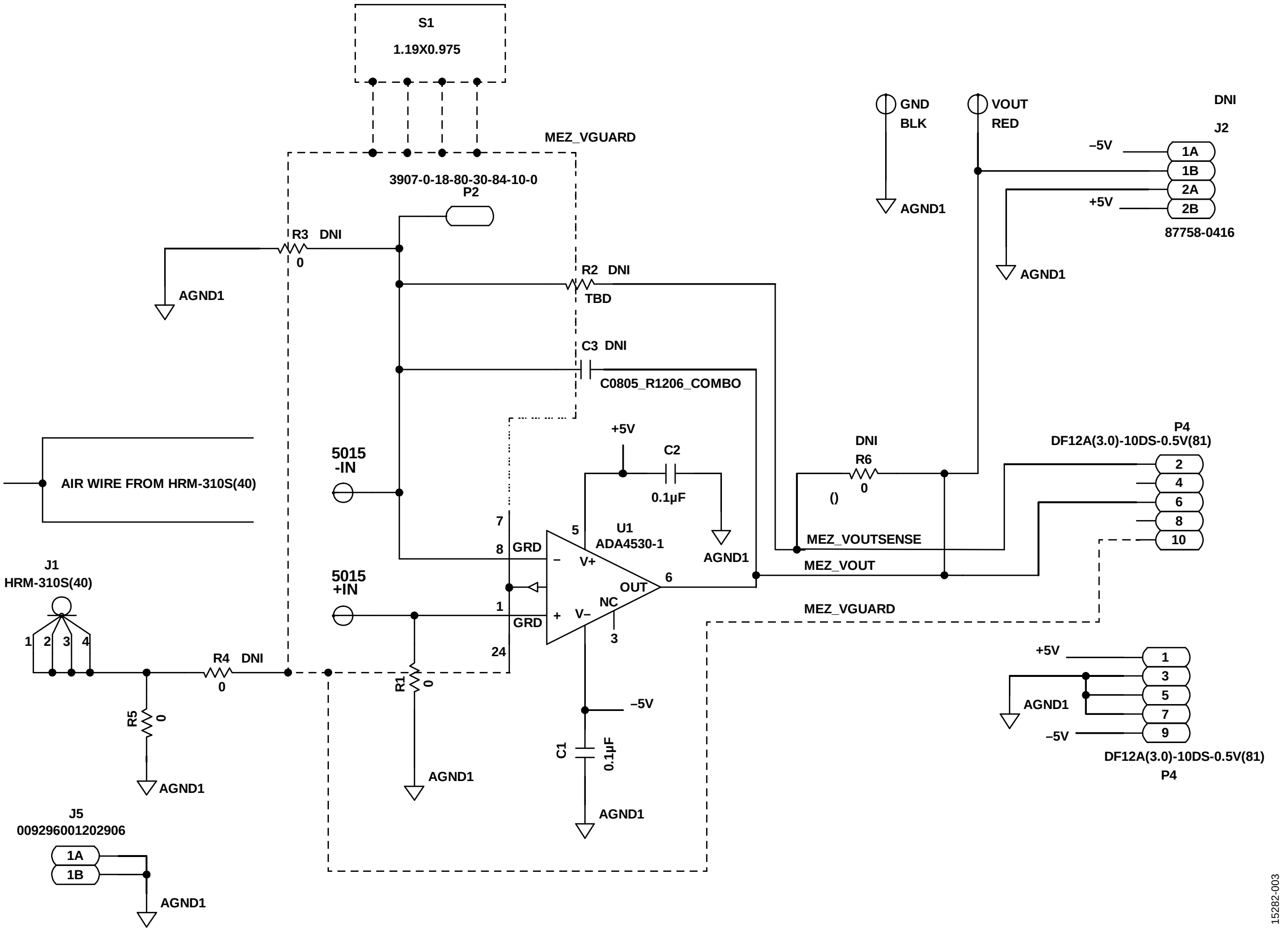

S1
1.19X0.975
MEZ_VGUARD
3907-0-18-80-30-84-10-0
P2
R3 DNI
0
AGND1
R2 DNI
TBD
C3 DNI
C0805_R1206_COMBO
AIR WIRE FROM HRM-310S(40)
5015
-IN
5015
+IN
J1
HRM-310S(40)
1 2 3 4
R4 DNI
0
R5
0
AGND1
J5
009296001202906
1A
1B
AGND1
R1
0
AGND1
+5V
C2
0.1µF
AGND1
U1
ADA4530-1
7
8
GRD
5
V+
OUT
6
NC
1
GRD
V–
3
24
–5V
C1
0.1µF
AGND1
GND
BLK
AGND1
VOUT
RED
DNI
J2
–5V
+5V
1A
1B
2A
2B
87758-0416
AGND1
DNI
R6
0
()
P4
DF12A(3.0)-10DS-0.5V(81)
2
4
6
8
10
MEZ_VOUTSENSE
MEZ_VOUT
MEZ_VGUARD
+5V
AGND1
–5V
1
3
5
7
9
DF12A(3.0)-10DS-0.5V(81)
P4
15282-003

Figure 3. Low Leakage Mezzanine Board (EVAL-CN0407-1-SDPZ) Detailed Schematic

Figure 3 shows the detailed mezzanine board schematic, where the ADA4530-1 is configured as a transimpedance amplifier (TIA) with a 10 GΩ glass resistor by default. In this configuration, a solid wire is soldered from the center pin of the SMA connector to the −IN pad. The SMA input connector includes a polytetrafluoroethylene (PTFE) dielectric between the center pin and the outer shield. The connector is mounted on the bottom of the mezzanine board, and the PTFE core and the center pin protrude through the top side. Because the connection is air wired through the protruding center pin to a pad on the top side of the board, all of the critical high impedance traces are on the top side of the board only. The need for a shield on the bottom side of the board is therefore eliminated. A metal shield on the top side is included to prevent electrostatic interference.

By default, the components on the mezzanine board are configured and preassembled as shown in Table 1.

Table 1. Default Setting for TIA with Glass Resistor

Component	Value
R1	0 Ω
R2, R3, R4, R6	Open
R5	0 Ω
Feedback Resistor	A 10 GΩ glass resistor is placed on the Teflon supports of the main board. One of its leads (the high impedance lead) is plugged into the single pin socket, P2, on the mezzanine board, and the other is soldered to J4 on the data acquisition board (this is a low impedance node).

With a 10 GΩ feedback resistor and an output voltage range of 4.96 V, the corresponding input current range is ±496 pA.

Transimpedance Amplifier Configuration with SMT Resistor

For applications that may not need the low leakage afforded by a glass resistor, R2 is a combined footprint that allows using an SMT resistor of 0805, 1206, 1210, or 2510 size. The transimpedance amplifier configuration is shown in Figure 4.

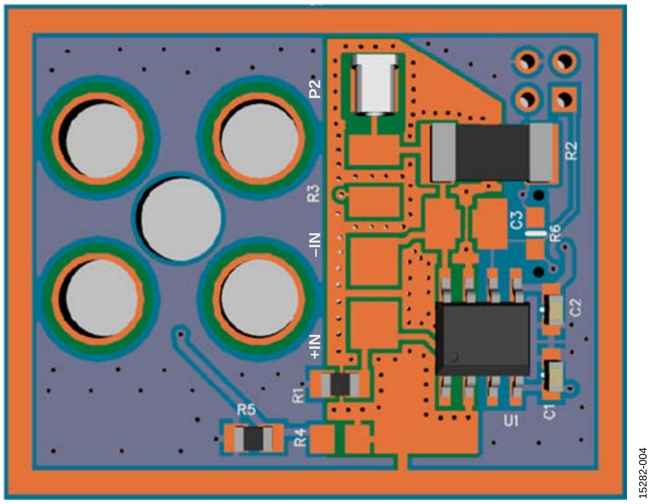


Figure 4. TIA Configuration with SMT Resistor

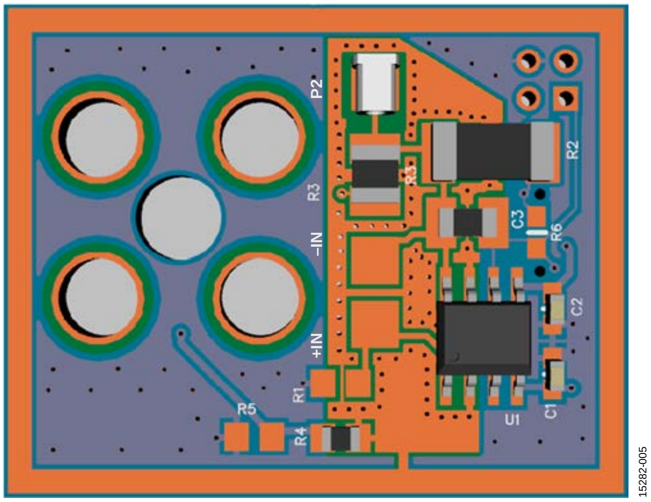


Figure 5. High Input Impedance Voltage Buffer Configuration

In this configuration, remove the glass resistor lead from P2 on the mezzanine board and use the desired resistor at R2 instead. In this configuration, a small metal shield (provided separately) that fits over just the mezzanine board results in a smaller profile, and the mezzanine board can be removed to be evaluated either individually or as part of an end system separate from the data acquisition board.

Buffer Configuration for High Impedance Voltage Output Sensors

The mezzanine board also includes pads to configure the amplifier as a buffer or noninverting amplifier for high impedance voltage output sensors. To configure the board for voltage conditioning, connect a solid wire from the center pin of the SMA connector to the +IN pad and use the settings in Table 2.

Table 2. Settings for Voltage Buffer Configuration

Component	Value
R1, R5, R6	Open
R2, R3	Values for desired gain
R4	0 Ω

With the settings in Table 2, the SMA shield is connected to the guard voltage. Use the poke-home connector, J5 (bottom side of mezzanine board), to connect a ground reference to the circuit.

When the board is configured in voltage buffer mode, as shown in Figure 5, the output is limited to approximately −4.96 V to +3.5 V because of the common-mode input voltage range of the ADA4530-1. If the amplifier is configured with closed-loop gains larger than 1, the input range must be limited to maintain the common-mode range of the amplifier inputs.

Data Acquisition Board (EVAL-CN0407-2-SDPZ)

The data acquisition board (EVAL-CN0407-2-SDPZ) contains power management, digital isolation, a 24-bit ADC, and a precision voltage reference. In addition to mating with the mezzanine board, this board also mates with the SDP-S board, which in turn connects to a PC via a USB connection. A detailed schematic and layout of the data acquisition board can be found in the CN-0407 Design Support Package at www.analog.com/CN0407-DesignSupport.

Power Management

Figure 6 shows a simplified diagram of the power management section that is located on the data acquisition board. A 9 V dc external power supply, connected to the J1 barrel connector, powers the mezzanine board, ADC, and digital isolation section. The input circuitry includes protection against overvoltage transients and against reverse voltage. Three ADP7118 low noise linear regulators generate 5 V for the ADA4530-1, 2.5 V for the analog front end of the AD7172-2 ADC, and 3.3 V for the digital input/output lines and the isolators. The SDP-S board provides power for the isolated section of the board.

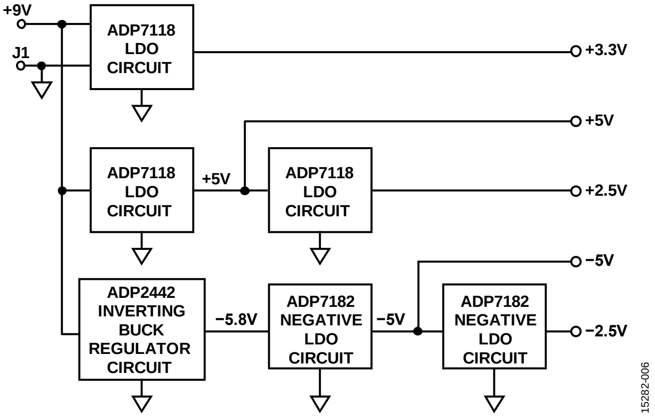


Figure 6. Simplified Block Diagram of Power Supply

An on-board LED provides an indication that power is on and the system is working correctly. Because some applications may use sensitive light sensors, the evaluation software includes an option to turn off DS1 while the board is acquiring data.

The inverting buck regulator built around the ADP2442 takes the dc input and generates approximately −5.8 V. The switching controller operates in fixed frequency mode (forced PWM), which results in lower efficiency (when compared with pulse-skipping mode) but maintains a constant switching frequency at close to 1 MHz, which makes it easy to filter out. Because the entire system consumes less than 5 mA from the negative supplies, the low power supply efficiency is not a concern.

The output of the inverting buck regulator supplies two ADP7182 negative linear regulators to provide −2.5 V for the AD7172-2 and −5 V for the ADA4530-1.

A detailed schematic and layout of the data acquisition board including the power management circuits, can be found in the CN-0407 Design Support Package at www.analog.com/CN0407-DesignSupport.

ADC and Reference

The output of the mezzanine board has an output voltage range of up to ±5 V, whereas the AD7172-2 ADC has an input range of ±2.5 V. A 10 kΩ/10 kΩ matched resistor divider attenuates the output of the mezzanine board by a factor of two. To minimize any offset errors due to the ADC, an ADG1419 single-pole/double-throw (SPDT) analog switch shorts the input of the resistor divider to ground and allows the software to measure the offset error due to the ADC and resistor divider. When offset cancellation is enabled, the software subtracts the measured offset from every reading. Any remaining offset is due only to the ADA4530-1 circuitry.

The GPIO0 digital line (EN_ADCOFFSETCAL) from the AD7172-2 controls the position of the ADG1419 switch. The software writes to register GP_DATA0, resulting in either a 0 or 1 output on GPIO0. The output is referenced to −2.5 V; therefore, the ground pin of the ADG1419 is connected to −2.5 V rather than ground.

The ADR4525 provides a low noise, high accuracy reference to the ADC. The ADC front end is powered from ±2.5 V; therefore, the ADR4525 GND pin is also tied to the −2.5 V supply. This connection develops the 2.5 V reference voltage between the REF+ and REF− pins of the AD7172-2.

Trigger In and Trigger Out

The EVAL-CN0407-SDPZ board includes trigger in and trigger out controls to simplify interfacing the board to external equipment. Both the trigger in and trigger out signals use standard TTL levels.

When trigger in is enabled through software, the system waits for a rising edge on trigger in before starting to acquire data. Similarly, when trigger out is enabled, the system outputs a rising edge when starting to acquire data.

Cleaning and Handling the Mezzanine Board

It is important to always handle the mezzanine boards by the edges and never touch the area within the SHIELD1 shield outline.

If any rework is done to components on the mezzanine board, the board must be properly cleaned to remove any contaminants, such as solder flux, saline moisture, dirt, and dust to maintain its low leakage performance. Any contaminants can severely degrade its femtoampere performance.

An effective cleaning procedure consists of the following steps:

1. Soak the board in an ultrasonic bath with cleanroom-grade isopropyl alcohol for 15 minutes. Ultrasonic cleaning uses ultrasound at a high frequency, creating cavitation in the cleaning solution. This process helps to remove contaminants on the surface of the board and in areas under soldered components that are hard to reach. The next cleaning steps require using fresh isopropyl alcohol.
2. Remove the board from the ultrasonic bath with a pair of forceps. Rinse and flush the board with isopropyl alcohol to remove any contaminant residue.
3. Flood the board with isopropyl alcohol and gently scrub it with an acid brush. Concentrate on areas between the U1 pins, J1, the guard rings, and the area within the shield outline.
4. Rinse and flush the board with isopropyl alcohol.
5. Use a final flush for the top and bottom of the board with isopropyl alcohol.
6. Use compressed dry air to dry the board. Blow air around the U1 pins, the input traces to J1, and the guard ring area. Be sure to direct the compressed air under J1 and U1 as well.
7. To make sure that the board is completely dry, bake the board in the oven at 125°C for 15 minutes.
8. After cleaning, remember to place the metal shield on the board. The metal shield helps prevent any contact to the guarded area.

COMMON VARIATIONS

For higher range of current measurement, use the AD8605/AD8606/AD8608 or AD8615/AD8616/AD8618. These amplifiers feature higher input bias current in the picoampere range in exchange for a wider bandwidth.

Other ADCs suitable for data acquisition include the 24-bit AD7175-2 and AD7124-4.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0407-SDPZ evaluation board and the SDP-S system demonstration platform (EVAL-SDP-CS1Z) evaluation board.

The evaluation software communicates with the SDP-S board to capture data from the EVAL-CN0407-SDPZ.

Equipment Needed

The following equipment is needed:

- PC with USB port and Windows® XP, Windows Vista (32-bit), or Windows 7 (32-bit)
- EVAL-CN0407-SDPZ evaluation board, includes low leakage mezzanine board (EVAL-CN0407-1- SDPZ) and data acquisition board (EVAL-CN0407-2-SDPZ)
- SDP-S board (EVAL-SDP-CS1Z)
- 9 V dc power supply or wall wart
- EVAL-CN0407-SDPZ evaluation software, available for download at ftp://ftp.analog.com/pub/cftl/CN0407/

In addition, a high quality coaxial cable assembly to connect the desired signal to the board is recommended.

Functional Block Diagram of Test Setup

Figure 7 shows a functional block diagram of the test setup.

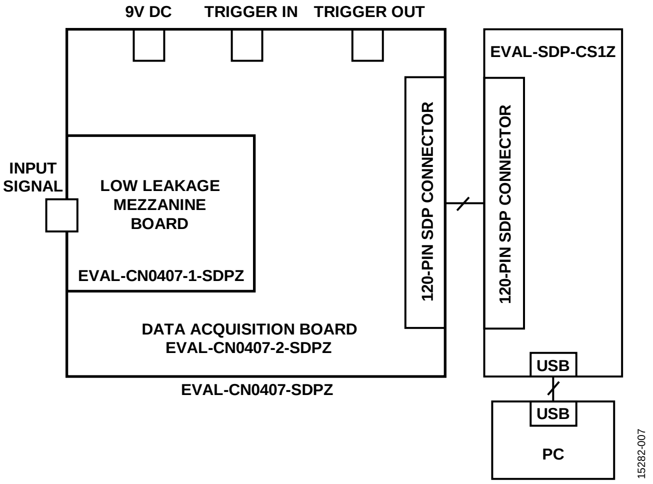

9V DC
TRIGGER IN
TRIGGER OUT
INPUT SIGNAL
LOW LEAKAGE MEZZANINE BOARD
EVAL-CN0407-1-SDPZ
120-PIN SDP CONNECTOR
DATA ACQUISITION BOARD
EVAL-CN0407-2-SDPZ
EVAL-CN0407-SDPZ
EVAL-SDP-CS1Z
120-PIN SDP CONNECTOR
USB
USB
PC
15282-007

Figure 7. Test Setup Functional Block Diagram

Getting Started

Download the evaluation software (available at ftp://ftp.analog.com/pub/cftl/CN0407/) and install it by running the **setup.exe** file.

Connect the EVAL-CN0407-SDPZ and SDP-S boards together, and connect the SDP-S board to the PC with a USB cable. Connect the 9 V dc power supply to the EVAL-CN0407-SDPZ board and load the user interface installer software, named **CN0407 Evaluation Software**, located under **Program Files**, **Analog Devices**. When USB communications are established, the SDP-S board can send, receive, and capture serial data from the EVAL-CN0407-SDPZ.

The SDP-S user guide (UG-291) contains additional information regarding the SDP-S board.

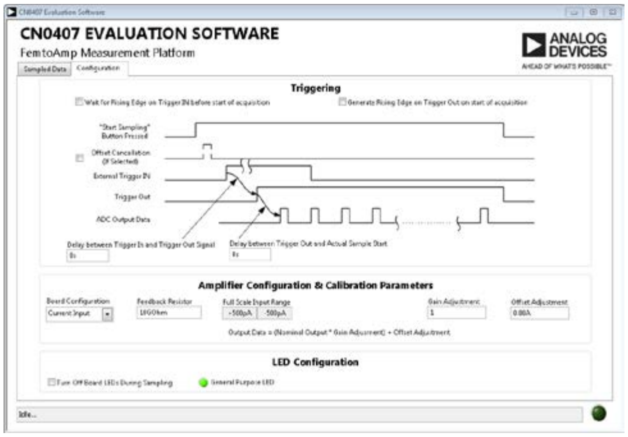
The AN-1373 application note provides more information regarding low current measurements.

Running the Evaluation Software

The evaluation software has a **Sampled Data** tab where time and frequency domain data are displayed, and a **Configuration** tab that allows setting parameters such as triggering, offset correction, board configuration, and manual calibration.

Configuration Tab

Figure 8 shows the **Configuration** tab. The **Triggering** section includes a graphical depiction of the trigger functionality. Select the desired check boxes to enable the trigger in or trigger out, and enter the desired delay between the trigger in signal, the trigger out signal, and when the ADC starts acquiring data. Select the **Offset Cancellation** box to measure and remove the offset error due to the ADC input offset and input bias current.


CN0407 Evaluation Software
CN0407 EVALUATION SOFTWARE
FemtoAmp Measurement Platform
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™
Sampled Data
Configuration
Triggering
"Start Sampling" Button Pressed
Offset Cancellation (If Selected)
External Trigger IN
Trigger Out
ADC Output Data
Amplifier Configuration & Calibration Parameters
LED Configuration
15282-008

☐ Wait for Rising Edge on Trigger IN before start of acquisition

☐ Generate Rising Edge on Trigger Out on start of acquisition

☐ Offset Cancellation (If Selected)

Delay between Trigger In and Trigger Out Signal: 0s

Delay between Trigger Out and Actual Sample Start: 0s

Board Configuration: Current Input

Feedback Resistor: 10GOhm

Full Scale Input Range: -500pA 500pA

Gain Adjustment: 1

Offset Adjustment: 0.00A

Output Data = (Nominal Output * Gain Adjustment) + Offset Adjustment

☐ Turn Off Board LEDs During Sampling

● General Purpose LED

Idle...

*Figure 8. **Configuration** Tab*

Set the **Board Configuration** (in the **Amplifier Configuration & Calibration Parameters** section) to match the configuration of the amplifier on the mezzanine board. Because the amplifier ships configured in transimpedance mode, the default setting is **Current Input**. In this mode, the feedback resistor control is visible to allow changing it to values different from the factory configuration. By default, it is set to 10 GΩ. The **Full Scale Input Range** value represents the full-scale input of the system, referred to the input, and it is calculated based on the value of the feedback resistor or the specified gain when configured as a voltage buffer.

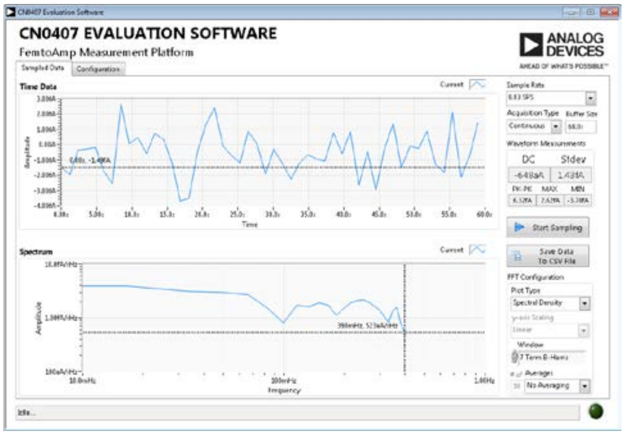
In addition to the offset compensation, the user can also apply manual system calibration by providing a gain and offset value. By default, **Offset Adjustment** is set to 0 and **Gain Adjustment** is set to 1.

The data presented in the evaluation software corresponds to the following equation:

Output Measurement =
(*Raw Reading* + *Offset Adjustment*) × *Gain Adjustment*

The **LED Configuration** section of the **Configuration** tab controls the LEDs on the board. Clicking **General Purpose LED** turns the corresponding LED, DS2 (refer to corresponding detailed schematic from the CN-0407 Design Support Package), on and off. Clicking **General Purpose LED** is a quick way to verify that the system is communicating with the evaluation software. In addition, **Turn off Board LEDs During Sampling** turns off the power (DS1) and general-purpose LED (DS2) while the ADC is acquiring data. When using a photodiode or other light sensors, turning off the LEDs on the board may improve the measurements.

Sampled Data Tab



Sample Rate: 0.83 SPS
Acquisition Type: Continuous
Plot Type: Spectral Density
Window: 7 Term B-Harris
No Averaging

Figure 9. **Sampled Data** Tab

The **Sample Rate** dropdown box selects the ADC output data rate between 0.83 SPS and 867.3 SPS.

After selecting the desired sampling rate, select the acquisition buffer size in seconds. This selection determines how much data is displayed on screen and retained in memory. Click **Start Sampling** to begin acquiring data from the board. For output data rates of 19.99 SPS and slower, the display is updated continuously as a rolling window. For output data rates greater than 19.99 SPS, the update rate of the chart is equal to the time duration of the acquisition window. The status bar at the bottom of the screen counts down the time remaining until the next update.

In **Continuous** acquisitions, the system continues to acquire data until the user clicks **Stop Sampling**. In **Single** acquisition, the system stops after reaching the specified **Buffer Size**.

Above the **Start Sampling** button, indicators display time domain information such as the dc value of the signal and the standard deviation. When measuring a dc input, the standard deviation is equal to the rms noise of the signal.

The lower section of the **Sampled Data** tab displays the frequency domain data from the system. The controls on the right configure the frequency domain chart as either power spectrum or power spectral density. The user can also configure the type of window, enable averaging, and configure the number of averages to perform. When displaying the power spectrum plot, use the Y-axis scaling control to set the Y-axis units to either dB of full scale or linear units (volts or amps, depending on the board configuration).

Click **Save Data To CSV File** to save the current time and frequency domain charts to two comma separated files.

Testing the System

Connect the external power supply and launch the evaluation software. The software is able to communicate with the EVAL-CN0407-SDPZ if the Analog Devices system development platform driver appears in Windows **Device Manager**. When USB communications are established, the SDP-S board can send, receive, and capture serial data from the EVAL-CN0407-SDPZ.

To measure system noise, make sure the shield is installed on the board, and do not connect anything to the input SMA connector. For best performance, place the entire assembly inside a metal box, which is electrically connected to ground.

In the **Configuration** tab, check the **Offset Cancellation** box, and make sure that the system is configured as **Current Input** with a 10 GΩ resistor. In the **Sampled Data** tab, select the desired sampling rate from the dropdown box and click **Start Sampling**. Thermal noise from the 10 GΩ resistor can dominate system noise; therefore, for best performance, select the lowest acceptable sampling rate. For example, Figure 10 shows the system noise when sampling at 0.83 SPS for 120 minutes. The resulting rms noise is 1.4 fA with a dc value of −150 aA.

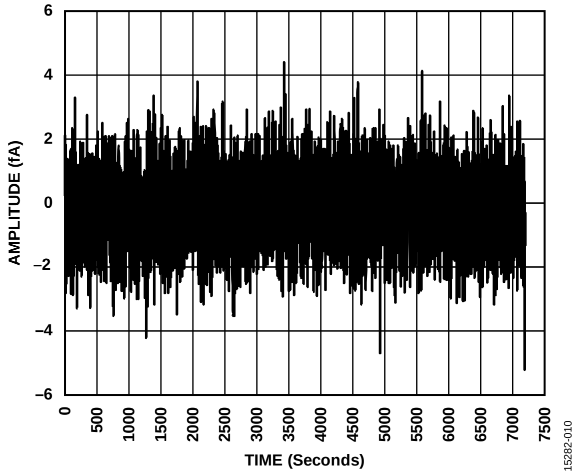


Figure 10. Sampled Data with an Open Input at 0.83 SPS

Figure 11 and Figure 12 show photographs of the EVAL-CN0407-SDPZ, including the low leakage mezzanine board and the data acquisition board.

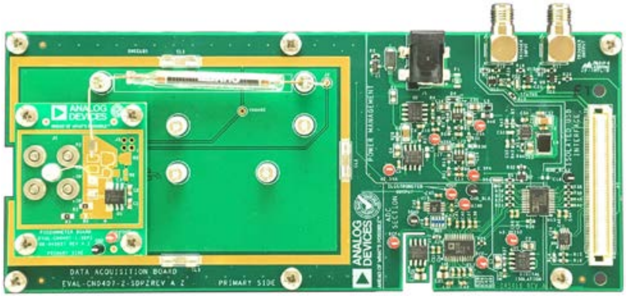


Figure 11. EVAL-CN0407-SDPZ (Without Shield Installed)

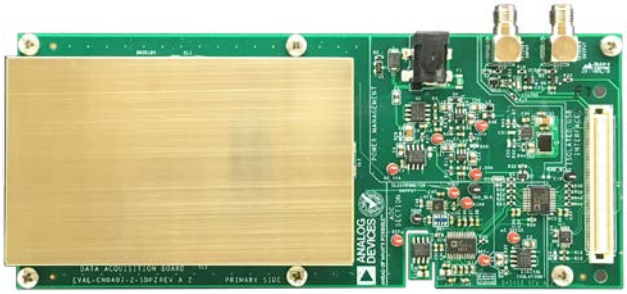


Figure 12. EVAL-CN0407-SDPZ Photograph (with Shield Installed)

LEARN MORE

CN-0407 Design Support Package:
www.analog.com/CN0407-DesignSupport

AN-1373 Application Note. *ADA4530-1 Femtoampere Level Input Bias Current Measurement.* Analog Devices.

ADA4530-1R-EBZ User Guide (UG-865). *ADA4530-1 8 Lead SOIC Package Evaluation Board.* Analog Devices.

MT-035 Tutorial. *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues.* Analog Devices.

MT-101 Tutorial. *Decoupling Techniques.* Analog Devices.

Data Sheets and Evaluation Boards

ADA4530-1 Data Sheet

AD7172-2 Data Sheet

ADR4525 Data Sheet

ADP2442 Data Sheet

ADG1419 Data Sheet

ADP7118 Data Sheet

ADP7182 Data Sheet

ADuM3151 Data Sheet

REVISION HISTORY

2/2019—Rev. 0 to Rev. A

Changes to Figure 3 3

4/2017—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab reference designs are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab reference designs in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab reference designs are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab reference designs at any time without notice but is under no obligation to do so.

©2017–2019 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
CN15282-0-2/19(A)

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0399.

Devices Connected/Referenced	
ADL5904	DC to 6 GHz, 45 dB TruPwr™ Detector with Envelope Threshold Detection
AD7091R	1 MSPS, Ultralow Power, 12-Bit ADC in 10-Lead LFCSP and MSOP
ADP160	Ultralow Quiescent Current, 150 mA, CMOS Linear Regulator

Battery or USB Powered 9 kHz to 6 GHz RMS Power Measurement System

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

- **CN-0399 Circuit Evaluation Board (EVAL-CN0399-SDPZ)**
- **System Demonstration Platform (EVAL-SDP-CS1Z)**

Design and Integration Files

- **Schematics, Layout Files, Bill of Materials**

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is an RF power measurement circuit that accurately measures the power from an RF signal source within a frequency range of 9 kHz to 6 GHz, and has a nominal input power range of 45 dBm (–30 dBm to +15 dBm).

This circuit constitutes a complete rms RF power meter in a tiny form factor that can be powered entirely from a 5 V USB power supply. The measurement signal chain consists of an rms responding RF power detector and a 12-bit, precision analog-to-digital converter (ADC). These devices are powered by a CMOS linear regulator which generates 3.3 V from the 5 V USB supply.

A simple calibration routine can be performed at multiple frequencies to compensate for any frequency response variation of the circuit. Calibration data is stored in a lookup table, which is referenced during the RF power measurement.

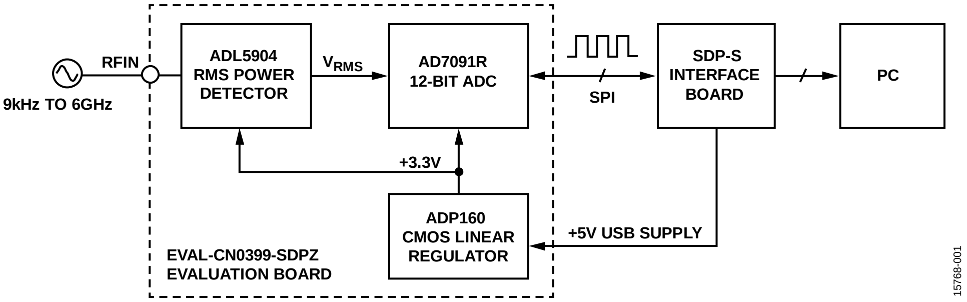


Figure 1. Portable RF Power Meter Evaluation Board Measurement Setup (All Connections and Decoupling Not Shown)

Rev. 0

Circuits from the Lab reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
©2017 Analog Devices, Inc. All rights reserved.

CIRCUIT DESCRIPTION

An RF signal ranging from 9 kHz to 6 GHz is applied to the SMA measurement head of the circuit. This signal drives the RFIN input pin of the ADL5904, an rms responding RF power detector, through an ac coupling capacitor. The size of this capacitor (0.47 µF) sets the minimum input frequency of the circuit. The output voltage from the detector (V_{RMS}) is a dc output voltage level that is proportional to the rms level of the input signal.

The output of the detector directly drives the input of the AD7091R 12-bit ADC. The ADC samples the input periodically and converts the voltage to a digitized voltage code. Each code is transferred to a PC via 3-wire serial peripheral interface (SPI), which uses an equation to calculate the RF power of the input signal. Calibration coefficient information is stored in a look-up table on the PC. The coefficient slope and intercepts are selected based on the frequency of operation, which must be known to accurately calculate the RF input power level.

RF Power Detector

The ADL5904 is a broadband rms responding RF power detector operating from dc to 6 GHz. A functional block diagram of the ADL5904 is shown in Figure 2.

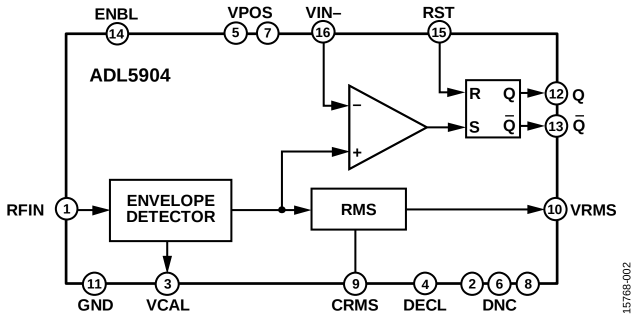


Figure 2. ADL5904 Block Diagram

The detector has a dynamic range of 45 dB, ranging from −30 dBm to +15 dBm with a linear-in-dB output characteristic. The low current consumption of 3 mA, makes the ADL5904 a suitable detector for this application circuit where the circuit is powered entirely from the 5 V USB interface from a PC.

An additional function provided by this detector is programmable envelope threshold detection. Threshold detection uses an internal comparator to compare the input envelope voltage with a predefined user input voltage. If the envelope voltage exceeds this predefined voltage, a digital output signal is asserted high. The output signal is latched high through an R/S flip-flop until the reset pin (RST) on the detector is pulsed high. This functionality is not used in the circuit shown in Figure 1.

Analog-to-Digital Converter

The AD7091R shown in Figure 3 is a 12-bit, single-channel successive approximation register (SAR) ADC. It has an ultralow power consumption of 1 mW in normal operation.

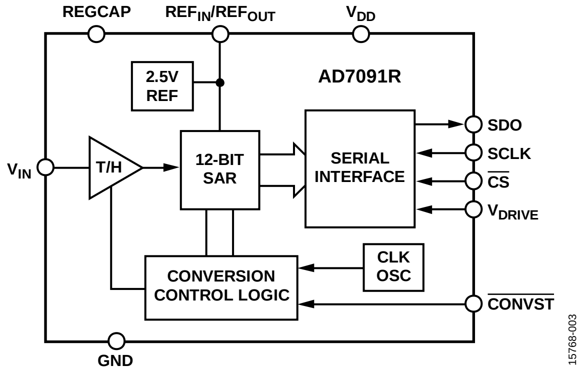


Figure 3. AD7091R Analog-to-Digital Converter

The REF_{IN}/REF_{OUT} pin of the ADC can be overdriven with an external reference voltage. However, in this application, accuracy is not compromised by using the internal 2.5 V reference. Using the 2.5 V internal reference means that the LSB size is

$$LSB = (2.5\ V)/2^{12} = 610\ \mu V$$

This means that the ADC has a resolution of 610 µV. The input voltage, V_{IN}, to the ADC can range from 0 V to 2.5 V (V_{REF}). Because the maximum output voltage of the detector is approximately 1.8 V, voltage scaling at the input of the ADC is not necessary, allowing the detector output to be connected directly to the ADC input.

On-Board Regulator

The ADP160 is a CMOS linear regulator, which can provide a stable output voltage from 2.2 V to 5.5 V with an ultralow output current quiescent current of 42 µA.

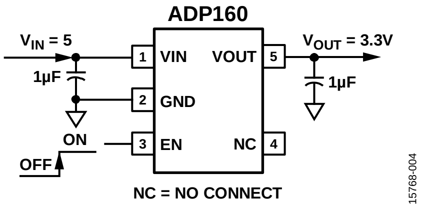


Figure 4. ADP160-3.3 Linear CMOS Regulator

The ADP160 is available in fixed or adjustable configurations. The 3.3 V fixed model used in this design provides a stable output to supply the power detector and ADC, with minimal external circuitry required, as shown in Figure 4.

Power Calculation

The equation used to calculate the power of the RF input signal as a power ratio in decibels (dBm) from the output of the detector is written as follows:

$$P_{IN}\ (\text{dBm}) = (V_{RMS}/m) + Int \tag{1}$$

where:
V_{RMS} is the output voltage of the detector as shown in Figure 5.
m is the slope of the power detector.
Int is the x-axis intercept of the power detector.

Using Equation 1, the overall system transfer function becomes

$$P_{IN}\ (\text{dBm}) = (CODE_{RMS}/m') + Int' \tag{2}$$

where:
$CODE_{RMS}$ is the digitized code representation of V_{RMS} from the ADC, as shown in Figure 5.
m′ is the slope of the combined power detector and ADC.
Int′ is x-axis intercept of the combined power detector and ADC.

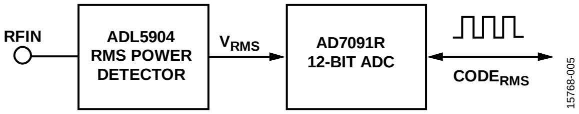


Figure 5. Detector and ADC Outputs

The slope and intercept within the equation are both frequency dependent parameters. As a result, calibration must be performed across frequency, that is, at enough frequency increments to ensure good system flatness across frequency.

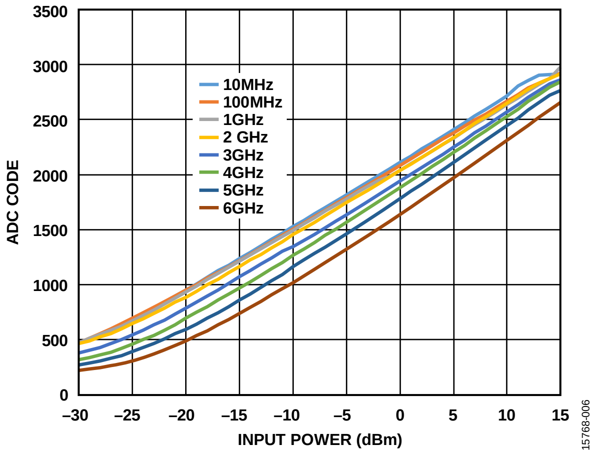
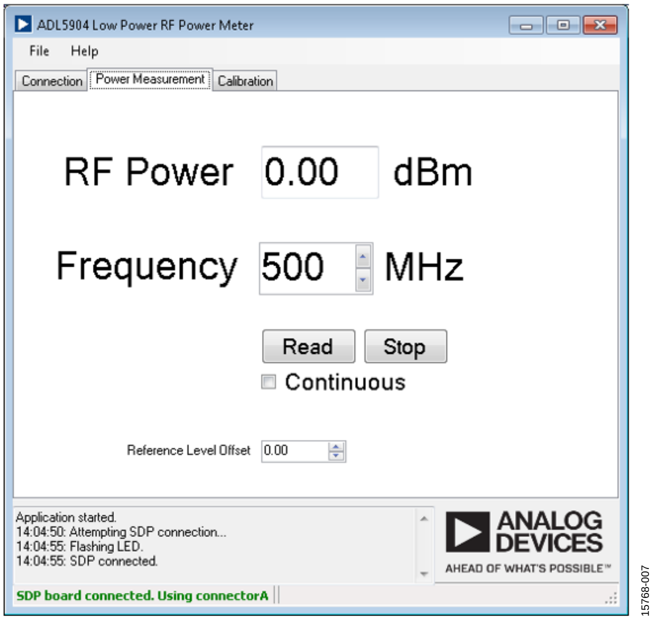


Figure 6. ADC Code vs. Input Power Transfer Function at 10 MHz

Figure 6 shows a plot of the raw measured ADC code versus input power to the detector. Multiple operating frequencies were plotted within the range of the power detector. These measured ADC codes correspond to the sampled and converted output voltage of the power detector. Each plot shown in Figure 6 shows how the characteristic curve of the detector varies linearly with decibel input power, within the operating range of the detector (–30 dBm to +15 dBm). This response is known as a linear-in-dB power detector response.

Software Interface

A simple software graphical user interface (GUI) is used to calculate and display the RF power being measured. Figure 7 shows the front panel of the GUI.



RF Power 0.00 dBm

Frequency 500 MHz

☐ Continuous

Reference Level Offset 0.00

Application started.
14:04:50: Attempting SDP connection...
14:04:55: Flashing LED.
14:04:55: SDP connected.

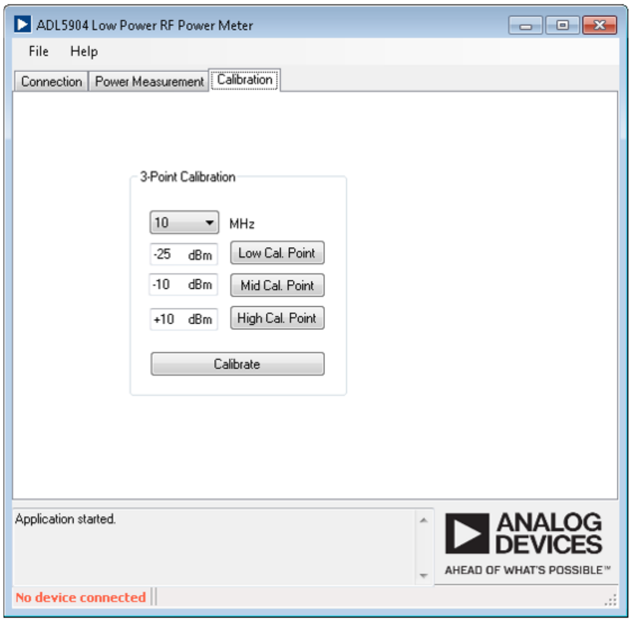
SDP board connected. Using connectorA

Figure 7. Software GUI Front Panel

In the **Power Measurement** tab, the frequency of the input signal must be entered prior to measurement, thereby telling the software which set of calibration coefficients (slope and intercept) to use. The software uses the calibration coefficients that are closest in frequency to the input frequency. Selecting **Continuous** and clicking **Read** periodically updates the measured power. A user defined reference level offset can be applied to the measurement to account for external cabling or coupling losses. This offset is added to the measured value, which is then displayed as the power.

Calibration Routine

Before performing a power measurement, the user must perform a calibration routine across frequency.


ADL5904 Low Power RF Power Meter
File
Help
Connection
Power Measurement
Calibration
3-Point Calibration
Low Cal. Point
Mid Cal. Point
High Cal. Point
Calibrate
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™
15768-008

10 MHz

-25 dBm

-10 dBm

+10 dBm

Application started.

No device connected

Figure 8. Calibration Routine Tab

Figure 8 shows the **Calibration** tab. A frequency is selected using the numeric selection box. Three power levels are then applied at that frequency. This 3-point calibration routine calculates two different slope and intercept values for the calibration frequency. These values are stored in the look-up table and used for power calculation. Figure 9 shows an example of calibration data for a selected frequency.

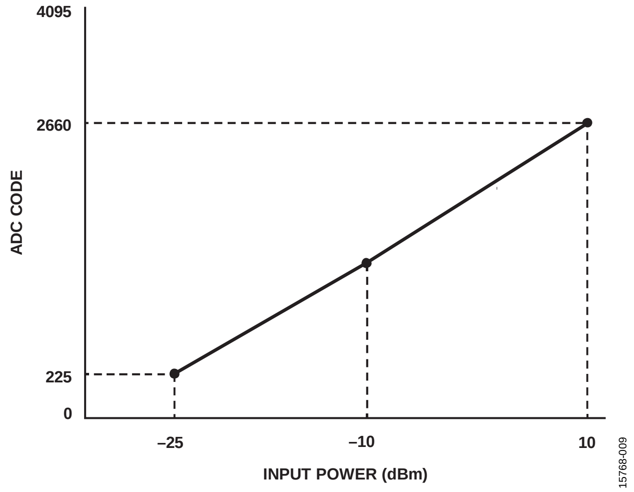


Figure 9. 3-Point Calibration Data Example

Each of the calibration points have a corresponding measured ADC code, as shown in Figure 9. These codes are used to calculate a slope and intercept value for each of the two regions between the calibration power levels. Calibration values stored for each calibrated frequency contain a slope and intercept for these two power regions, as shown in the look-up table outline in Figure 10.

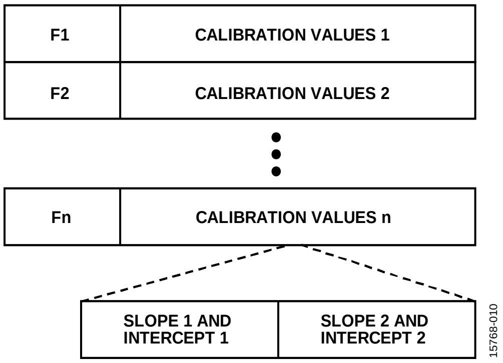

F1
CALIBRATION VALUES 1
F2
CALIBRATION VALUES 2
Fn
CALIBRATION VALUES n
SLOPE 1 AND INTERCEPT 1
SLOPE 2 AND INTERCEPT 2
15768-010

Figure 10 Look-up Table Outline

Measurement Sequence

Figure 11 shows the measurement sequence executed during power measurement.

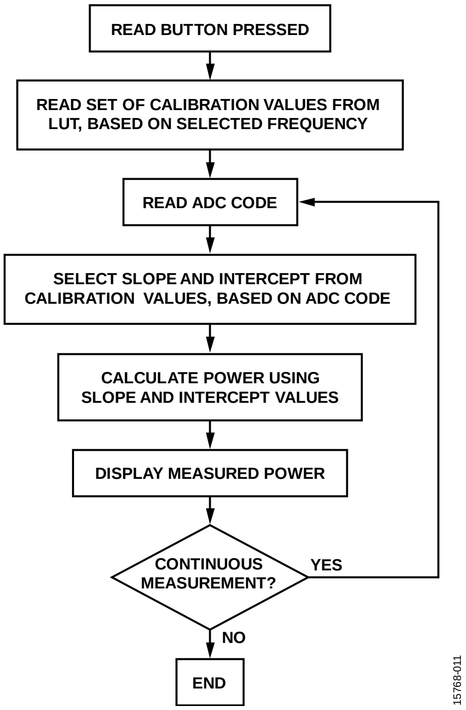

READ BUTTON PRESSED
READ SET OF CALIBRATION VALUES FROM LUT, BASED ON SELECTED FREQUENCY
READ ADC CODE
SELECT SLOPE AND INTERCEPT FROM CALIBRATION VALUES, BASED ON ADC CODE
CALCULATE POWER USING SLOPE AND INTERCEPT VALUES
DISPLAY MEASURED POWER
CONTINUOUS MEASUREMENT?
YES
NO
END
15768-011

Figure 11. Measurement Sequence

When the user clicks **Read**, the set of calibration values for the calibration frequency closest to the selected operating frequency are read from the look-up table.

These calibration values contain slope and intercepts for the two power regions of the 3-point calibration routine. The raw ADC code is then read through the SPI interface. This code is used for the power calculation. The slope and intercept from one of the two power regions are extracted from the calibration values for the selected frequency, based on the raw ADC code read.

With these slope and intercept values, power is then calculated using Equation 1 and displayed in the GUI. If the **Continuous** checkbox is selected, the measurement is repeated periodically for the selected frequency.

Measurement Timing

The timing of each measurement is shown in Figure 12. The ADC is sampled after the convert start (CONSTB) input is asserted low using a GPIO on the SDP-S interface board. After approximately 1 ms, the resultant ADC code value corresponding to the sampled voltage is transferred over the SPI. After calculating power, the GUI display is updated with the current power measurement. The measured power is displayed on the GUI for 1 sec. If measuring continuously, the measurement is repeated.

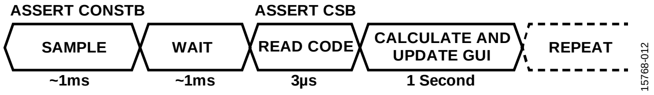


Figure 12. Measurement Timing

A complete set of documentation for the EVAL-CN0399-SDPZ board including schematics, layout files, and bill of materials can be downloaded from www.analog.com/CN0399-DesignSupport.

Test Results

After performing the calibration routine at different frequencies, measurement data was manually gathered over the entire power range of the detector to verify that the detector circuit was measuring power accurately.

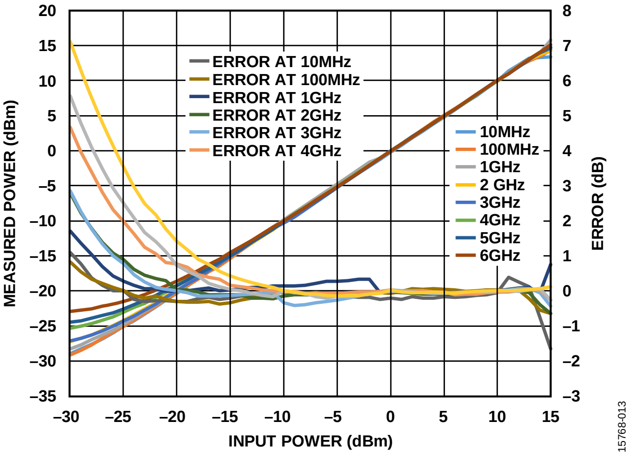


Figure 13. Input Power vs. Measured Power Data

As shown in the results in Figure 13, the circuit tracks the input power accurately from 10 MHz to 6 GHz. Over this frequency range, the maximum deviation from the actual input power was determined to be 0.57 dB at 5 GHz.

COMMON VARIATIONS

At low input power levels (below −20 dBm), the nonlinearity of the transfer function of the ADL5904 increases, suggesting that calibration points can be placed in this region. Note that there is no requirement or benefit in spacing the calibration power levels at even intervals.

If USB power was not available from the port of the PC, as an alternative, a 3.3 V supply can be provided externally to the circuit via the VPOS and GND test points. If an external supply is used, R15 is removed to isolate the on-board regulator output.

Instead of using the internal 2.5 V reference, an external reference source can be supplied to the V_{REF} pin of the ADC to increase the reference voltage or to provide a more stable reference.

An alternative method of reading from the ADC is to use the serial port (SPORT) interface protocol. Using SPORT requires that the larger SDP-B interface board (EVAL-SDP-CB1Z) be used. Custom software must also be programmed for use with the SPORT interface. This option is useful for applications that require faster throughput rate, because using the SDP-B interface board provides up to 1 MSPS throughput.

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is needed to perform the evaluations described in this circuit note:

- EVAL-CN0399-SDPZ evaluation board
- SDP-S board (EVAL-SDP-CS1Z)
- Signal generator (with output frequency within the range of dc to 6 GHz)
- CN-0399 Evaluation Software, which can be downloaded from ftp://ftp.analog.com/pub/cftl/CN0399/
- PC running Windows® 7 connected to the SDP-S board via a USB cable (supplied with the EVAL-SDP-CS1Z)

Setup and Test

To set up and test the EVAL-CN0399-SDPZ board, connect the SDP-S board to the EVAL-CN0399-SDPZ board and connect the USB cable from the PC to the SDP-S board.

1. Turn on the signal generator and ensure that the RF output signal is off.
2. Directly connect the RF output of the signal generator to the input of the RF power meter board.
3. Open the evaluation software, **ADL5904 Low Power RF Power Meter.exe**, and click **Connect**.
4. Click the **Calibration** tab in the software window, and begin the calibration routine by setting the signal generator frequency to 1 GHz, and setting the power level to −20 dBm.
5. Turn on the RF output of the signal generator, then click **Low Cal. Point** in the software window. A dialog box appears indicating that the calibration code has been stored for that power level.
6. Repeat Step 4 and Step 5 for each of the calibration points at 1 GHz, adjusting the power level of the signal generator each time.
7. Click **Calibrate** to calculate the slope and intercept values for 1 GHz. This operation stores the values in a look-up table in the software folder.
8. On the signal generator, adjust the power level to −10 dBm output.
9. In the software window, click the **Power Measurement** tab.
10. Select the **Continuous** checkbox and click **Read**.
11. The **RF Power** display box reads −10 dBm at 1 GHz.
12. Increase the power level in 1 dB steps from −10 dBm to +15 dBm. In the software window, the power level is read up to +15 dBm.
13. To halt measurement, click **Stop**.

Functional Block Diagram of Test Setup

Figure 14 shows the functional block diagram of the test setup.

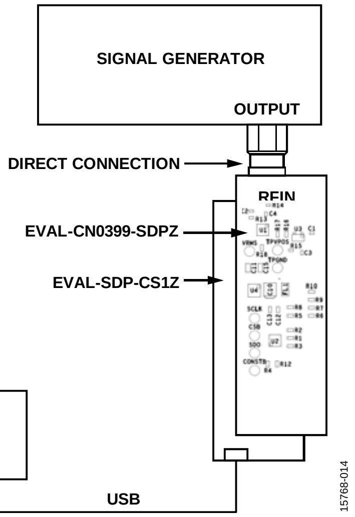


Figure 14. Functional Block Diagram of Test Setup

A photograph of the top of the EVAL-CN0399-SDPZ board is shown in Figure 15. The bottom view in Figure 16 shows the EVAL-SDP-CS1Z board connected to the EVAL-CN0399-SDPZ board.

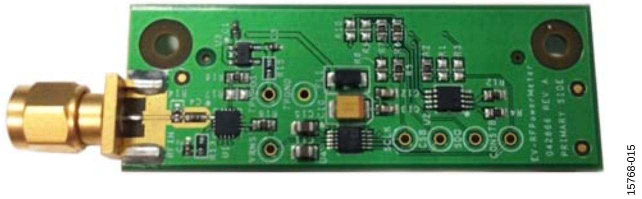


Figure 15. Top View Showing EVAL-CN0399-SDPZ Board

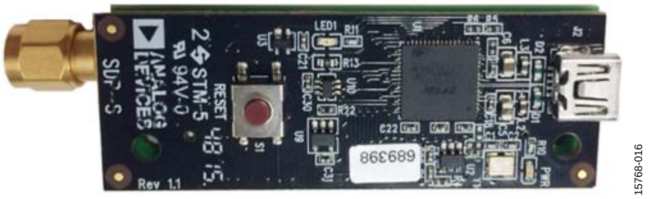


Figure 16. Bottom View Showing SDP-S Board Connected to EVAL-CN0399-SDPZ Board

LEARN MORE

CN-0399 Design Support Package: www.analog.com/CN0399-DesignSupport

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, *Analog Dialogue* 39-09, September 2005.

EVAL-AD7091RSDZ Evaluation Board User Guide (UG-409). Analog Devices.

ADIsimRF Design Tool.

CN-0178 Circuit Note, *Software-Calibrated, 50 MHz to 9 GHz, RF Power Measurement System*, Analog Devices.

CN-0366 Circuit Note, *A 40 GHz Microwave Power Meter with a Range from −30 dBm to +15 dBm*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

EVAl-SDP-CB1Z System Demonstration Platform User Guide (UG-277).

Data Sheets and Evaluation Boards

ADL5904 Data Sheet and Evaluation Board

AD7091R Data Sheet and Evaluation Board

ADP160 Data Sheet and Evaluation Board

REVISION HISTORY

4/2017—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab reference designs are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab reference designs in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab reference designs are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab reference designs at any time without notice but is under no obligation to do so.

©2017 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

CN15768-0-4/17(0)

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0385.

Devices Connected/Referenced	
AD4003	18-Bit, 2 MSPS, PulSAR®, 7.0 mW ADC in MSOP/QFN
AD8251	10 MHz, 20 V/µs, G = 1, 2, 4, 8, *i*CMOS Programmable Gain Instrumentation Amplifier
ADuM141E	Robust, Quad Channel Isolator with Output Enable and 1 Reverse Channel
ADG5207	High Voltage, Latch-Up Proof, 8-Channel Differential Multiplexer
AD8475	Precision, Selectable Gain, Fully Differential Amplifier
ADA4807-2	3.1 nV/√Hz, 1 mA, 180 MHz, Rail-to-Rail Input/Output Dual Op Amp

Isolated, Multichannel Data Acquisition System with PGIA for Single-Ended and Differential Industrial Level Signals

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0385 Circuit Evaluation Board (EVAL-CN0385-FMCZ)
System Demonstration Platform (EVAL-SDP-CH1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a cost effective, isolated, multichannel data acquisition system that is compatible with standard industrial signal levels. The components are specifically selected to optimize settling time between samples, providing 18-bit performance at channel switching rates up to approximately 750 kHz.

The circuit can process eight gain-independent channels and is compatible with both single-ended and differential input signals.

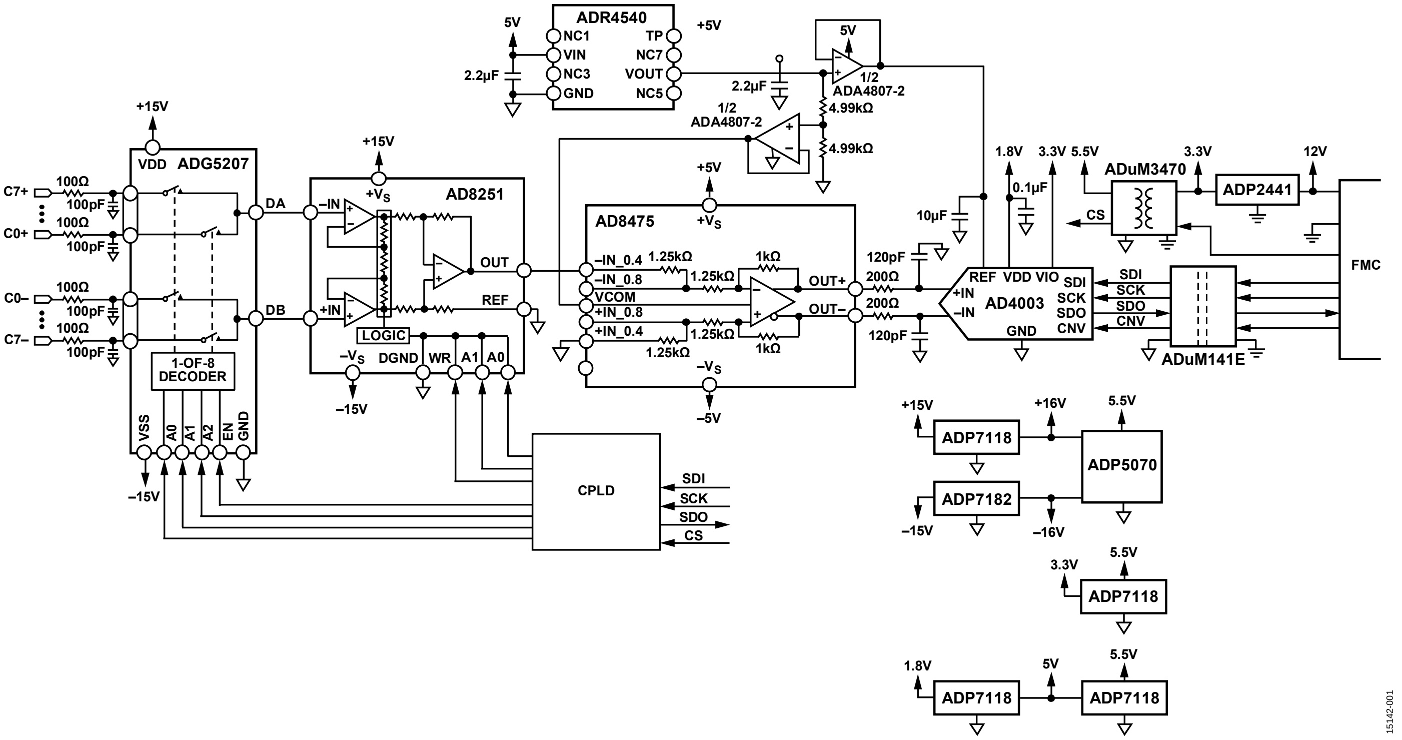
The analog front end includes a multiplexer, programmable gain instrumentation amplifier (PGIA); precision analog-to-digital converter (ADC) driver for performing the single-ended to differential conversion; and an 18-bit, 2.0 MSPS precision PulSAR® ADC for sampling the signal on the active channel. Gain configurations of 0.4, 0.8, 1.6, and 3.2 are available.

The maximum sample rate of the system is 2 MSPS in turbo mode, and 1.5 MSPS in normal mode. The channel switching logic is synchronous to the ADC conversions, and the maximum channel switching rate is 1.5 MHz. A single channel can be sampled at up to 2 MSPS with 18-bit resolution in turbo mode. Channel switching rates up to 750 kHz also provide 18-bit performance.

Rev. 0

Circuits from the Lab® reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
www.analog.com
Fax: 781.461.3113
©2016 Analog Devices, Inc. All rights reserved.



ADR4540
NC1
VIN
NC3
GND
TP
NC7
VOUT
NC5
5V
+5V
2.2µF
2.2µF
1/2
ADA4807-2
4.99kΩ
4.99kΩ
+15V
VDD ADG5207
C7+
100Ω
100pF
C0+
C0–
C7–
DA
DB
1-OF-8
DECODER
VSS
A0
A1
A2
EN
GND
–15V
AD8251
–IN
+IN
+VS
–VS
OUT
REF
LOGIC
DGND
WR
A1
A0
AD8475
–IN_0.4
–IN_0.8
VCOM
+IN_0.8
+IN_0.4
1.25kΩ
1kΩ
OUT+
OUT–
–5V
CPLD
SDI
SCK
SDO
CS
10µF
120pF
200Ω
1.8V
3.3V
5.5V
0.1µF
REF VDD VIO
+IN
–IN
AD4003
GND
SDI
SCK
SDO
CNV
ADuM3470
ADP2441
12V
FMC
ADuM141E
+15V
+16V
ADP7118
ADP7182
ADP5070
–15V
–16V
3.3V
1.8V
15142-001

Figure 1. Isolated Multichannel Data Acquisition Simplified Circuit (All Connections and Decoupling Not Shown)

CIRCUIT DESCRIPTION

The circuit shown in Figure 1 is an isolated multichannel data acquisition signal chain consisting of a multiplexer, programmable gain stage, ADC driver, and a fully differential, precision, successive approximation register (SAR) ADC. The channel switching and gain switching is synchronized to the conversion period of the ADC.

The system can monitor up to eight channels using a single ADC, reducing component count and cost compared to systems with one ADC per channel. Each channel can be configured with a different gain, allowing for flexibility of input ranges. It is manipulated by the complex programmable logic device (CPLD) which can be configured in the Labview graphical user interface (GUI). The effective sample rate for each channel is equal to the sample rate of the ADC divided by the total number of channels being sampled.

The maximum sample rate of the system is limited by the settling time of the components (such as the programmable gain amplifier (PGA) bandwidth and RC filter bandwidth) in the analog front end and the isolated digital interface clock rate which runs at 75 MHz. Multiplexed signals are discontinuous in nature, resulting in potentially large voltage steps between sampling intervals. The components in the signal chain must be given adequate time to settle to these steps before the ADC performs a conversion. To maximize the time given for the signal to settle, the multiplexer channels are switched immediately after the ADC begins a new conversion.

The board power supply can take a dc input from 5 V to 12 V at the dc jack or 12 V from the SDP-H1 controller board. The ADP2441 dc-to-dc converter generates 3.3 V for the digital interface and the ADuM3470 primary supply input. The ADP5070, ADP7118, and ADP7182 are used to generate positive and negative ±15 V supplies. The ADP7118 is used to generate 5 V, 3.3 V, and 1.8 V for the analog and digital power supplies. The ADuM141E is selected for isolated high speed SPI communication. It has 150 Mbps maximum data rate, low propagation delay, and low dynamic power consumption.

Component Selection

The ADG5207 is a high voltage, latch-up proof, 8-channel differential multiplexer. The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. A switching network at the inputs of the ADG5207 adds compatibility with both single-ended and differential input signals. The active channel is selected via the address pins of the device, which are controlled by the CPLD, and which can be configured in the GUI.

The AD8251 is a programmable gain instrumentation amplifier that provides selectable gain settings of 1, 2, 4, and 8. The higher gain settings boost smaller input signals to the full-scale input range of the AD4003. Each gain setting has its own suitable input range, which is shown in Table 1.

Table 1. Input Range for Each of the Four Gain Configurations

Gain	Full-Scale Input Range
0.4	±10.24 V
0.8	±5.12 V
1.6	±2.56 V
3.2	±1.28 V

The AD8475 funnel amplifier provides high precision attenuation (0.4×), accurate common-mode level shifting, and single-ended to differential conversion. Its low output noise spectral density (10 nV/√Hz) and fast settling time (50 ns to 0.001% for a 2 V output step) make it well suited to drive the AD4003.

The AD4003 is a fully-differential, 2 MSPS, 18-bit precision SAR ADC that features a typical signal-to-noise ratio (SNR) of 98 dB when using a 4.096 V reference. The AD4003 is also low power, and only consumes approximately 17 mW at full throughput. Its power consumption scales with throughput, and can operate at lower sample rates to cut its power use (for example, 0.17 mW at 100 kSPS).

System DC Accuracy Errors

Figure 2 shows the ideal transfer function of the data acquisition system.

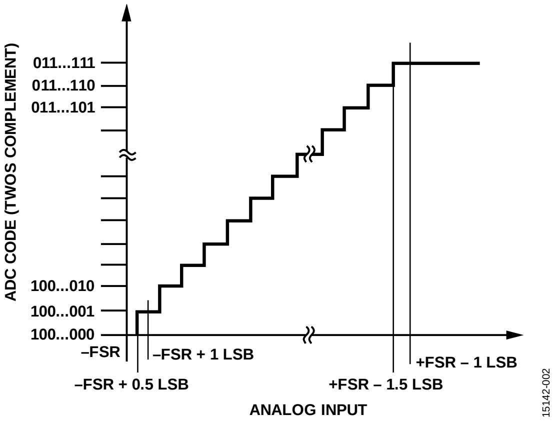


Figure 2. ADC Ideal Transfer Function

Each of the components in the data acquisition signal chain adds its own offset error and gain error that cause the real transfer function of the system to deviate from the ideal transfer function shown in Figure 2. The cumulative effects of these errors can be measured at a system level by comparing known dc inputs near zero and full scale at the input to the ADG5207 (RC filter if it is present) and the resulting output codes from the AD4003 to obtain a system calibration factor.

Offset Error Measurement

For ideal bipolar, differential ADCs, a 0 V differential input results in an output code of 0. Real ADCs typically exhibit some offset error (ε_b), which is defined as the deviation between the ideal output code and the measured output code for a 0 V input.

The offset error for the data acquisition system can be found by grounding its input and observing the resulting output code. This error varies between each of the gain settings of the AD8251 and between each of the channels of the ADG5207. Offset error is therefore measured for each of the channels in all four gain configurations.

Because the system monitors multiple channels, it is also important to quantify the amount by which the offset error deviates between channels. Offset error match ($\Delta\varepsilon_{b,MAX}$) is a measure of the maximum deviation between the offset error of each of the channels and the average offset error of all of the channels. Offset error match is calculated using the following equation:

$$\overline{\Delta\varepsilon_{b,\,MAX}} = (\max(\varepsilon_{b,i} - \frac{\sum_{j=0}^{7}\varepsilon_{b,j}}{8}) \mid i = 0, 1, \ldots, 7)$$

where $\varepsilon_{b,i}$ and $\varepsilon_{b,j}$ are the offset errors for the i and j channels, respectively.

This offset error match can be found for each of the gain configurations. Note that offset error can be expressed either in codes or volts.

Gain Error Measurement

Error in the gain of the system also contributes to overall system inaccuracy. The ideal transfer function of the AD4003 is shown in Figure 2, where the -2^{17} and $2^{17} - 1$ output codes correspond to a negative full-scale input voltage (−FS) and a positive full-scale input voltage (+FS), respectively; however, the combination of offset error (ε_b) and gain error (ε_m) results in a deviation from this relationship.

Gain error can be expressed as a percentage error between the actual system gain and the ideal system gain. The more common expression is in percent full-scale error (%FS), which is a measure of the error between the ideal and actual input voltages that produces the $2^{17} - 1$ code.

The ideal full-scale input voltage ($V_{FS,\,IDEAL}$) is a function of the resolution of the ADC (18-bits for the AD4003) and the accuracy of the reference voltage (V_{REF}). Errors in the voltage reference translate to gain errors in the ADC. To decouple reference errors from ADC gain error, V_{REF} is measured using a precision multimeter. The ideal full-scale input voltage can then be calculated using

$$V_{FS,\,IDEAL} = \frac{2^{18}}{2 \times V_{REF,\,MEAS}} = \frac{2^{17}}{V_{REF,\,MEAS}}$$

The actual system gain can be found by calculating the slope of the linear regression of a group of several input voltages (m_{LR}) and the resulting output codes:

$$Y_{REAL} = m_{LR} \times V_{IN}$$

The real full-scale input voltage ($V_{FS,\,REAL}$) can then be calculated using

$$V_{FS,\,REAL} = \frac{Y_{REAL}}{m_{LR}} = \frac{2^{17}}{m_{LR}}$$

The gain error (expressed in %FS error) can then be calculated using

$$\varepsilon_m = \frac{V_{FS,\,IDEAL} - V_{FS,\,REAL}}{V_{FS,\,IDEAL}} \times 100\%$$

The gain error of the system varies with the gain of the AD8251, but is channel independent. Therefore, gain error is measured for each of the four gain configurations, but only using one of the ADG5207 channels in this system.

System Noise Analysis

One of the key design goals in precision data acquisition systems is achieving a high SNR, which can be achieved by increasing the full-scale signal amplitude and/or by decreasing the noise power generated by the components in the system.

The total noise power present in the system can be found by taking the root sum square (rss) of the noise power contributed by its individual components, referred to the input of the AD4003:

$$v_{n,TOTAL} = \sqrt{v_{n,ADG5207}^2 + v_{n,AD8251}^2 + v_{n,AD8475}^2 + v_{n,AD4003}^2}$$

The expected SNR of the system ($SNR_{EXPECTED}$) can then be found using

$$SNR_{EXPECTED} = 20\log\left(\frac{V_{REF}/\sqrt{2}}{v_{n,TOTAL}}\right)$$

The expected noise contributions for each component in the system and the resulting expected SNR performance of the whole system is shown in Table 2. The total system noise calculation ignores thermal noise contributed by the passive components in the system.

Noise Due to the AD4003 ADC

The noise of the AD4003 ADC is a function of both its inherent quantization error and noise caused by internal components (such as passive components producing thermal noise).

The rms input voltage noise of the AD4003 can be calculated from its specified SNR using

$$v_{n,AD4003} = \frac{V_{REF}}{\sqrt{2}} \times 10^{\left(\frac{SNR_{AD4003}}{20}\right)}$$

The SNR for the AD4003 (SNR_{AD4003}) is specified as approximately 98 dB for a 4.096 V reference.

The single-pole RC filter at the input of the AD4003 limits the wideband noise from the upstream components. A smaller filter bandwidth improves SNR by further limiting noise power; however, its time constant must also be sufficiently short to settle voltage kickbacks due to charge injections that occur as the AD4003 inputs reconnect to the front-end circuitry during the acquisition phase. The appropriate bandwidth for the system is at least 5 MHz (for more information, see the Analog Dialogue article, *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter*).

Noise Due to the AD8475 Funnel Amplifier

The rms noise contributed by the AD8475 ($v_{n,AD8475}$) is a function of its referred to output noise spectral density (NSD) (e_{AD8475}) and the RC filter bandwidth at the input to the AD4003 (BW_{RC}):

$$v_{n,AD8475} = e_{AD8475} \times \sqrt{\frac{\pi}{2} \times BW_{RC}}$$

where e_{AD8475} = 10 nV/√Hz.

Noise Due to the AD8251 Instrumentation Amplifier

The AD8251 functions as a gain stage that improves SNR for small amplitude signals by boosting their amplitude to more closely fill the $\pm V_{REF}$ range at the input to the AD4003. Ideally, if the system gain increases by a factor of G, the SNR (in dB) of the input signal improves by

$$\Delta SNR = \log_{10}(G)$$

This level of improvement is not achievable in reality, however, because wideband noise is also amplified by the noise gain of the circuit. Fortunately, this degradation is not as large as the improvement due to signal gain.

The rms noise contributed by the AD8251 is a function of its referred to input NSD (e_{AD8251}), its gain setting (G_{AD8251}), the attenuation factor of the AD8475 (G_{AD8475}), and the noise filter bandwidth at the input of the AD4003:

$$v_{n,AD8251} = e_{AD8251} \times G_{AD8251} \times G_{AD8475} \times \sqrt{\frac{\pi}{2} \times BW_{RC}}$$

The value of e_{AD8251} is also dependent on the AD8251 gain; the value of e_{AD8251} can be found in the AD8251 data sheet.

Noise Due to the ADG5207 Multiplexer

The NSD and resulting rms noise contributed by the ADG5207 can be found by using the Johnson/Nyquist noise equation, because the device acts like a series resistance between the source and the rest of the analog front end:

$$e_{n,ADG5207} = \sqrt{4 \times k_B \times T \times R_{ON}}$$

and

$$v_{n,ADG5207} = e_{n,ADG5207} \times G_{AD8251} \times G_{AD8475} \times \sqrt{\frac{\pi}{2} \times BW_{RC}}$$

The resistance of each channel (R_{ON}) can be found in the ADG5207 data sheet.

A summary of the calculated noise performance of the system is shown in Table 2. The largest contributors to the total noise are the AD8251 in-amp and the AD4003 ADC.

Table 2. Noise Performance for the Multichannel Data Acquisition System

	ADG5207		AD8251		AD8475		AD4003	Total	
Gain	e_n, ADG5207 (nV/√Hz)	v_n, ADG5207 (µV rms)	e_n, AD8251 (nV/√Hz)	v_n, AD8251 (µV rms)	e_n, AD8475 (nV/√Hz)	v_n, AD8475 (µV rms)	v_n, AD4003 (µV rms)	v_n, total (µV rms)	SNR (dB)
0.4	2.04	2.29	40	44.7	10	28	35.4	63.6	93.2
0.8	2.04	4.57	27	60.4	10	28	35.4	75.5	91.7
1.6	2.04	9.15	22	98.4	10	28	35.4	108.6	88.5
3.2	2.04	18.3	18	161	10	28	35.4	168.2	84.7

Settling Time Analysis

When the circuit shown in Figure 1 is sampling multiple channels, each of the different inputs are merged into a time-division multiplexed signal by the ADG5207. Multiplexed signals are discontinuous in nature, and typically have large voltage steps occurring in short time intervals. For the system in Figure 1, the voltage differential between two consecutive channels may be as large as 20 V at the inputs of the ADG5207, and the time allotted for settling is only as long as the sampling period.

Figure 3 shows the settling time model of the circuit in Figure 1. Each of the components in the system has its own settling characteristics (see the following sections).

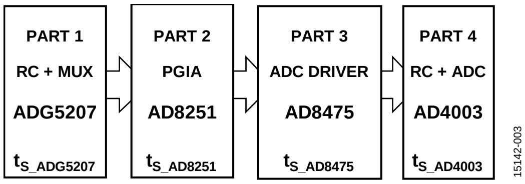


Figure 3. Settling Time Model of CN-0385 Circuit

Settling time is defined as the time required for the analog front-end circuitry to settle an input step to a certain precision. This precision is usually specified in percent error (for example, 0.1% or 0.01%); however, in conversion systems, it is also helpful to relate it to resolution. For example, settling to a 16-bit resolution is roughly equivalent to settling to 0.001%. Table 3 shows the relationship between settling to percent error and to resolution for a single-pole system.

Table 3. Percent Error and Effective Resolution

Resolution, No. of Bits	LSB (%FS)	No. of Time Constants = −ln (% Error/100)
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

Estimating the settling time of an analog front end with multiple components is not trivial for a variety of reasons. First, many devices do not specify settling characteristics to very high precision. Settling time for an active device is also not linearly related to settling precision, and it may take up to 30 times as long to settle to 0.01% as to 0.1%. The settling time can be due to long-term thermal effects inside the amplifier. Settling time is also dependent on the load that the device is driving, and settling time is generally not characterized for multiple load conditions.

Measuring high precision settling is also difficult without a specialized characterization platform, because of the effects of oscilloscope overdrive and sensitivity, and the difficulty of generating an input pulse with sufficient rise time and settling time.

Settling time can be estimated provided certain bounds and assumptions are used in analyzing the circuit. The total settling time can be calculated by taking the rss of the settling times of the individual components:

$$t_{S\_TOTAL} = \sqrt{{t_{S\_ADG5207}}^2 + {t_{S\_AD8251}}^2 + {t_{S\_AD8475}}^2 + {t_{S\_AD4003}}^2}$$

The maximum throughput of the system is inversely proportional to the total settling time:

$$f_{SR} < \frac{1}{t_{S\_TOTAL}}$$

Settling Time of the ADG5207

The equivalent circuit for a CMOS switch can be approximated as an ideal switch in series with a resistor (R_{ON}) and in parallel with two capacitors (C_S, C_D). The multiplexer stage and associated filters can therefore be modeled as shown in Figure 4.

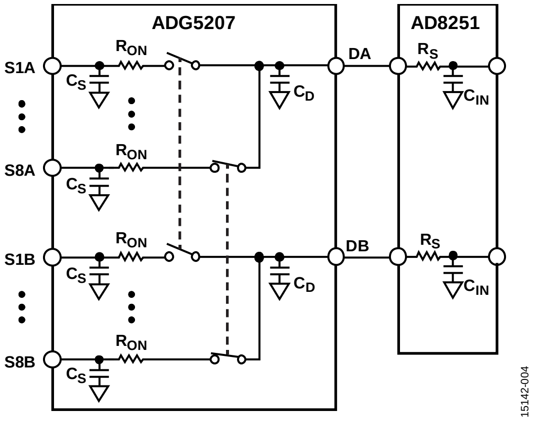


Figure 4. Settling Time Model of the ADG5207

Each channel functions similarly to an RC circuit having an associated time constant that dominates settling time. Dynamically switching channels complicates signal settling; at the time channels are switched, the difference between the previous output and the current input produces a kickback transient. This kickback is similar to the one that occurs at the input to the AD4003 as it enters the acquisition phase. For a more detailed description, see the Analog Dialogue article, *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter*.

The circuit in Figure 4 was simulated using NI Multisim™, as shown in Figure 5, with the following component values from the respective device data sheets:

- R_{ON} = 250 Ω
- C_S = 3.5 pF
- C_D = 36 pF
- $R_{IN}||C_{IN}$ = 1.25 GΩ||2 pF

The input resistance of the AD8251 (R_{IN}) is sufficiently large (1.25 GΩ) to be omitted from simulation.

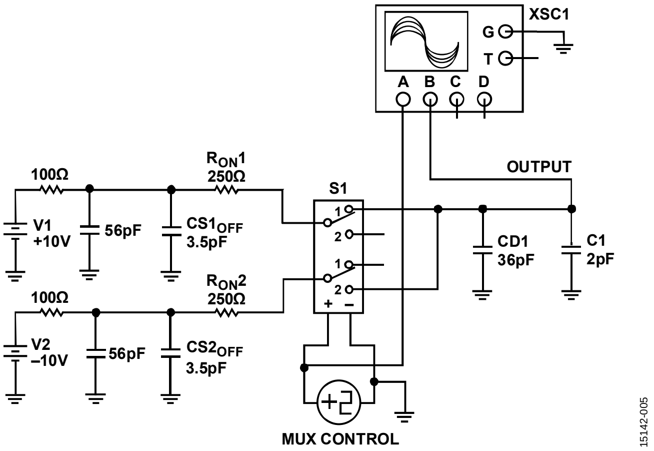


Figure 5. Multisim Settling Time Model of the ADG5207

The simulation results are shown in Figure 6. The time required for the output of the ADG5207 to settle to 0.001% of 10 V is $t_{S\_ADG5207}$ = 188 ns.

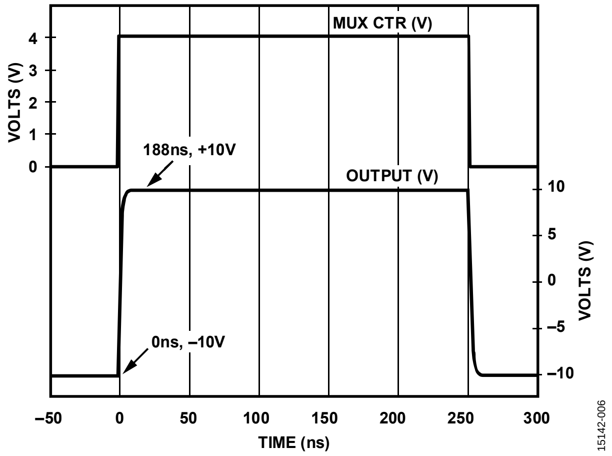


Figure 6. Settling Time Waveforms for the ADG5207 Simulation Model

Settling Time of the AD8251 and AD8475

The AD8251 data sheet specifies its settling time for a variety of input voltage step sizes down to a 0.001% error for each gain configuration. Given a load of 10 kΩ and gain setting of 1, the AD8251 can settle a 20 V step at its output to 0.001% in approximately 1 µs. The gain of 1 setting requires the most settling time; therefore, the settling time analysis uses 1 µs.

However, the 1 µs number may not be accurate when the AD8251 is driving one of the inputs of the AD8475, which has an input impedance of 2.92 kΩ instead of 10 kΩ. It is also not possible to ascertain settling time of the AD8251 to 18-bit resolution, because of the nonlinear relationship between settling time and precision. Therefore, the best settling time estimation is 0.001% error (or 16-bit resolution).

The AD8475 has a settling time specification of 50 ns to 0.001% for a 2 V differential output step. The maximum voltage step size expected on the outputs of the AD8475 is twice the reference voltage (V_{REF}), or approximately 8 V. Assuming that the settling time is proportional to the output voltage step, the settling time to 0.001% (16 bits) for an 8 V step is approximately 200 ns (4 × 50 ns).

The settling time of each amplifier is, therefore,

- t_{S_AD8251} = 1 µs
- t_{S_AD8475} = 200 ns

Settling Time of the RC Noise Filter and AD4003

Figure 7 shows the equivalent circuit of the inputs of the AD4003. R_{EXT} and C_{EXT} are the components in the RC wideband noise filter in front of the ADC. R_{IN} and C_{IN} are the input resistance and capacitance of the AD4003, respectively. C_{IN} is mainly the internal capacitive digital-to-analog converter (DAC). C_{PIN} is primarily the pin capacitance, and is ignored. The values for these components are as follows:

- R_{EXT} = 200 Ω
- C_{EXT} = 120 pF
- R_{IN} = 400 Ω
- C_{IN} = 40 pF

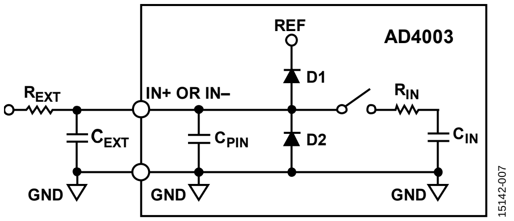


Figure 7. Settling Time Model of the AD4003 and RC Noise Filter

The AD4003 employs an internal capacitive DAC and a charge redistribution algorithm to determine its output code. The conversion process contains two phases, acquisition and conversion. During acquisition, the capacitive DAC is connected to the input terminals of the AD4003. During conversion, it is disconnected from the input terminals, and internal logic performs the charge-redistribution algorithm. Compared to other PulSAR ADCs, the AD4003 has a much shorter conversion time, and it allows the user to return to acquisition phase before the end of conversion. Therefore, if the user runs the ADC at slower throughput, there is have more time to settle the kickback.

The signal must be settled by the end of the acquisition phase for an accurate conversion. To maximize the time given for the signal to settle, the multiplexer switches channels immediately after the AD4003 begins its conversion phase.

In addition to settling from the multiplexed signal from the output of the AD8475, the RC noise filter and AD4003 inputs also need to settle to the voltage kickback that occurs at the beginning of the acquisition phase. For more information, see the Analog Dialogue article, *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter*.

The settling time for the circuit in Figure 7 was simulated in NI Multisim, as shown in Figure 8. V1 represents the maximum voltage step expected at either input of the AD4003 (from a single-ended output of the AD8475). CNV and S1 simulate the AD4003 switching from the conversion phase (occurring when V1 changes value) to the acquisition phase (300 ns after start of conversion). CNV keeps S1 open until 300 ns after V1 steps from 0 V to 4 V to represent the transition from the conversion phase to the acquisition phase. ADC_IN is the voltage that is sampled by the AD4003 on a CNV rising edge.

The settling time for this portion of the system is equal to the time between V1 switching to 4 V (at TIME = 0, see Figure 9) to ADC_IN settling to 0.001% of 4 V.

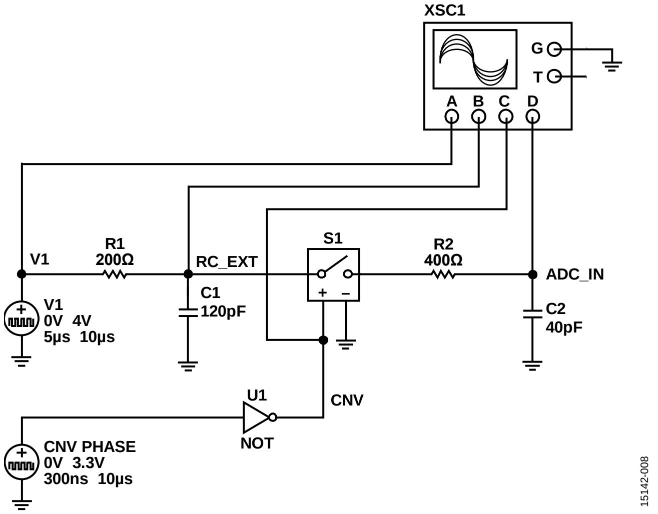


Figure 8. Multisim™ Settling Time Model of the AD4003 and RC Noise Filter

The simulation results are shown in Figure 9. The time taken for the output to settle to 0.001% of 4 V is t_{S_AD4003}= 711 ns.

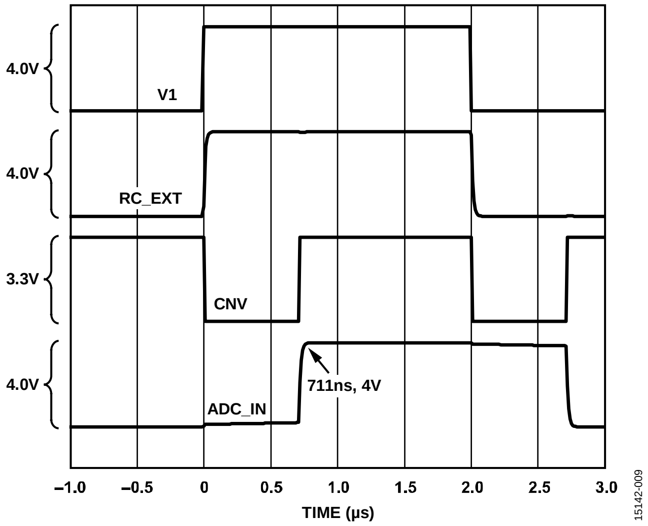


Figure 9. Settling Time Waveforms for the AD4003 and RC Noise Filter Simulation Model

Total System Settling Time

The total settling time of the entire circuit shown in Figure 1 can now be estimated by calculating the rss of the settling times for each component:

- $t_{S\_ADG5207}$ = 188 ns
- t_{S_AD8251} = 1000 ns
- t_{S_AD8475} = 200 ns
- t_{S_AD4003} = 711 ns
- $t_{S\_TOTAL} = \sqrt{188\ \text{ns}^2 + 1\ \mu\text{s}^2 + 200\ \text{ns}^2 + 711\ \text{ns}^2} \approx 1257\ \text{ns}$

The expected maximum channel switching sample rate of the system is then

$$f_{SR} < \frac{1}{1257\ \text{ns}} \approx 795\ \text{kSPS}$$

Offset and Gain Error Results

Table 4 shows the offset error measured (in LSBs) for each of the channels in each gain configuration for the circuit in Figure 1. Table 4 also shows the average offset error of all of the channels for each gain configuration.

The offset errors were measured by grounding all of the channel inputs and collecting and averaging 32,768 samples taken on each of the channels in each gain configuration.

Table 4. Offset Error Measurements for all Channels and Gain Configurations (Error in LSBs)

Gain	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	Channel Average
0.4	1.34	1.33	1.31	1.36	1.44	1.45	1.46	1.48	1.40
0.8	1.98	1.99	2.02	2.06	2.00	1.98	1.99	1.97	2.00
1.6	3.25	3.19	3.22	3.19	3.17	3.08	3.13	3.14	3.17
3.2	5.57	5.66	5.67	5.55	5.57	5.50	5.54	5.52	5.57

Table 5 shows the gain error measured for each of the gain configurations for the circuit in Figure 1. The %FS error was found using the analysis methods described previously, and the actual gain in V/V was calculated by subtracting this error from the ideal gain.

Table 5. Gain Error Measurements for all Gain Configurations

Gain	Gain Error (%FS)
0.4	0.02
0.8	0.02
1.6	0.03
3.2	0.02

Performance Results Without Channel Switching

Figure 10, Figure 11, Figure 12, and Figure 13 show the fast Fourier transform (FFT) plots for a 10 kHz, full-scale, sine wave input on a single channel for gain configurations of 0.4, 0.8, 1.6, and 3.2, respectively. Table 6 shows the SNR and rms noise measured for each of the gain configurations.

Table 6. SNR, Noise, and THD vs. Gain for 10 kHz Input

Gain	SNR (dB)	RMS Noise (µV rms)	THD (dB)
0.4	93.9	55.2	−99.2
0.8	92.8	62.6	−98.5
1.6	90.6	80.7	−97.0
3.2	88.0	108.9	−94.6

The input signal was supplied by an Audio Precision SYS-2700 series signal generator, with the board set in differential input mode. Figure 14 shows total harmonic distortion (THD) measurements vs. the frequency of the input signal for each gain configuration.

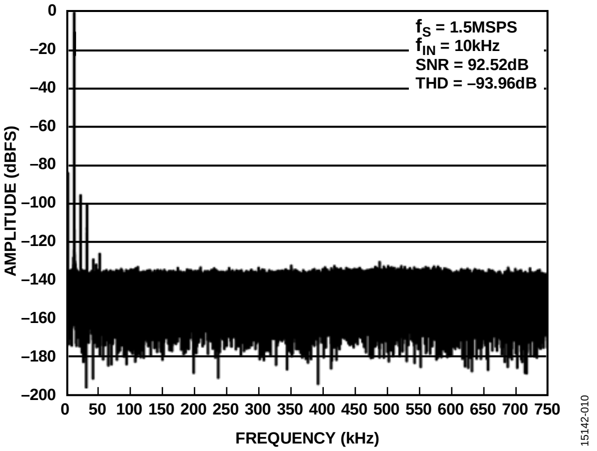


Figure 10. FFT for 10 kHz, 20 V p-p Input for Gain = 0.4 on Single, Static Channel

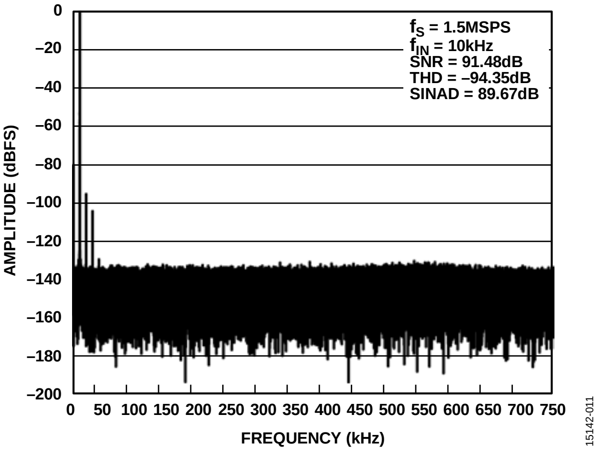


Figure 11. FFT for 10 kHz, 10 V p-p Input for Gain = 0.8 on Single, Static Channel

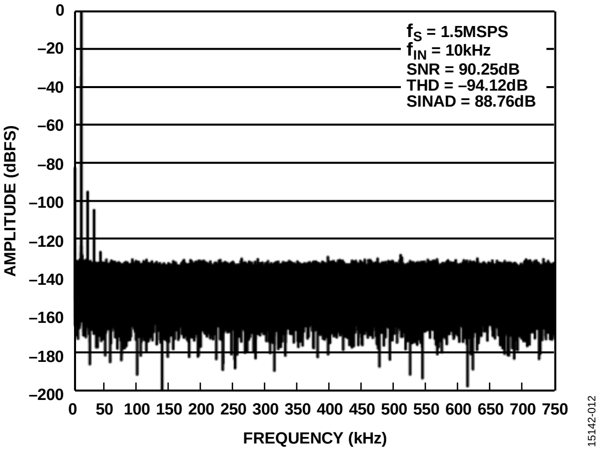


Figure 12. FFT for 10 kHz, 5 V p-p Input for Gain = 1.6 on Single, Static Channel

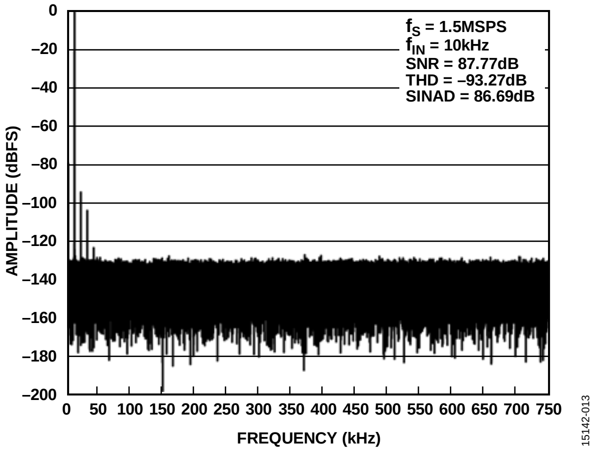


Figure 13. FFT for 10 kHz, 2.5 V p-p Input for Gain = 3.2 on Single, Static Channel

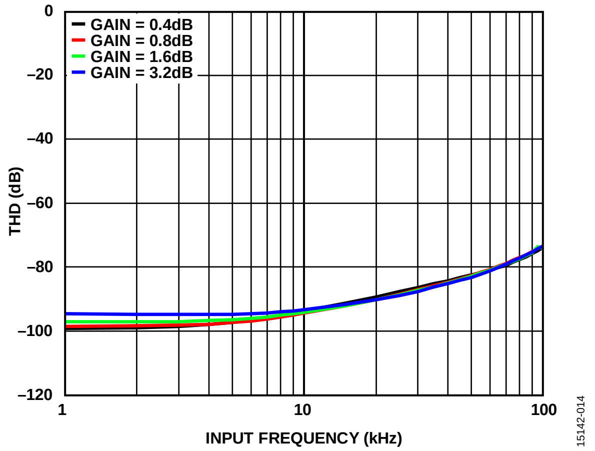


Figure 14. THD Measured for Various Input Frequencies on a Single, Static Channel

System Performance with Channel Switching

Several tests were performed to evaluate the performance of the system when scanning multiple channels. Experiments using precision dc sources measured the error in output code with respect to sample rate (see the Circuit Note CN-0269 for similar tests) and voltage step size between channels. AC performance was also measured for switching between two out of phase, full-scale inputs from a precision ac source (Audio Precision AP SYS-2712).

Figure 15 and Figure 16 show the test setup for dc and ac performance tests, respectively. The channel switching rate is the rate at which the ADG5207 switches from one channel to another, and is equivalent to the sample rate of the AD4003.

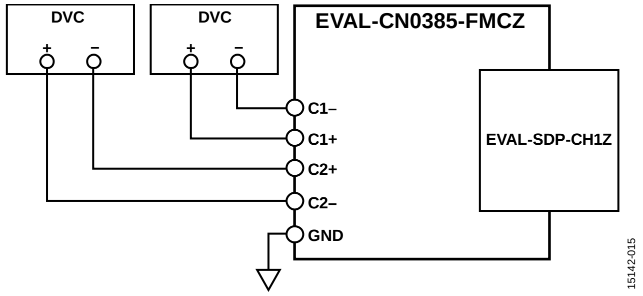


Figure 15. Settling Time Evaluation Setup Using DC Calibrators

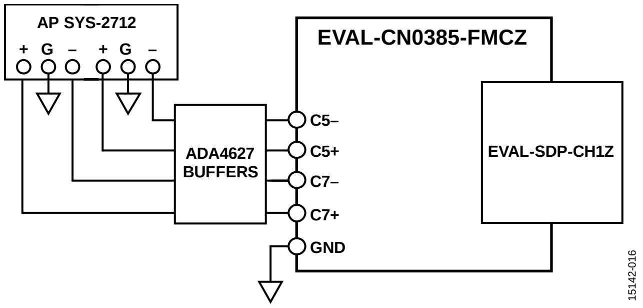


Figure 16. Settling Time Evaluation Setup Using AC Signal Generator

The dc tests involved varying the voltage step size between the two channels and the channel switching rate. The channel switching rate was varied from 50 kHz to 1 MHz in 50 kHz increments. The voltage step size was varied over different ranges for each of the gain configurations. A mean code result was measured for each channel for each voltage step size and channel switching rate by averaging 8,192 samples taken on each channel. A mean code result was also measured for each channel in the static case (no switching between channels). The mean code errors discussed below were found by taking the difference between the mean codes measured for the static case and for the switching channels.

Figure 17, Figure 18, Figure 19, and Figure 20 show the mean code error for various voltage step sizes at several switching rates in each of the four gain configurations. Figure 21, Figure 22, Figure 23, and Figure 24 show the mean code error for full-scale voltage steps at various switching rates in each of the four gain configurations.

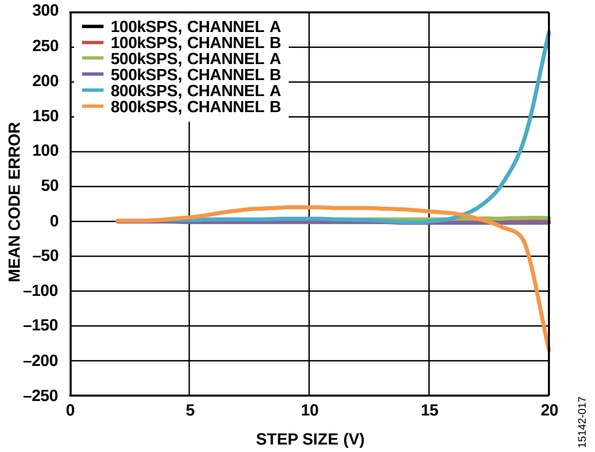


Figure 17. Mean Code Error vs. Voltage Step Size, Gain = 0.4

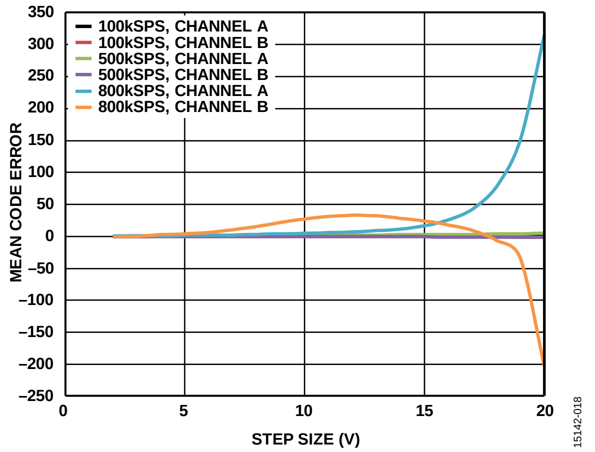


Figure 18. Mean Code Error vs. Voltage Step Size, Gain = 0.8

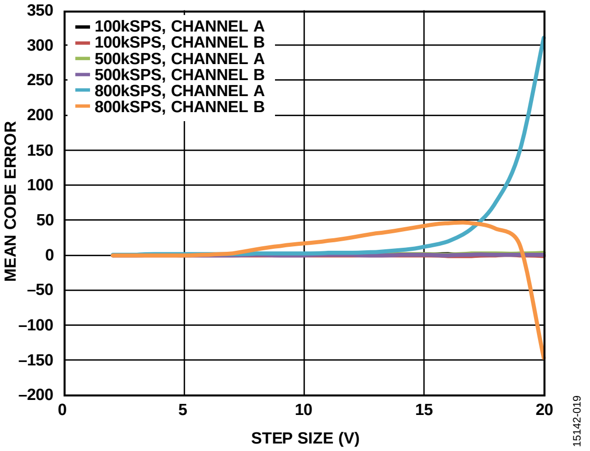


Figure 19. Mean Code Error vs. Voltage Step Size, Gain = 1.6

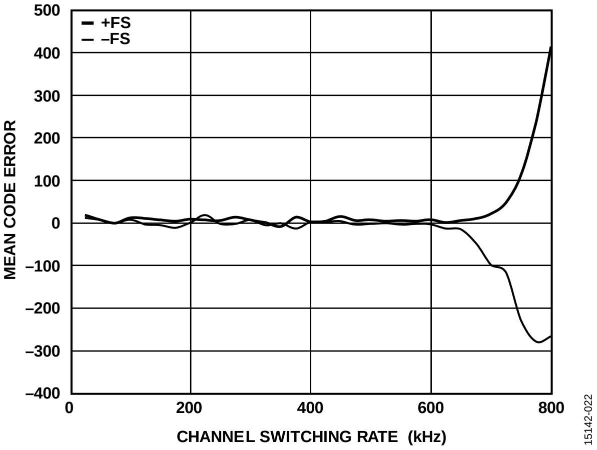


Figure 22. Mean Code Error vs. Channel Switching Rate for Full-Scale Input Step, Gain = 0.8

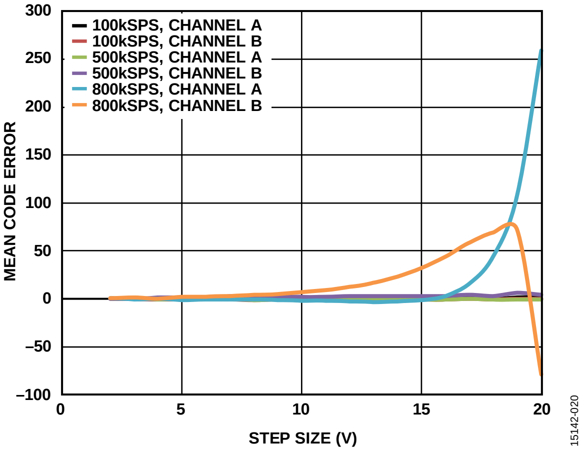


Figure 20. Mean Code Error vs. Voltage Step Size, Gain = 3.2

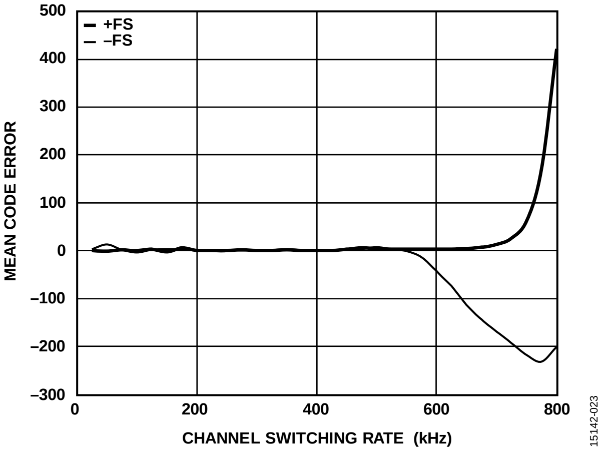


Figure 23. Mean Code Error vs. Channel Switching Rate for Full-Scale Input Step, Gain = 1.6

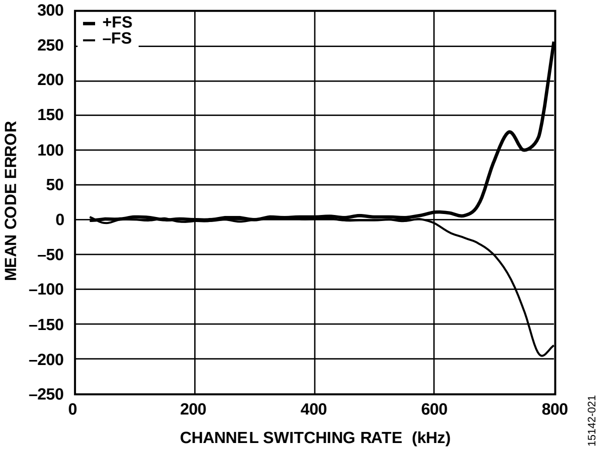


Figure 21. Mean Code Error vs. Channel Switching Rate for Full-Scale Input Step, Gain = 0.4

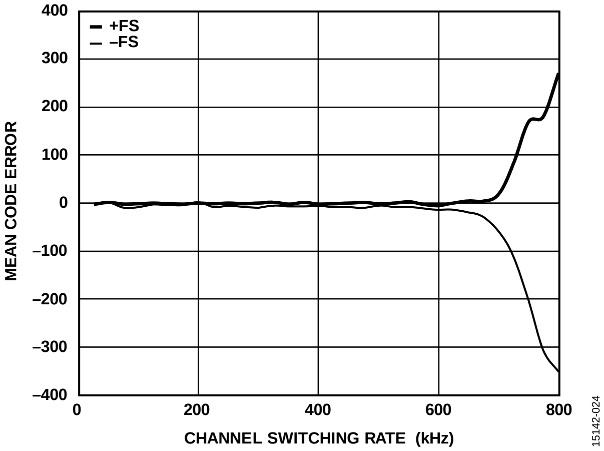


Figure 24. Mean Code Error vs. Channel Switching Rate for Full-Scale Input Step, Gain = 3.2

The mean code error increases as the voltage step size and channel switching rate increase. This increase is caused by the combined slew and settling time limitations of the components in the signal chain. Increasing the step size forces the system to settle larger changes in voltage and increasing the channel switching rate decreases the amount of time the system is given to settle these changes. At sufficiently high step sizes and switching rates, the mean code error becomes unpredictably large, as in the gain of 0.4 configuration (see Figure 17 and Figure 21). This code error is caused by the slew rate limitations of the input buffer amplifiers in the AD8251 in-amp.

The performance of the system when using the ac source was evaluated by comparing its THD with respect to the channel switching rate. The AP SYS-2712 provided a full-scale sine wave input on one channel and an inverted version of the sine wave on another channel. THD was measured for various sample rates, ranging from 25 kSPS to 1.5 MSPS in 25 kSPS increments. Figure 25 shows the THD measured for each of the channels in each of the gain configurations.

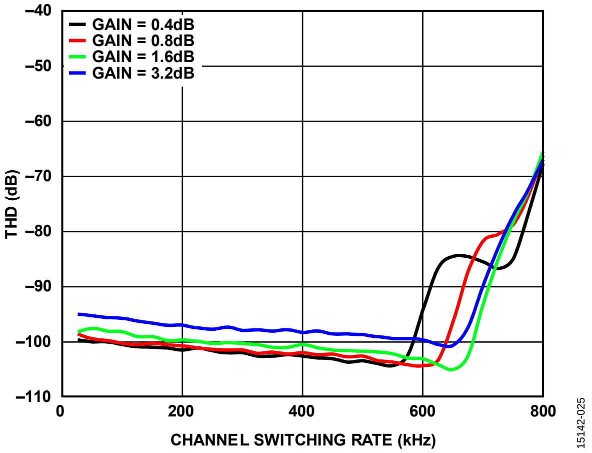


Figure 25. THD vs. ADG5207 Channel Switching Rate for Full-Scale 1 kHz Input

The THD performance of the system begins to degrade at roughly 700 kSPS (depending on the gain configuration). The whole signal chain SNR and THD performance is mainly limited by the PGA AD8251. A smaller RC filter at the front of AD4003 also gives better THD at higher channel switching sampling rate.

COMMON VARIATIONS

The AD4003 ADC is pin-for-pin compatible with various other 14-bit, 16-bit, and 18-bit, 10-lead precision SAR ADCs that can be used in the CN-0385 system. The ADG1207, with wider bandwidth, can be an alternative to the ADG5207. The ADG5248F, with fault protection and detection function, can be used for single-ended inputs. The AD8475 provides a differential output signal for other differential ADCs, such as the AD7690. The ADA4805-1 op amp is an alternative for the AD8475 when driving pseudo differential or single-ended ADCs, such as the AD4000. Other Analog Devices, Inc., LDOs, such as the ADP7102 and ADP7142, can replace the ADP7118.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0385-FMCZ circuit board and the EVAL-SDP-CH1Z SDP-H1 system demonstration platform controller board. The two boards have 160-pin mating connectors, allowing quick setup and evaluation of the performance of the circuit. The circuit board contains the circuit to be evaluated, as described in this circuit note, and the SDP-H1 controller board is used with the CN-0385 Evaluation Software to capture the data from the circuit board.

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP or Windows Vista® (32-bit), or Windows 7 (32-bit)
- EVAL-CN0385-FMCZ circuit evaluation board
- EVAL-SDP-CH1Z SDP-H1 controller board
- CN-0385 Evaluation Software (download from ftp://ftp.analog.com/pub/cftl/CN0385/)
- 5 V to 12 V dc power supply or wall wart (9 V wall wart included with EVAL-CN0385-FMCZ board)
- USB to micro-USB cable
- Low distortion, low output impedance signal generator to provide ±10 V output
- Low noise, high precision dc supply to provide ±10 V output

Getting Started

Download the evaluation software from ftp://ftp.analog.com/pub/cftl/CN0385/, and then install the software on the PC.

Functional Block Diagram

See Figure 1 for the circuit block diagram and the **EVAL-CN0385-FMCZ-SCH.pdf** file for the complete circuit schematic. This file is contained in the CN-0385 Design Support Package (available at www.analog.com/CN0385-DesignSupport). A functional block diagram of the test setup is shown in Figure 26.

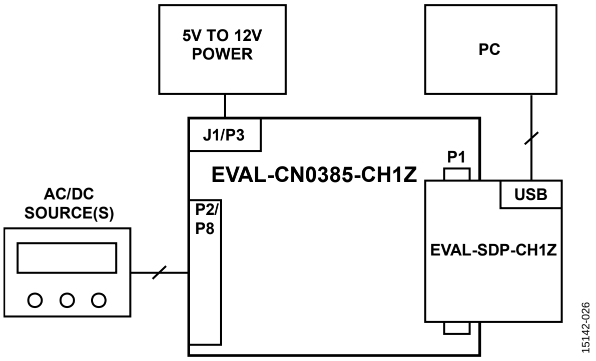


Figure 26. Test Setup Functional Block Diagram

Hardware Setup

Figure 27 shows the EVAL-CN0385-FMCZ evaluation hardware. Information and details regarding the SDP-H1 board can be found in the SDP-H1 User Guide.

Connect the 160-pin connector on the circuit board to the J4 connector on the SDP-H1 controller board.

First, connect a 5 V to 12 V dc wall wart to the P3 dc jack or to Terminal Block J1 and Jumper J2 on position V_EXT. Or, place J2 in position V_FMC to use the 12 V supply from the SDP-H1 board. Then connect the SDP-H1 board to the PC via the USB to micro-USB cable.

Test

With the power supply or dc wall wart and USB cable connected, launch the evaluation software. When USB communications are established, the SDP-H1 board can be used to send, receive, and capture data from the EVAL-CN0385-FMCZ board and perform data analysis in the time and frequency domains.

Information and details regarding test setup and calibration, and how to use the evaluation software for data capture can be found in the CN-0385 Software User Guide (available at www.analog.com/CN0385-UserGuide).

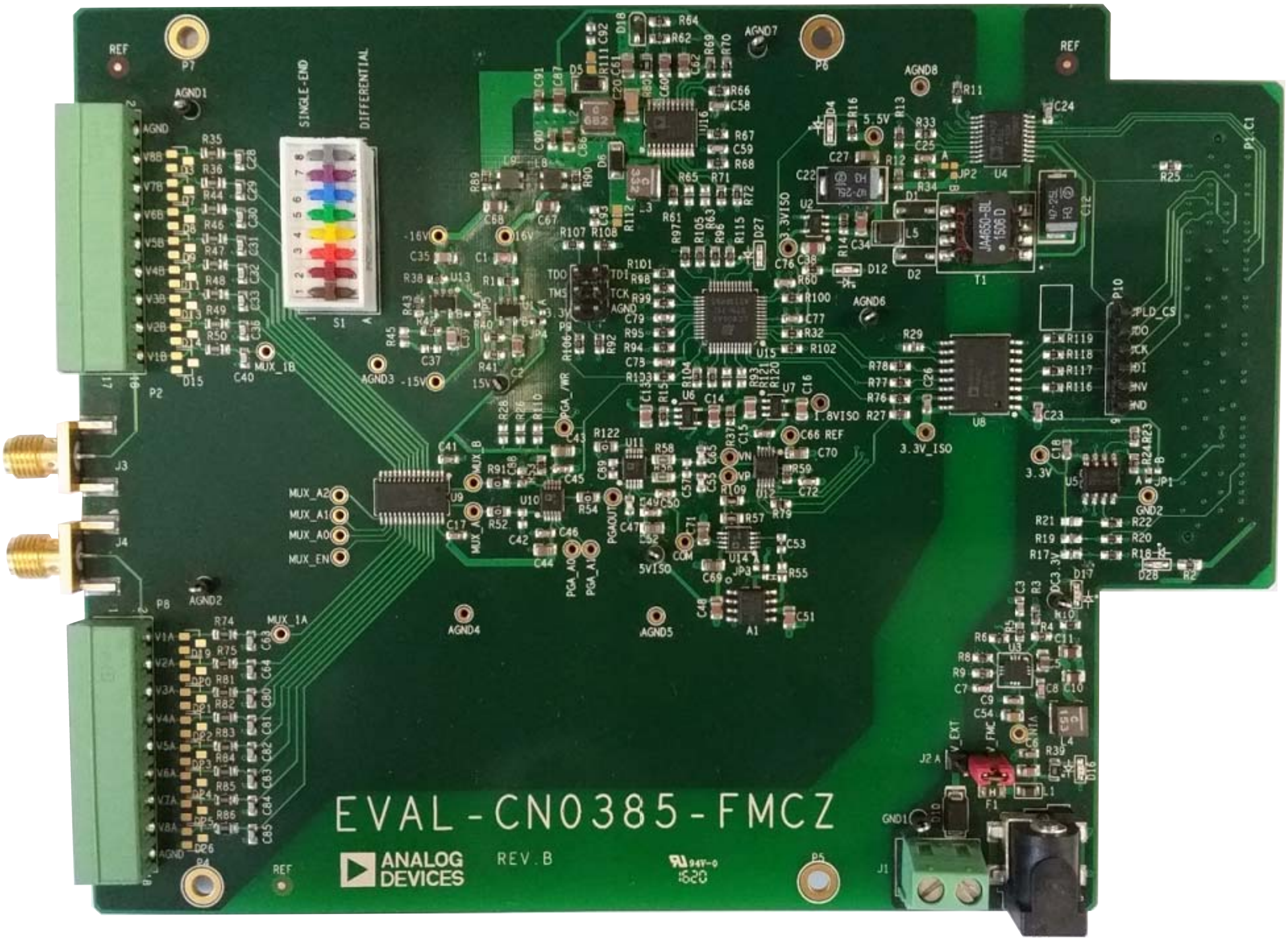


Figure 27. EVAL-CN0385-FMCZ Evaluation Hardware

LEARN MORE

CN-0385 Design Support Package: www.analog.com/CN0385-DesignSupport

UG-502. SDP-H1 User Guide. Analog Devices.

Ardizzoni, John. "A Practical Guide to High-Speed Printed-Circuit-Board Layout," Analog Dialogue 39-09, September 2005.

Kester, Walt. "Multichannel Data Acquisition Systems" in *Data Conversion Handbook*, Chapter 8, Section 8.2. Elsevier.

Pachchigar, Maithil. "Complete Sensor-to-Bits Solution Simplifies Industrial Data-Acquisition System Design," Analog Dialogue 47-04, April 2013.

Pachchigar, Maithil. "Demystifying High-Performance Multiplexed Data-Acquisition Systems," Analog Dialogue 48-07, July 2014.

Walsh, Alan. "Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter," Analog Dialogue 46-12, December 2012.

AN-359 Application Note. *Settling time of Operational Amplifiers*. Analog Devices.

AN-931 Application Note. *Understanding PulSAR ADC Support Circuitry*. Analog Devices.

AN-1024 Application Note. *How to Calculate the Settling Time and Sampling Rate of a Multiplexer*. Analog Devices.

AN-1264 Application Note. *Precision Signal Conditioning for High Resolution Industrial Applications.* Analog Devices.

MT-004 Tutorial. *The Good, the Bad and the Ugly Aspects of ADC Input Noise – Is No Noise Good Noise?* Analog Devices.

MT-046 Tutorial. *Op Amp Settling Time*. Analog Devices.

MT-048 Tutorial. *Op Amp Noise Relationships: 1/f Noise, RMS Noise and Equivalent Noise Bandwidth*. Analog Devices.

Data Sheets and Evaluation Boards

CN-0385 Circuit Evaluation Board (EVAL-CN0385-FMCZ)

System Demonstration Platform (EVAL-SDP-CH1Z)

AD4003 Data Sheet

AD8251 Data Sheet

ADG5207 Data Sheet

ADA4807-2 Data Sheet

AD8475 Data Sheet

ADR4540 Data Sheet

ADuM141E Data Sheet

ADP7118 Data Sheet

ADP7182 Data Sheet

ADP5070 Data Sheet

ADuM3470 Data Sheet

ADP2441 Data Sheet

REVISION HISTORY

10/2016—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab reference designs are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab reference designs in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab reference designs are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab reference designs at any time without notice but is under no obligation to do so.

©2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

CN15142-0-10/16(0)

ANALOG DEVICES

Circuit Note
CN-0191

Circuits from the Lab™

Circuits from the Lab™ tested circuit designs address common design challenges and are engineered for quick and easy system integration. For more information and/or support, visit www.analog.com/CN0191.

Devices Connected/Referenced	
AD5791	1 ppm, 20-Bit, ±1 LSB INL Voltage Output DAC
AD8675	Single, Ultraprecision, 36 V, 2.8 nV/√Hz, Rail-to-Rail Output Op Amp
AD8676	Dual, Ultraprecision, 36 V, 2.8 nV/√Hz, Rail-to-Rail Output Op Amp

20-Bit, Linear, Low Noise, Precision, Bipolar ±10V DC Voltage Source

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides a programmable 20-bit voltage with an output range −10 V to +10 V, ±1 LSB integral nonlinearity, ±1 LSB differential nonlinearity, and low noise.

The digital input to the circuit is serial and is compatible with standard SPI, QSPI™, MICROWIRE®, and DSP interface standards. For high accuracy applications, the circuit offers high precision, as well as low noise, and this is ensured by the combination of the AD5791, AD8675, and AD8676 precision components.

The reference buffer is critical to the design because the input impedance at the DAC reference input is heavily code dependent and will lead to linearity errors if the DAC reference is not adequately buffered. With a high open-loop gain of 120 dB, the AD8676 has been proven and tested to meet the settling time, offset voltage, and low impedance drive capability required by this circuit application. The AD5791 is characterized and factory calibrated using the AD8676 dual op amp to buffer its voltage reference inputs, further enhancing confidence in partnering the components.

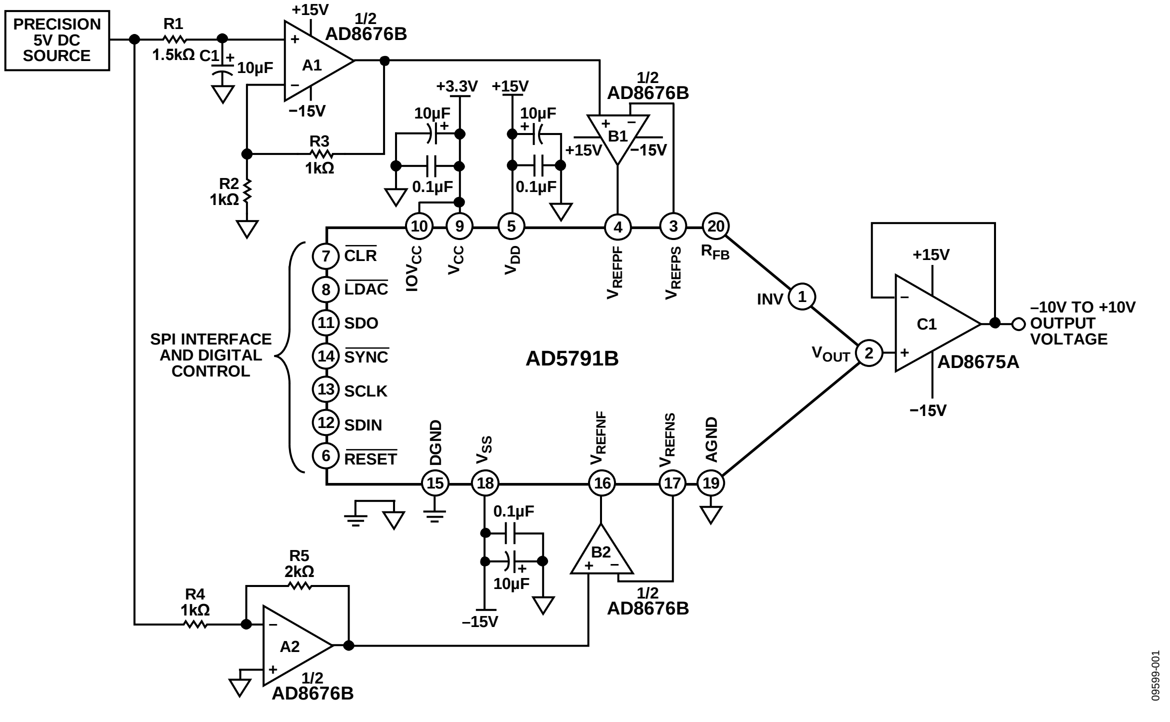

PRECISION 5V DC SOURCE
R1
1.5kΩ
C1
10µF
+15V
1/2 AD8676B
A1
−15V
R3 1kΩ
R2 1kΩ
+3.3V
+15V
10µF
0.1µF
10µF
0.1µF
1/2 AD8676B
B1
+15V
−15V
10 9 5 4 3 20
IOVCC
VCC
VDD
VREFPF
VREFPS
RFB
7 CLR
8 LDAC
11 SDO
14 SYNC
13 SCLK
12 SDIN
6 RESET
SPI INTERFACE AND DIGITAL CONTROL
AD5791B
INV 1
VOUT 2
+15V
C1
AD8675A
−15V
−10V TO +10V OUTPUT VOLTAGE
DGND
VSS
VREFNF
VREFNS
AGND
15 18 16 17 19
0.1µF
10µF
−15V
B2
1/2 AD8676B
R5 2kΩ
R4 1kΩ
A2
1/2 AD8676B
09599-001

Figure 1. 20-Bit Accurate, ±10 V Voltage Source (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. 0

Circuits from the Lab™ circuits from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2011 Analog Devices, Inc. All rights reserved.**

This combination of parts provides industry-leading 20-bit integral nonlinearity (INL) of ±1 LSB and differential nonlinearity (DNL) of ±1 LSB, with guaranteed monotonicity, as well as low power, small PCB area, and cost effectiveness.

CIRCUIT DESCRIPTION

The digital-to-analog converter (DAC) shown in Figure 1 is the AD5791, a high voltage, 20-bit converter with SPI interface, offering ±1 LSB INL and ±1 LSB DNL performance and 7.5 nV/√Hz noise spectral density. The AD5791 also exhibits an extremely low temperature drift of 0.05 ppm/°C. The precision architecture of the AD5791 requires force-sense buffering of its voltage reference inputs to ensure specified linearity. The amplifiers (B1 and B2) chosen to buffer the reference inputs should have low noise, low temperature drift, and low input bias currents. The recommended amplifier for this function is the AD8676, an ultraprecision, 36 V, 2.8 nV/√Hz, dual op amp exhibiting low offset drift of 0.6 μV/°C and input bias currents of 2 nA. In addition, the AD5791 is characterized and factory calibrated using this dual op amp to buffer its voltage reference inputs, further enhancing confidence in partnering the components.

Figure 1 shows the AD5791 configured with independent positive and negative reference voltages, such that the output voltage ranges from the negative reference voltage to the positive reference voltage, in this case from −10 V to +10 V. The output buffer is the AD8675, a single op amp version of the AD8676, used for its low noise and low drift. The AD8676 amplifier (A1 and A2) is also used to scale the +5 V reference voltage to +10 V and −10 V. R2, R3, R4, and R5 in these scaling circuits are precision metal foil resistors with 0.01% tolerance and a temperature coefficient of resistance of 0.6 ppm/°C. For optimum performance over temperature, resistor networks, such as the Vishay 300144 or VSR144 series can be used, The resistor values are selected to be low (1 kΩ and 2 kΩ) to keep noise in the system low. R1 and C1 form a low pass filter with a cutoff frequency of approximately 10 Hz. The purpose of this filter is to attenuate voltage reference noise.

Linearity Measurements

The following data demonstrates the precision performance of the circuit shown in Figure 1. Figure 2 and Figure 3 show integral nonlinearity and differential nonlinearity as a function of DAC code. As can be seen, both are significantly within the specifications of ±1 LSB and ±1 LSB, respectively.

The total unadjusted error for the circuit consists of the dc errors combined together—that is, INL error, zero-scale error, and full-scale error. Figure 4 shows a plot of total unadjusted error as a function of DAC code. The maximum errors occur at DAC code zero (zero-scale error) and DAC code 1,048,575 (full-scale error). This is expected, and is due to the mismatches in resistor pair R2 and R3, resistor pair R4 and R5, and the offset errors of amplifiers A1, A2, B1, and B2 (see Figure 1).

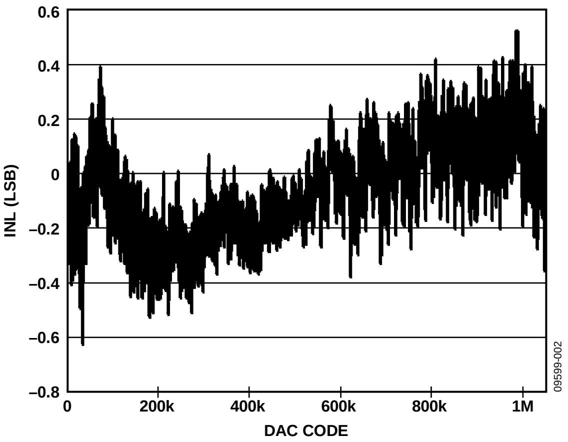


Figure 2. Integral Nonlinearity vs. DAC Code

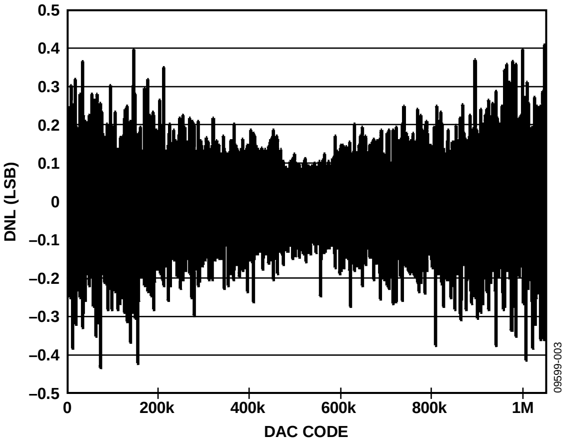


Figure 3. Differential Nonlinearity vs DAC Code

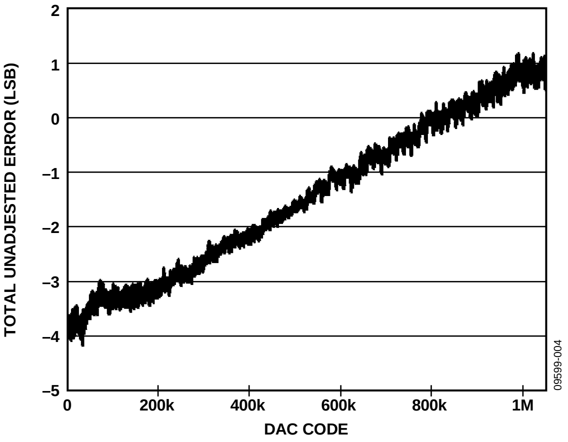


Figure 4. Total Unadjusted Error vs. DAC Code

The specified mismatch in the resistor pairs in this case is 0.02% maximum (the typical mismatch is far less than this). The amplifier offset errors are 75 µV maximum, or 0.000375% of full-scale range and are negligible relative to the error induced by the resistor mismatch. The maximum expected full-scale and zero-scale errors are, therefore, approximately 0.02%, or 210 LSBs each. Figure 4 shows the measured full-scale error to be 1 LSB and the measured zero-scale error to be 4 LSBs, or 0.0003% of full-scale range, indicating that all components are performing significantly better than their specified maximum tolerances.

Noise Measurements

To be able to realize high precision, the peak-to-peak noise at the circuit output must be maintained below 1 LSB, which is 19.07 µV for 20-bit resolution and a 20 V peak-to-peak voltage range. Figure 5 shows peak-to-peak noise measured in the 0.1 Hz to 10 Hz bandwidth over a period of 10 seconds. The peak-to-peak values for each of the three conditions are 1.48 µV for mid-scale output, 4.66 µV for full-scale output, and 5.45 µV for zero-scale output. Mid-scale output exhibits the lowest noise, as it represents the noise from the DAC core only. The noise contribution from each voltage reference path is attenuated by the DAC when mid-scale code is selected.

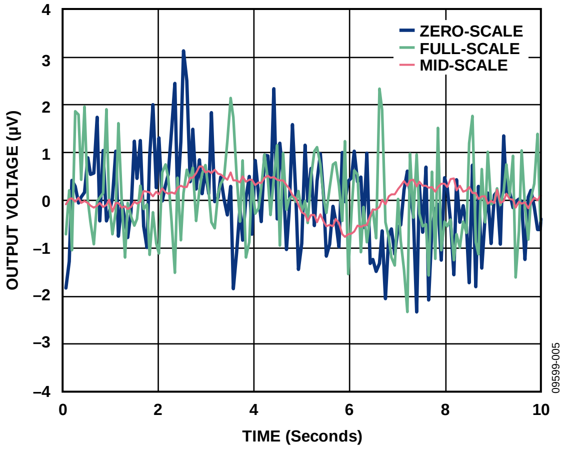


Figure 5. Voltage Noise in 0.1 Hz to 10 Hz Bandwidth

A real application, however, will not have a high-pass cutoff at 0.1 Hz to attenuate 1/f noise but will include frequencies down to dc in its pass band; therefore, the measured peak-to-peak noise will be more realistically as shown in Figure 6. In this case the noise at the output of the circuit was measured over a period of 100 seconds, effectively including frequencies as low as 0.01Hz in the measurement. The upper frequency cutoff is at approximately 14 Hz and is limited by the measurement setup. For the three conditions shown in Figure 6 the peak-to-peak values are: 4.07 µV for mid-scale output, 11.85 µV for full-scale output, and 15.37 µV for zero-scale output. The worst case peak-to-peak value of 15.37 µV corresponds to approximately 0.8 LSB.

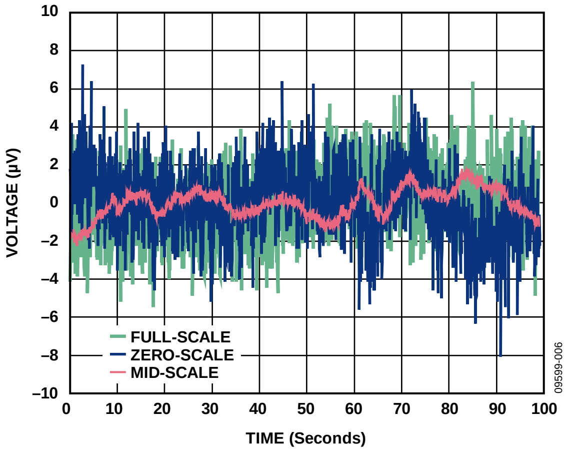


Figure 6. Voltage Noise Measured Over 100 Second Period

As the time period over which the measurement is taken is increased, lower frequencies will be included, and the peak-to-peak value will increase. At low frequencies, temperature drift and thermocouple effects become contributors to noise. These effects can be minimized by choosing components with low thermal coefficients, such as the AD5791, AD8675 and AD8676 and by giving careful consideration to circuit construction, see linked documentation in the LEARN MORE section.

COMMON VARIATIONS

The AD5791 will support a wide variety of output ranges from 0 V to +5 V up to ±10 V, and values in between. The configuration as shown in Figure 1 can be used to generate symmetrical or asymmetrical ranges as required. Individual references are applied at V_{REFP} and V_{REFN}, and the output buffer should be configured for unity gain as described in the AD5791 datasheet, with the RBUF bit of the AD5791 internal control register set to a Logic 1.

The AD5791 also offers a gain of 2 mode of operation that generates a symmetrical bipolar output range from a single positive voltage reference as described in the AD5791 data sheet, removing the necessity to generate a negative voltage reference. This mode, however, will result in larger full-scale and zero-scale errors. This mode is selected by setting the RBUF bit of the AD5791 internal control register to a Logic 0.

CIRCUIT EVALUATION AND TEST

The circuit of Figure 1 was constructed on a modified AD5791 evaluation board. Details of the AD5791 evaluation board and test methods can be found in Evaluation Board User Guide, UG-185.

LEARN MORE

Egan, Maurice. "The 20-Bit DAC Is the Easiest Part of a 1-ppm-Accurate Precision Voltage Source," *Analog Dialogue*, Vol. 44, April 2010.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-016 Tutorial, *Basic DAC Architectures III: Segmented DACs*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets and Evaluation Boards

AD5791 Data Sheet

AD5791 Evaluation Board

AD8676 Data Sheet

AD8675 Data Sheet

REVISION HISTORY

3/11—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab circuits are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab circuits in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab circuits. Information furnished by Analog Devices is believed to be accurate and reliable. However, "Circuits from the Lab" are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab circuits at any time without notice but is under no obligation to do so.

©2011 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

CN09599-0-3/11(0)

LTC4316
EasySMU: I^{2}C Address Translator and Simple Multichannel Source Measurement Unit

DESCRIPTION

EasySMU is a single-channel ±12V/±40mA programmable-voltage/programmable-current source with accurate voltage/current measurement capability. The LTC®4316 I^{2}C address translator enables up to eight independent EasySMUs to be controlled by a single I^{2}C master.

In this demonstration, each EasySMU board contains four I^{2}C slaves and the associated components to implement a single-channel ±12V/±40mA programmable-voltage/programmable-current source. The LTC4316 translates the I^{2}C addresses of each EasySMU to a unique set of addresses, enabling up to eight EasySMU boards to be stacked on a single Linduino® (I^{2}C master). In this form, it resembles a multichannel automated test system. Alternatively, an optional touchscreen allows the user to interactively control up to four channels, forming a compact multichannel programmable-voltage/programmable-current bench source for lab testing, powered from a single 12V AC/DC wall adapter.

The primary purpose of the EasySMU is to demonstrate the LTC4316 I^{2}C address translator. The programmable-voltage/programmable-current source and meter also provide a convenient demonstration of the associated components: LT®1970A, LT5400-3, LTC2655-H, LTC3265, LTC2051, LT3010, LT1991, LTC6655, and LTC2485.

While the EasySMU is not designed to demonstrate the ultimate performance that can be obtained from each of those components, the EasySMU does provide impressive results from a reasonably simple circuit.

Design files for this circuit board are available at http://www.linear.com/demo/DC2591A

, LT, LTC, LTM, Linear Technology, Linduino and the Linear logo are registered trademarks and QuikEval is a trademark of Analog Devices, Inc. All other trademarks are the property of their respective owners.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

EasySMU SET VOLTAGE	EasySMU VOLTAGE MEASUREMENT ERROR[1]
–5V to 5V	±0.25mV
–12V to –5V, 5V to 12V	±0.5mV

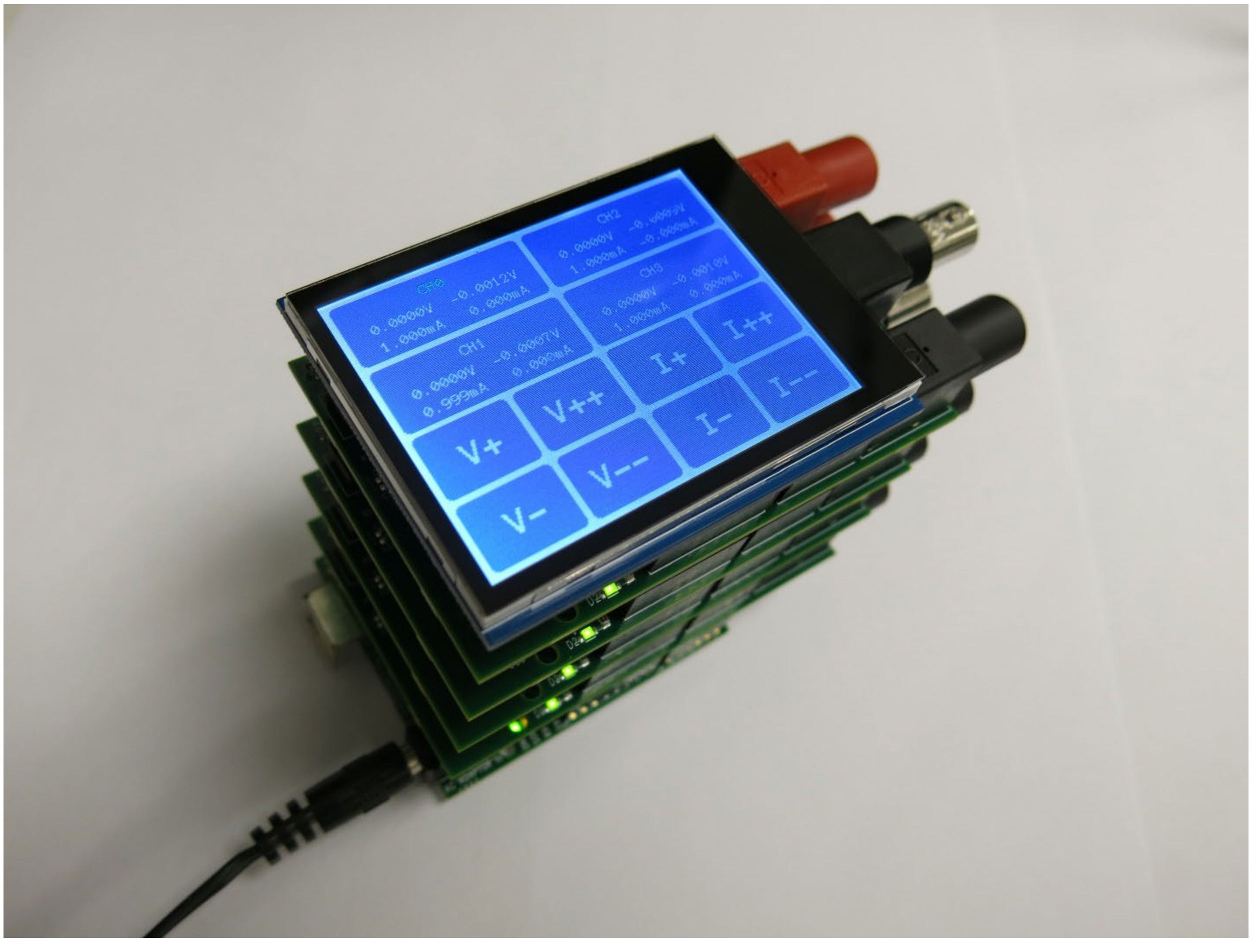
EasySMU SET CURRENT	EasySMU CURRENT MEASUREMENT ERROR[2]
40mA	±10µA
10mA	±2µA
5mA	±2µA
1mA	±1µA

[1] The EasySMU voltage measurement is tested at –12V, –5V, 0V, 5V, and 12V. The measurement error is tested with an Agilent HP34401A 6.5 digit voltmeter. Although the output voltage setting is configurable with <1mV step sizes, it is recommended to use the voltage measurement to accurately determine the actual output voltage.

[2] The current can be measured accurately to the microamp level, but the current limit setting is only configurable between 1mA to 40mA. The current measurement is tested with output voltage settings of 12V and –12V while the output is shorted to ground through the Agilent HP34401A current meter.

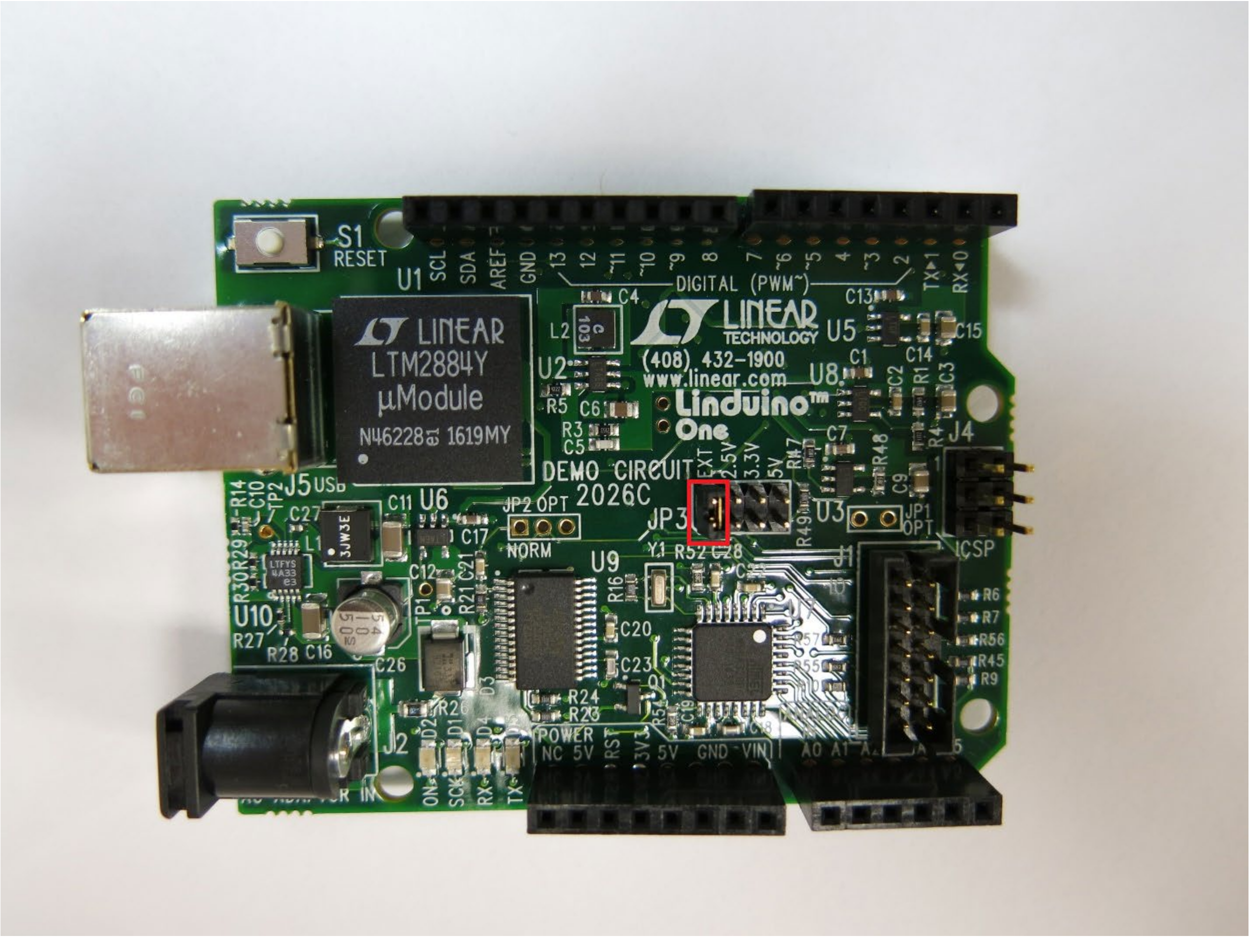
QUICK START PROCEDURE

The simplest way to use the EasySMU is to provide power through the Linduino's 12V input and control it with an Adafruit Capacitive Touchscreen (https://www.adafruit.com/products/1947) as shown in the photo below. Up to eight EasySMUs can be powered from a single 12V/1A wall adapter. Good choices for the AC/DC wall adapter are a Jameco ReliaPro 100870 or a CUI Inc. SW12-12-N-P5. When adding or removing EasySMUs from the Linduino, it is recommended to first remove power by disconnecting the AC/DC wall adapter and USB cable from the Linduino.


CH0
0.0000V -0.0012V
1.000mA 0.000mA
CH1
0.0000V -0.0007V
0.999mA 0.000mA
CH2
0.0000V -0.0009V
1.000mA -0.000mA
CH3
0.0000V -0.0010V
1.000mA 0.000mA
V+
V++
I+
I++
V-
V--
I-
I--

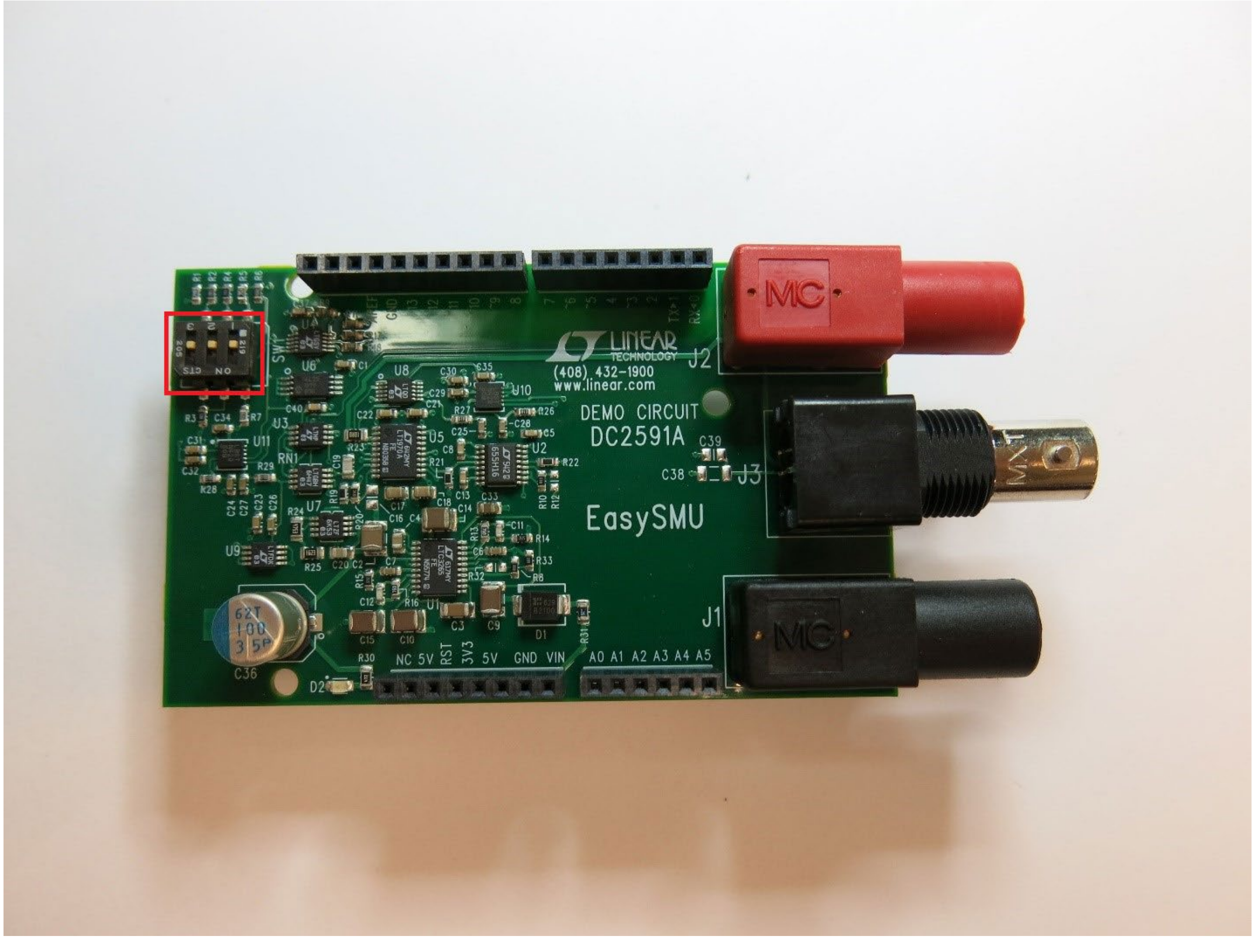
QUICK START PROCEDURE

It is recommended to set the Linduino JP3 jumper to the EXT position when using the EasySMU shield. The QuikEval™ connector is not used by the EasySMU, so eliminating the fast edges generated by the Linduino's I^2C and SPI digital buffers reduces noise that could be coupled from the fast signal edges.



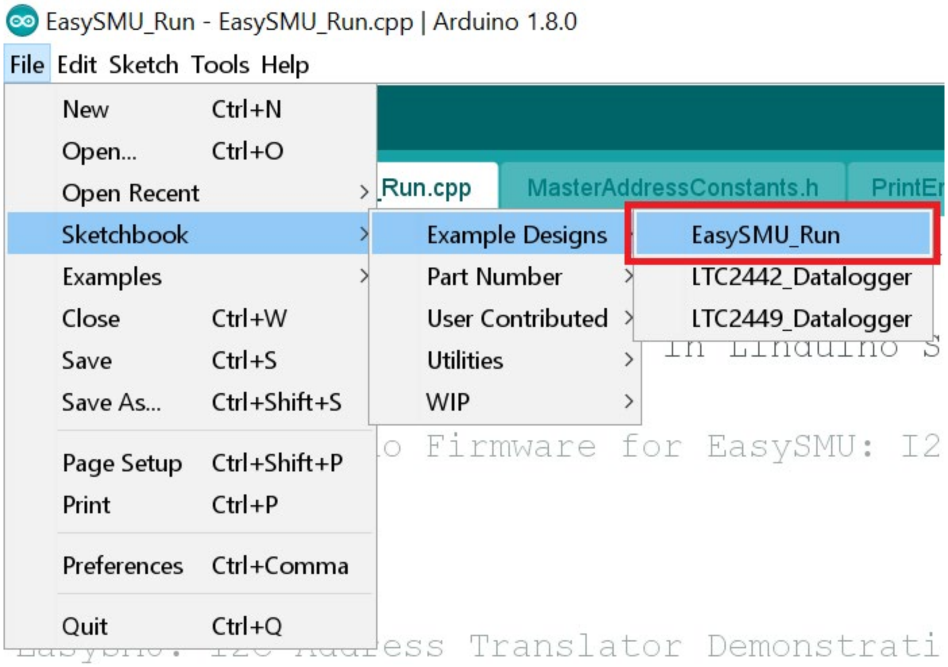
QUICK START PROCEDURE

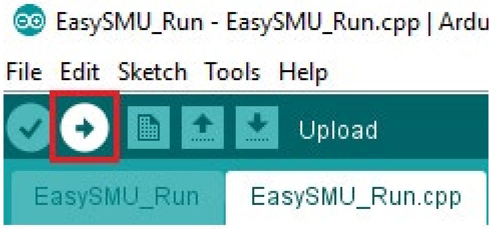
Up to four EasySMU channels (CH0-CH3) can be controlled directly from the touchscreen, and up to eight (CH0-CH7) can be controlled through the USB port. When multiple channels are present, configure the DIP switches to assign a unique number to each EasySMU. Since the optional touchscreen displays channels CH0-CH3, it is easiest to assign channel numbers starting with 0 at the bottom and increasing by one for each additional channel. The DIP switch setting is only checked when power is first applied to the EasySMU. Therefore, if a DIP switch setting is changed while the EasySMU is powered it will not be updated until the 12V power input and USB cable have been removed and power is reapplied.



QUICK START PROCEDURE

If this is your first time using a Linduino, see the Quick Start instructions at http://www.linear.com/solutions/Linduino to install the Arduino IDE and download the LTsketchbook. Use the Arduino IDE to upload the EasySMU_Run sketch. This is required before using the EasySMU for the first time.

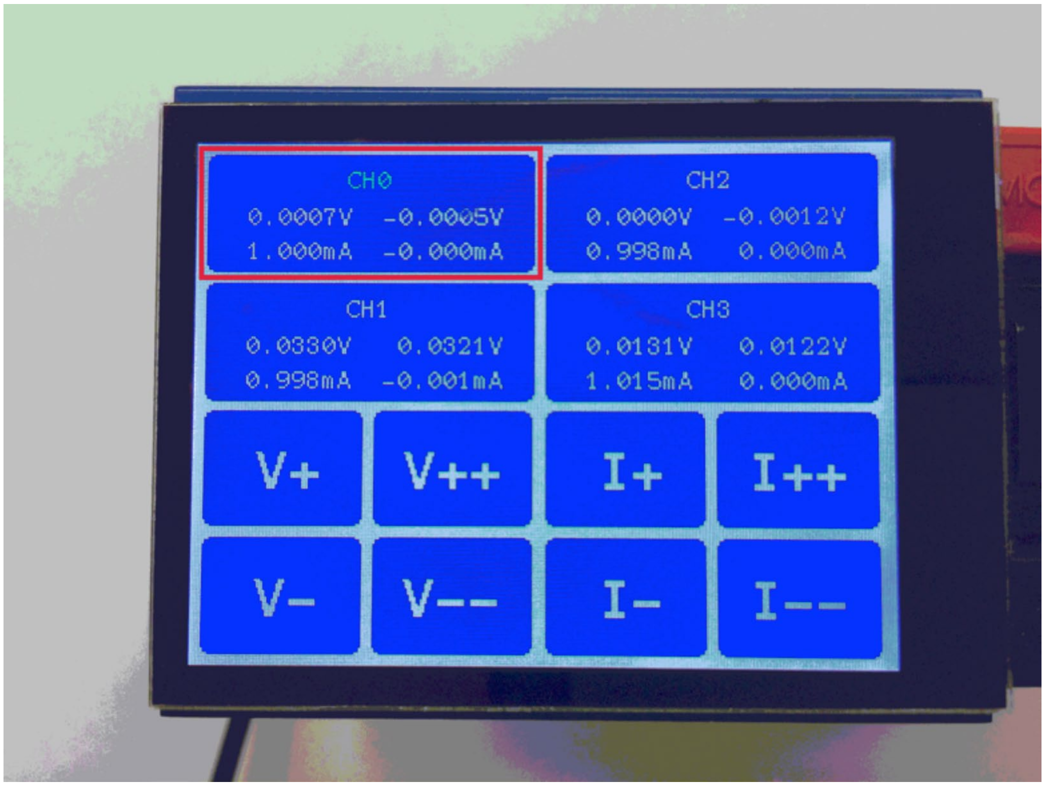

EasySMU_Run - EasySMU_Run.cpp | Arduino 1.8.0
File Edit Sketch Tools Help
New Ctrl+N
Open... Ctrl+O
Open Recent
Sketchbook
Examples
Close Ctrl+W
Save Ctrl+S
Save As... Ctrl+Shift+S
Page Setup Ctrl+Shift+P
Print Ctrl+P
Preferences Ctrl+Comma
Quit Ctrl+Q
Run.cpp
MasterAddressConstants.h
PrintEr
Example Designs
Part Number
User Contributed
Utilities
WIP
EasySMU_Run
LTC2442_Datalogger
LTC2449_Datalogger
In Linduino S
o Firmware for EasySMU: I2
EasySMU: I2C Address Translator Demonstrati


EasySMU_Run - EasySMU_Run.cpp | Ardu
File Edit Sketch Tools Help
Upload
EasySMU_Run
EasySMU_Run.cpp

QUICK START PROCEDURE

If the touchscreen is not used, skip ahead to the section entitled USB operation.

When the touchscreen is present, press a measurement box to select the corresponding channel. The label of the selected channel is displayed in green. The labels of unselected channels are white.



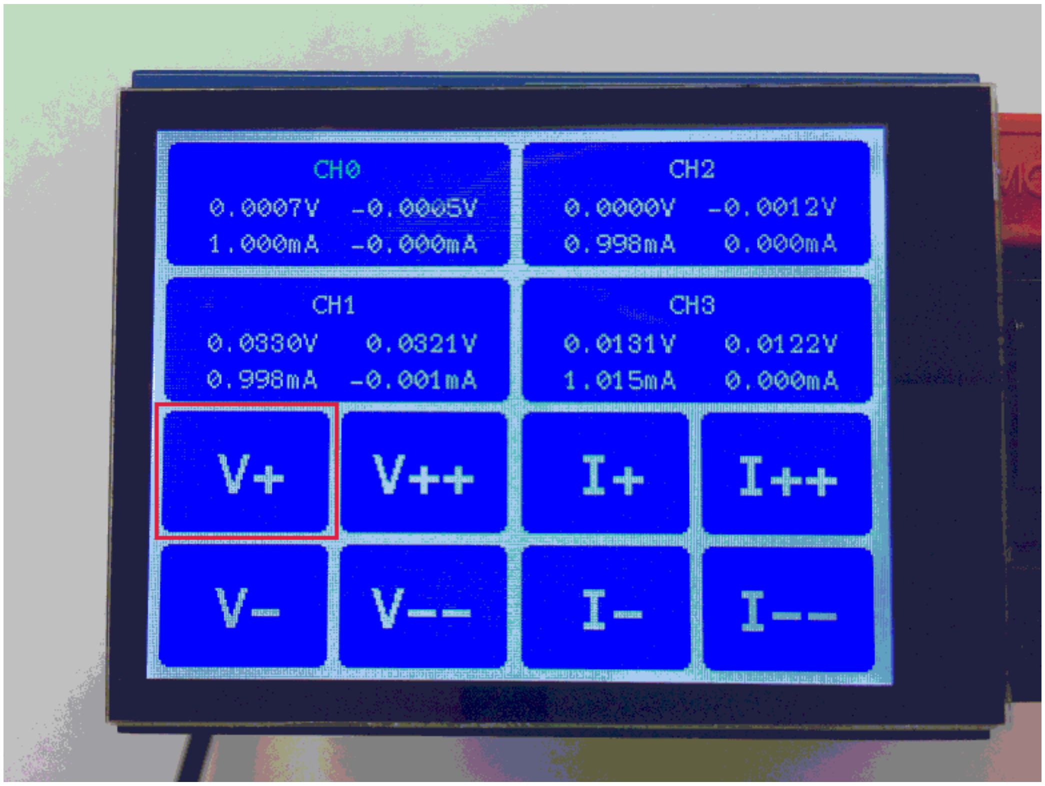
```
         CH0                        CH2
0.0007V   -0.0005V         0.0000V   -0.0012V
1.000mA   -0.000mA         0.998mA    0.000mA

         CH1                        CH3
0.0330V    0.0321V         0.0131V    0.0122V
0.998mA   -0.001mA         1.015mA    0.000mA
```

QUICK START PROCEDURE

The V+, V++, V–, V– –, I+, I++, I–, and I– – buttons adjust the output voltage and current of the selected channel.

The values on the left side of the measurement box are the voltage and current source settings. In other words, the left side shows the voltage limit and current limit configurations. The values on the right side of the box are the actual measured values at the output.



```
        CH0                          CH2
0.0007V   -0.0005V         0.0000V   -0.0012V
1.000mA   -0.000mA         0.998mA    0.000mA

        CH1                          CH3
0.0330V    0.0321V         0.0131V    0.0122V
0.998mA   -0.001mA         1.015mA    0.000mA
```

USB OPERATION

The USB port on the Linduino appears as a virtual COM port on the PC, allowing an EasySMU to be controlled with the serial commands listed below. The baud rate is 9600bps, and the serial port configuration is 8-N-1 (data bits: 8, parity: none, stop bit: 1).

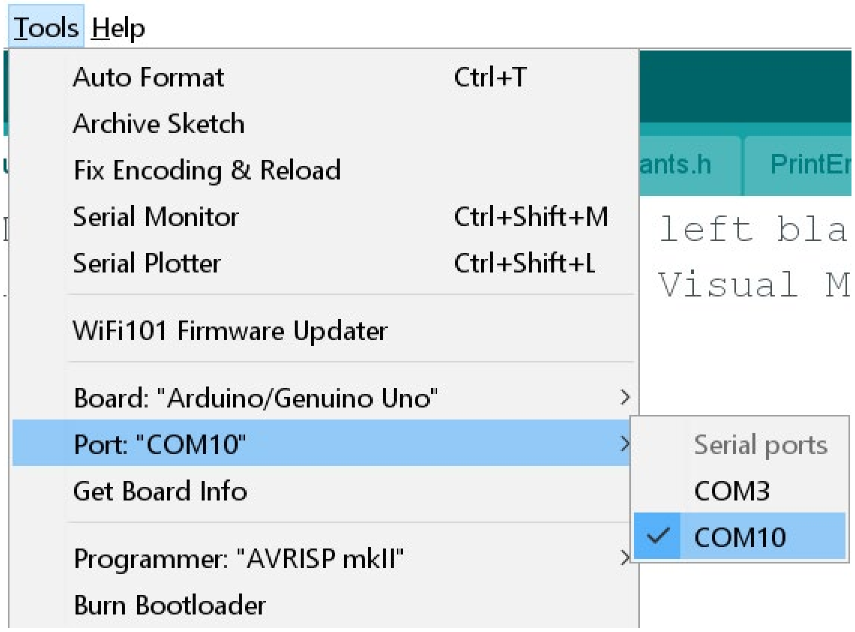
(If you have a Windows version of Excel, the EasySMU.xls spreadsheet available for download at www.linear.com/demo/DC2591A provides another simple way to set and measure the voltage and current of EasySMUs.)

In the commands below, x is substituted with 0-7, a number corresponding to the appropriate channel.

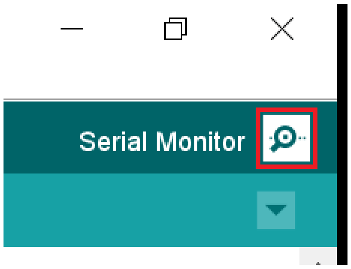
COMMAND	DESCRIPTION
CHx:VOL value	Set the output voltage to value in volts
CHx:CUR value	Set the output current to value in amps. (If value is preceded by + or – it will force source or sink only operation.)
CHx:MEA:VOL	Returns the measured output voltage in volts.
CHx:MEA:CUR	Returns the measured output current in amps.
*RST	Reset to power-up state
*IDN or *IDN?	Return ID string that includes revision, channels that are present, serial number of each channel, etc.
LCD:ENA	Enable the LCD/TFT display (default)
LCD:DIS	Disable the LCD/TFT display. This is sometimes useful to reduce noise at the output caused by SPI communication with the screen.
CHx:DIS	Disable the output. This configures the output to a relatively high impedance state.
CHx:ENA	Enable the channel. (Default state)
CHx:CAL:SET	Calibration routine. (Factory use only. Disabled by default.)
CHx:CAL:RES	Restore factory calibration. (Only useful if the user has overwritten the calibration, which is not possible without editing the firmware.)

USB OPERATION

Any terminal software may be used to communicate with the EasySMU. The following example uses the Arduino IDE's serial monitor. Start by configuring the terminal for the appropriate serial port from the Tools→Port menu. In the example below, COM10 is selected.

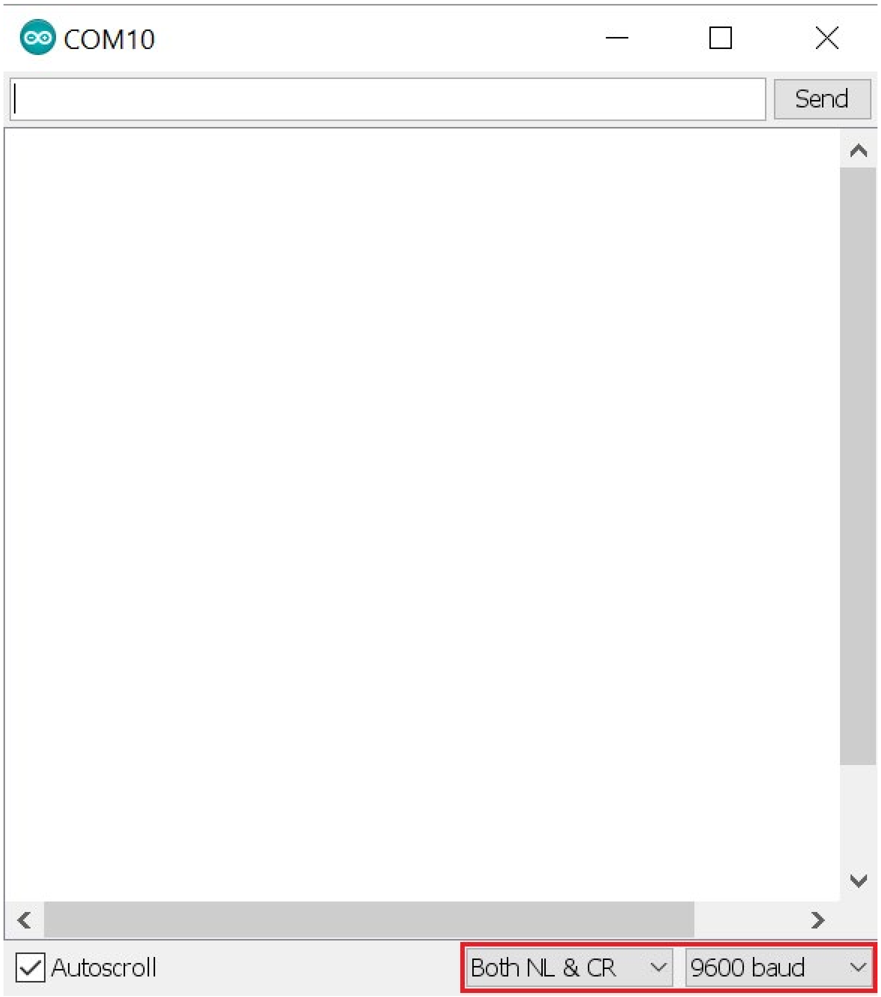

Tools
Help
Auto Format Ctrl+T
Archive Sketch
Fix Encoding & Reload
Serial Monitor Ctrl+Shift+M
Serial Plotter Ctrl+Shift+L
WiFi101 Firmware Updater
Board: "Arduino/Genuino Uno"
Port: "COM10"
Get Board Info
Programmer: "AVRISP mkII"
Burn Bootloader
Serial ports
COM3
✓ COM10
ants.h
PrintEr
left bla
Visual M

Open the serial monitor by clicking on the magnifying glass icon in the upper right corner of the Arduino IDE.


Serial Monitor

USB OPERATION

Then, when the serial monitor window opens, be sure the drop-down menus in the bottom right corner are configured to a baud rate of 9600 and the line terminator is set to Both NL & CR.

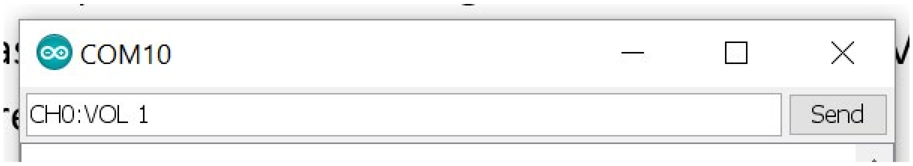

COM10
Send
☑ Autoscroll
Both NL & CR
9600 baud

USB OPERATION

Now, if you would like to set CH0's output to 1.00V, type:

CH0:VOL 1

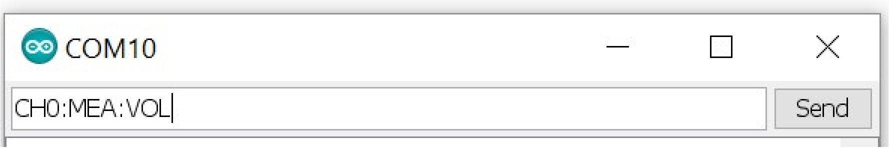
and press Send.



```
CH0:VOL 1
```

The terminal responds with the voltage value that has been set, and the voltage on the output changes. In this case, CH0's output will be configured to 1.0000V.

The actual voltage measured at the output can be read with the CH0:MEA:VOL command.



```
CH0:MEA:VOL
```

On this EasySMU, the response is 0.9977. The voltage measurement is more accurate than the setting value, so it can be concluded that the output voltage is 0.9977V.

The current limit can be configured in a similar manner by sending:

CH0:CUR 0.005

This example sets the output current limit to 5mA. With this configuration, the EasySMU sources or sinks a maximum of 5mA. (If the load on the EasySMU output sinks or sources less than 5mA, the output will be driven to the configured output voltage.) Note that the minimum current limit is 1mA. Current limit values below 1mA will exhibit a significant error. In fact, when the current limit is configured to a value less than 0.6mA, the EasySMU will instead current limit to a value between 0.4mA and 0.6mA.

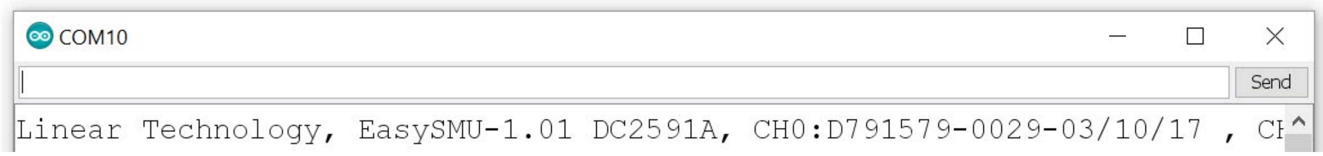
The actual current at the output of CH0 may be read using the following command:

CH0:MEA:CUR

USB OPERATION

The measurement value is accurate to the microamp level, and the minimum current limit value of 1mA does not influence the measurement accuracy.

The *IDN? Command is useful for determining information about the EasySMUs that are connected, including the serial number of each channel which matches a sticker affixed to the bottom of the EasySMU.



```
Linear Technology, EasySMU-1.01 DC2591A, CH0:D791579-0029-03/10/17 , CH
```

LTC4316 I²C ADDRESS TRANSLATOR

The EasySMU demonstrates how the LTC4316 I²C address translator solves addressing problems in complex I²C systems. Each EasySMU channel (shield) contains four I²C components: two LTC2485 analog-to-digital converters, an LTC2655 quad digital-to-analog converter, and a 24LC025 I²C serial EEPROM memory. Communicating with eight EasySMU channels using one I²C bus would be impossible without the LTC4316 address translator (or an I²C addressable multiplexer). Consider that an eight channel EasySMU configuration has 16 LTC2485's. Without the LTC4316, each LTC2485 can be configured to one of only six I²C addresses, far fewer than the 16 addresses required.

In this demonstration, all EasySMUs are identical except for the setting of a user configurable DIP switch. Each EasySMU contains an LTC4316 address translator, and based on the DIP switch setting, the I²C addresses are translated to new addresses in real-time before they are received by the EasySMU's I²C components. As a result, the I²C master (in this case a Linduino) communicates with every I²C component in the system using a unique I²C address.

Although this demonstration relies on the user to configure a unique DIP switch setting for each EasySMU, a typical system does not require any user intervention. In systems with backplane connectors, one or two pins of each connector are dedicated to resistive dividers that reside on the backplane and configure the XORL and XORH pins of the LTC4316. As a result, each card inserted in the backplane responds to unique I²C addresses based on the slot location (and a resistive divider).

VOLTAGE SOURCE

At its core, the EasySMU is built around the LT1970A power op amp with adjustable precision current limit. When it is not current limiting, the LT1970A behaves as a power op amp with its output voltage configured by feedback resistors and an input source. In the EasySMU, the input source is provided by an LTC2655B-H16 quad I^2C 16-bit digital-to-analog converter which has a full-scale output voltage of 4.096V. The DAC output drives the noninverting input of the LT1970A directly. An LT5400-3 matched 10k/100k resistor network provides the feedback to the inverting terminal of the LT1970A with one end of the divider tied to the LT1970A's output and the other end tied to the 2.048V output reference voltage of the LTC2655B-H16, buffered by an LTC2051 op amp. The resulting circuit drives 2.048V at the output when the DAC output is 2.048V, or mid-scale. As the DAC output increases or decreases, the output moves with a gain of 10, as configured by the LT5400-3's 100k/10k resistive divider.

Since the LT1970A power dissipation varies based on loading and output settings, most discrete resistors would exhibit mismatch as the PCB temperature gradients change. The LT5400-3 matched resistor network eliminates this mismatch.

CURRENT LIMIT

The LT1970A's stand out feature is the simple manner in which its current limit can be adjusted on the fly. The voltages at the LT1970A VCSRC and VCSNK pins configure the output source and sink current limits respectively, in conjunction with an external current sense resistor. The LT1970A divides the voltage at the VCSRC and VCSNK pins by 10 to configure the maximum voltage across the sense resistor before current limit is invoked.

Two channels of the quad LTC2655B-H16 digital-to-analog converter configure the EasySMU source and sink current. Because the LTC2655B-H16 has a full-scale voltage of 4.096V, the maximum configurable voltage across the current sense resistor is 4.096V/10 or 409.6mV. The EasySMU's current sense resistor value of 10Ω results in a full-scale current limit of roughly 40mA. The LT1970A's minimum configurable voltage across the sense resistor is guaranteed to be at least 10mV, setting the lower end of the current limit range. As a result, a 1mA current limit is guaranteed, but the EasySMU allows the current limit setting to be configured as low as 0.6mA.

VOLTAGE MEASUREMENT

The EasySMU provides an accurate measurement of the output voltage using an LTC2485 I^2C ΔΣ analog-to-digital converter. In this circuit, the LTC2485's REF^- pin is tied to GND, and the REF^+ pin is set at 3.3V by an LTC6655-3.3 low noise, low drift precision reference. A 10k/100k resistive divider in the LT5400-3 quad matched resistor network is connected between the output of the LT1970A and the 3.3V reference, with the middle of the divider tied to the IN^+ pin of the LTC2485. The IN^- pin of the LTC2485 is connected to the 3.3V reference. The result is that the LTC2485's differential voltage measurement between IN^+ and IN^- pins remains inside of the GND and V_{CC} = 5V power supply range, while measuring voltages that range between 12V and –12V. To understand the operation intuitively, consider when the output voltage is 3.3V. The IN^+ and IN^- pins are equal to 3.3V, and the LTC2485 measures 0V differential voltage. When the output moves away from 3.3V, the differential measurement reflects the output voltage divided by 10k/(100k+10k) = 1/11. To reduce errors caused by the input sampling current of the LTC2485 interacting with the high impedance of the resistive divider, an LTC2051 op amp in a unity gain configuration buffers the IN^+ input of the LTC2485.

CURRENT MEASUREMENT

The output current measurement is implemented with an LT1991 precision gain selectable amplifier and another LTC2485 analog-to-digital converter. The LT1991 is configured so that its accurate internal matched resistors produce a gain of 3V/V from the differential voltage across the 10Ω current sense resistor to the output voltage of the amplifier. Because the LT1991's REF pin is tied to the 3.3V reference, the output voltage of the LT1991 is at 3.3V when there is no current through the current sense resistor. When voltage is present across the current sense resistor, the LT1991's output moves above or below 3.3V with a gain of 3V/V. The output of the LT1991 is connected to IN^+ of the LTC2485 analog-to-digitial converter while IN^- pin is connected to the 3.3V reference. As a result, the differential voltage sensed across the IN^+ and IN^- pins of the LTC2485 is zero when the voltage across the sense resistor is zero.

POWER SUPPLIES

An LTC3265 creates 15V and –15V supplies from the single 12V AC adapter input. The LTC3265 creates the positive and negative supplies using capacitive charge pumps, which it then post regulates using positive and negative low dropout regulators. The post regulation removes the ripple voltage present on the charge pump outputs, and as a result the output supplies are very low noise.

The 5V supplies used throughout the EasySMU are generated by an LT3010 low dropout linear regulator whose input supply is generated directly from the 12V input.

CALIBRATION

A 24LC025 I^{2}C serial EEPROM on each EasySMU board stores calibration information.

As you might have noticed in the above description of the current measurement, the feedback resistors and the voltage sensing resistive divider create a small current in the 10Ω current sense resistor even when no current is delivered to the output. This current is measured during the factory calibration routine and is compensated for in the EasySMU firmware as a function of the output voltage.

In addition, the voltage sense and current sense LSB weight and offset are measured during this calibration, and are used by the EasySMU firmware on the Linduino.

The EEPROM is also programmed with a unique serial number returned by the *IDN? serial command.

TROUBLESHOOTING

The EasySMU resets every 15 seconds when the USB cable is connected.

If you have Keysight IO Libraries Suite version 16.4 or later, it autoscans all available ports every 15 seconds, resetting the connected equipment. As of the time of this was written, there is not an option to disable this feature. It also causes the similar problems with other commercial lab equipment. If it is necessary to install the Keysight IO Libraries Suite, downgrade to version 16.3 which is available from the following link:

http://www.keysight.com/main/software.jspx?cc=US&lc=eng&nid=-33330.977662&id=2175637&pageMode=PV

EasySMU does not respond to serial commands.

Begin by confirming that you are communicating with the correct COM port. Connect the Linduino beneath the EasySMU shield to the PC using a USB cable. Open the Arduino IDE, and look at the list of COM ports under the Tools→Ports menu. Unplug the USB cable, and again select Tools→Ports. The port that is now missing from the list is the COM port assigned to the EasySMU on your PC. Plug the USB cable in once more, and select the COM port in the Tools→Ports menu. Then, open the serial terminal by selecting Tools→Serial Monitor. Type *IDN? into the terminal and you should see a response string similar to the following.

Linear Technology, EasySMU-1.01 DC2591A, CH0:D727578-0002, CH1:D727578-0007, CH2:SD727578-0004, CH3:D727578-0020

(There are four EasySMU channels in this example, configured as CH0-CH3 with the DIP switches.)

If you do not receive this response, you have probably forgotten to upload the EasySMU firmware into the Linduino. From the Arduino IDE select File→Sketchbook→Example Designs→EasySMU_Run. Then, select Sketch→Upload to upload the firmware. You only need to do this the first time you use the EasySMU.

DEMONSTRATION BOARD IMPORTANT NOTICE

Linear Technology Corporation (LTC) provides the enclosed product(s) under the following **AS IS** conditions:

This demonstration board (DEMO BOARD) kit being sold or provided by Linear Technology is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not provided by LTC for commercial use. As such, the DEMO BOARD herein may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including but not limited to product safety measures typically found in finished commercial goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may or may not meet the technical requirements of the directive, or other regulations.

If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

No License is granted under any patent right or other intellectual property whatsoever. **LTC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind.**

LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

Copyright © 2004, Linear Technology Corporation

© LINEAR TECHNOLOGY CORPORATION 2017

DEMO MANUAL DC2132A

LT3081, LT8612, LT3092 24V 3A Constant Voltage, Constant Current Bench Supply

DESCRIPTION

DC2132A is a 24V 3A constant voltage, constant current bench supply. It regulates any output voltage from 0V to 24V and any output current from 0A to 3A. It runs from 10V to 40V input although the output voltage should remain 5V or more below the input voltage.

The LT®8612 step-down regulator is followed by two parallel LT®3081 linear regulators for a combination of low output ripple, high bandwidth and easy-to-adjust output voltage and current limits. The LT8612 is configured in pulse-skipping operation and its output voltage is regulated to roughly 1.7V above the output voltage of the LT3081. The LT3081 SET and I_{LIM} pins are connected to potentiometers that act as adjustable knobs on the PCB for voltage and current limit respectively.

The LT®3092 current source is used to deliver current to power the adjustable resistance of the voltage limit knob (potentiometer). That voltage directly sets the output voltage of the LT3081. The maximum output voltage can be set to three settings: 24V, 15V and 5.5V with the shunt position on JP1. The setting should be changed according to the choice of input voltage. A 36V, 24V, or 12V AC/DC converter can be used to power this supply (as well as any DC voltage between 10V and 40V.) If input voltage limits maximum output voltage, then it is recommended to adjust the maximum output voltage to get the full range of the adjustment knob for best resolution.

DC2132A operates to 0V and 0A. It is short-circuit proof. With very small output capacitance, the short-circuit spike is hundreds of times shorter in duration than commonly used and expensive laboratory bench power supplies. With the LT3081s in parallel on the output of this supply, small output capacitance makes this possible. Only 30µF is needed on the output of each LT3081. The LT3081 provides very low output ripple and short-circuit robustness.

An ON/OFF switch turns the converter and its components on and off. A green indicator LED tells if the circuit is on or not. Two TEMP turrets and an I_{MON} turret provide readouts of the LT3081 IC temperatures and the bench supply output current.

The LT3081, LT8612, and LT3092 data sheets give complete descriptions of the devices, operation and applications information. The data sheet must be read in conjunction with this demo manual for DC2132A. The LT3081ER is assembled in a 7-lead plastic DD (R) package with a thermally enhanced V_{OUT} tab and with θ_{JA} = 15ºC/W. Proper board layout is essential for maximum thermal performance. See the the Layout Considerations section in the data sheet.

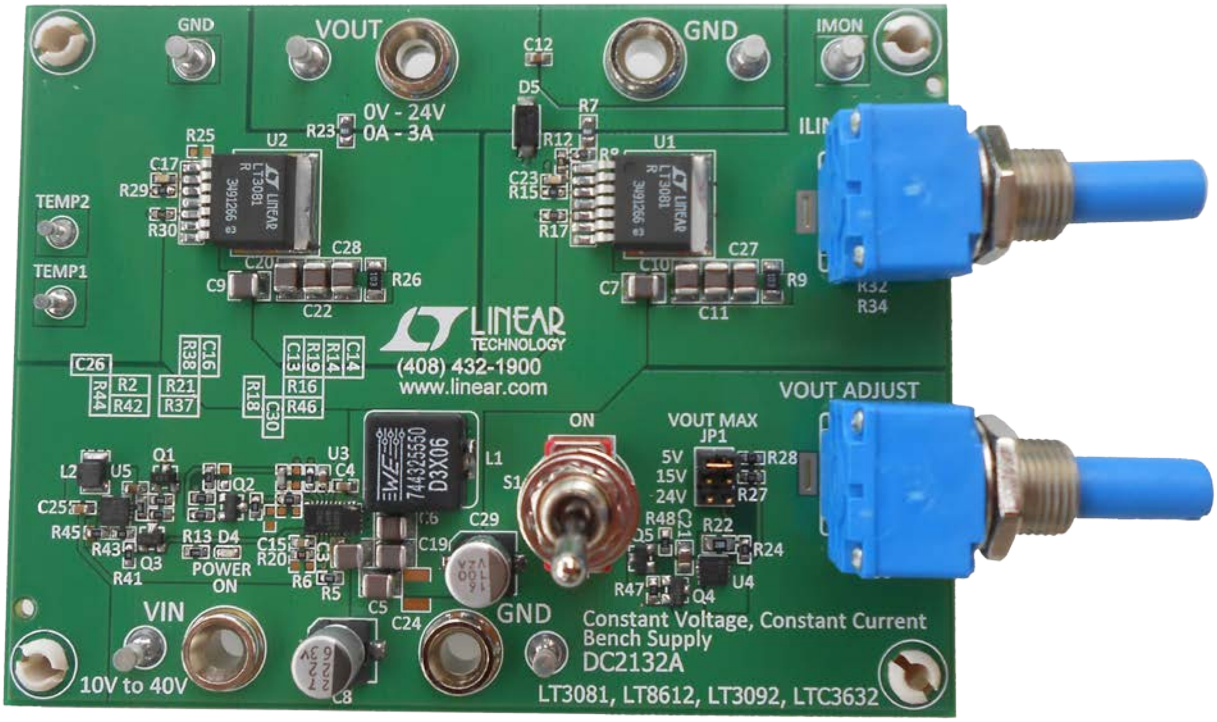
Design files for this circuit board are available at http://www.linear.com/demo/DC2132A

, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

PERFORMANCE SUMMARY Specifications are at $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Input Voltage Range		10		40	V
LT8612 Switching Frequency	R20 = 60.4k		700		kHz
V_{OUT} Range (Set by V_{LIMIT})	V_{IN} = 36V, JP1 Set to 24V	0		25	V
I_{OUT} Range (Set by I_{LIMIT})		0		3.1	A
Quiescent Current	V_{IN} = 36V V_{OUT} = 24V, No Load		31		mA
Typical Efficiency with 3A Output	V_{IN} = 36V, V_{OUT} = 24V V_{IN} = 12V, V_{OUT} = 5V V_{IN} = 12V, V_{OUT} = 3.3V		90 71 62		% % %
LT3081 Input-to-Output Voltage Drop	R37 = 1.00k, R21 = R38 = 100k, R18 = 4.99k		1.7		V
V_{OUT} AC Ripple	V_{IN} = 36V, V_{OUT} = 24V, I_{OUT} = 3.0A		~10		mV_{P-P}
Minimum Load		0			mA

BOARD PHOTO


GND
VOUT
GND
IMON
0V - 24V
0A - 3A
TEMP2
TEMP1
LINEAR TECHNOLOGY
(408) 432-1900
www.linear.com
VOUT ADJUST
VOUT MAX
JP1
5V
15V
24V
ON
POWER ON
VIN
10V to 40V
GND
Constant Voltage, Constant Current
Bench Supply
DC2132A
LT3081, LT8612, LT3092, LTC3632

QUICK START PROCEDURE

DC2132A is easy to set up to evaluate the performance of the LT3081 and LT8612. Follow the procedure below:

1. Set the ON/OFF switch to OFF to disable switching.
2. With power off, connect the input power supply to the V_{IN} and GND terminals. Make sure that the V_{IN} DC input voltage will not exceed 40V. Be careful for hot plug transients above 40V.
3. The DC2132A bench supply is robust and can be turned on with or without a load. If the load is too big, DC2132A will limit its output. If there is a short-circuit on the output, DC2132A will run through the short safely and will limit its current to its I_{LIMIT} setting.
4. Observe the output voltage and current as well as the temperature of the ICs.

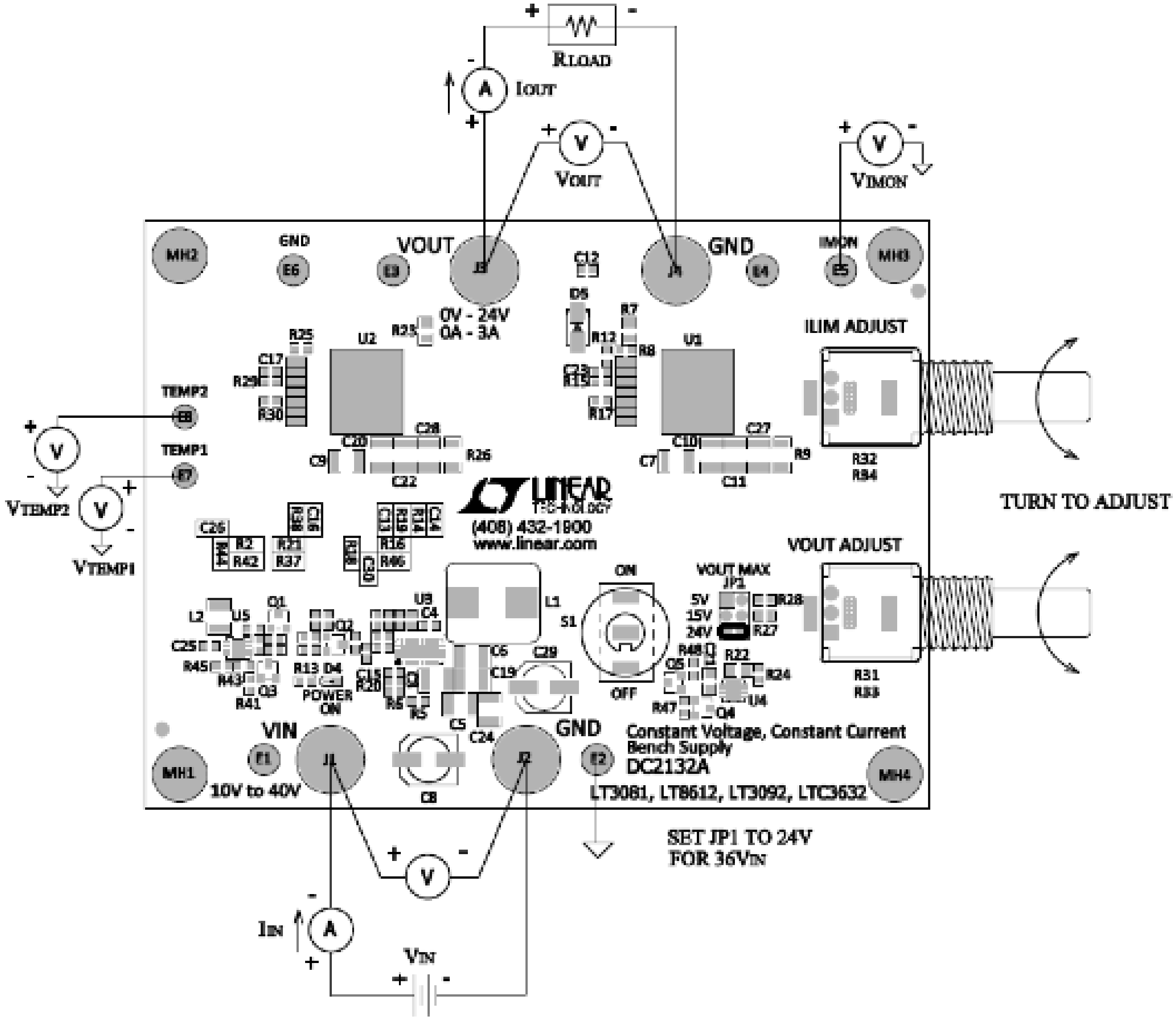
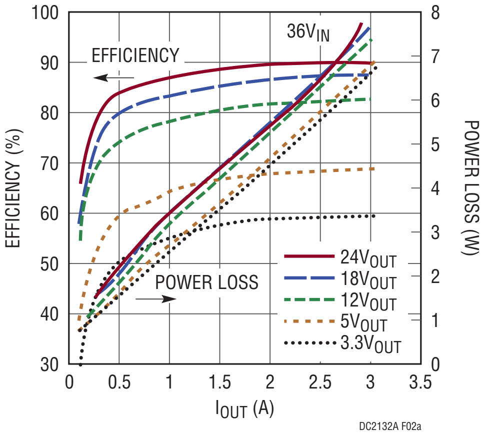

RLOAD
IOUT
VOUT
VIMON
TEMP2
TEMP1
VTEMP2
VTEMP1
GND
VOUT
GND
IMON
0V - 24V
0A - 3A
ILIM ADJUST
TURN TO ADJUST
VOUT ADJUST
VOUT MAX
JP1
5V
15V
24V
ON
OFF
S1
POWER ON
(408) 432-1900
www.linear.com
VIN
10V to 40V
GND
Constant Voltage, Constant Current Bench Supply
DC2132A
LT3081, LT8612, LT3092, LTC3632
SET JP1 TO 24V FOR 36VIN
IIN
VIN

Figure 1. Test Procedure Setup Drawing for DC2132A

QUICK START PROCEDURE



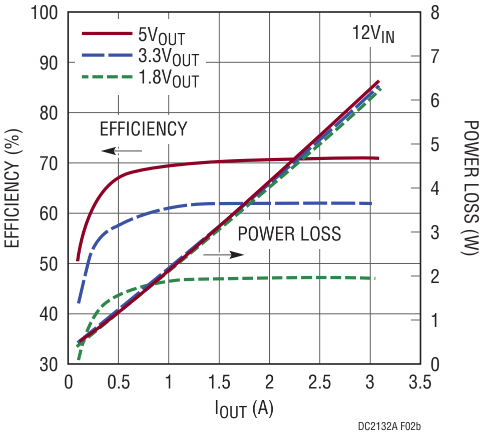


Figure 2. DC2132A Efficiency and Power Loss at Different Voltage and Current

QUICK START PROCEDURE

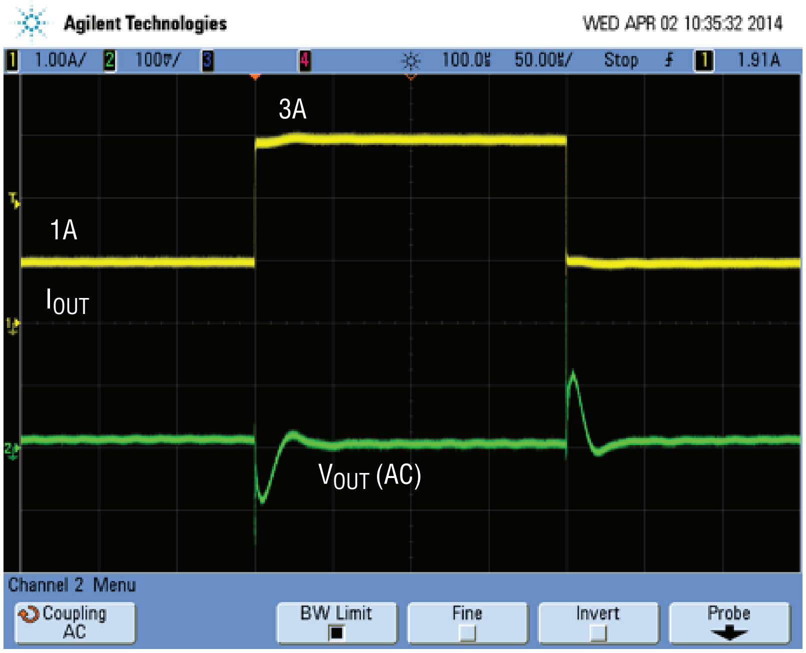


Figure 3. DC2132A 1A to 3A Transient Response $36V_{IN}$, $24V_{OUT}$

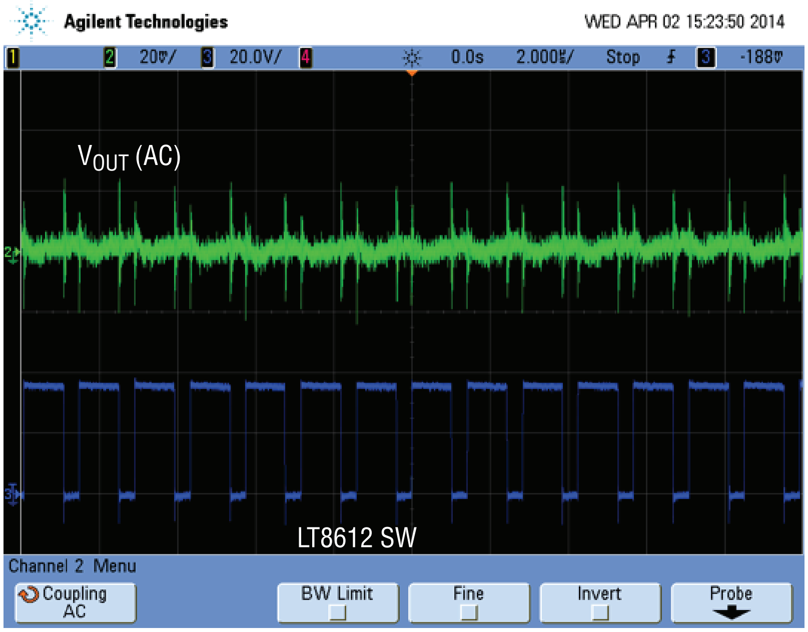


Figure 4. DC2132A Output Voltage Ripple

QUICK START PROCEDURE

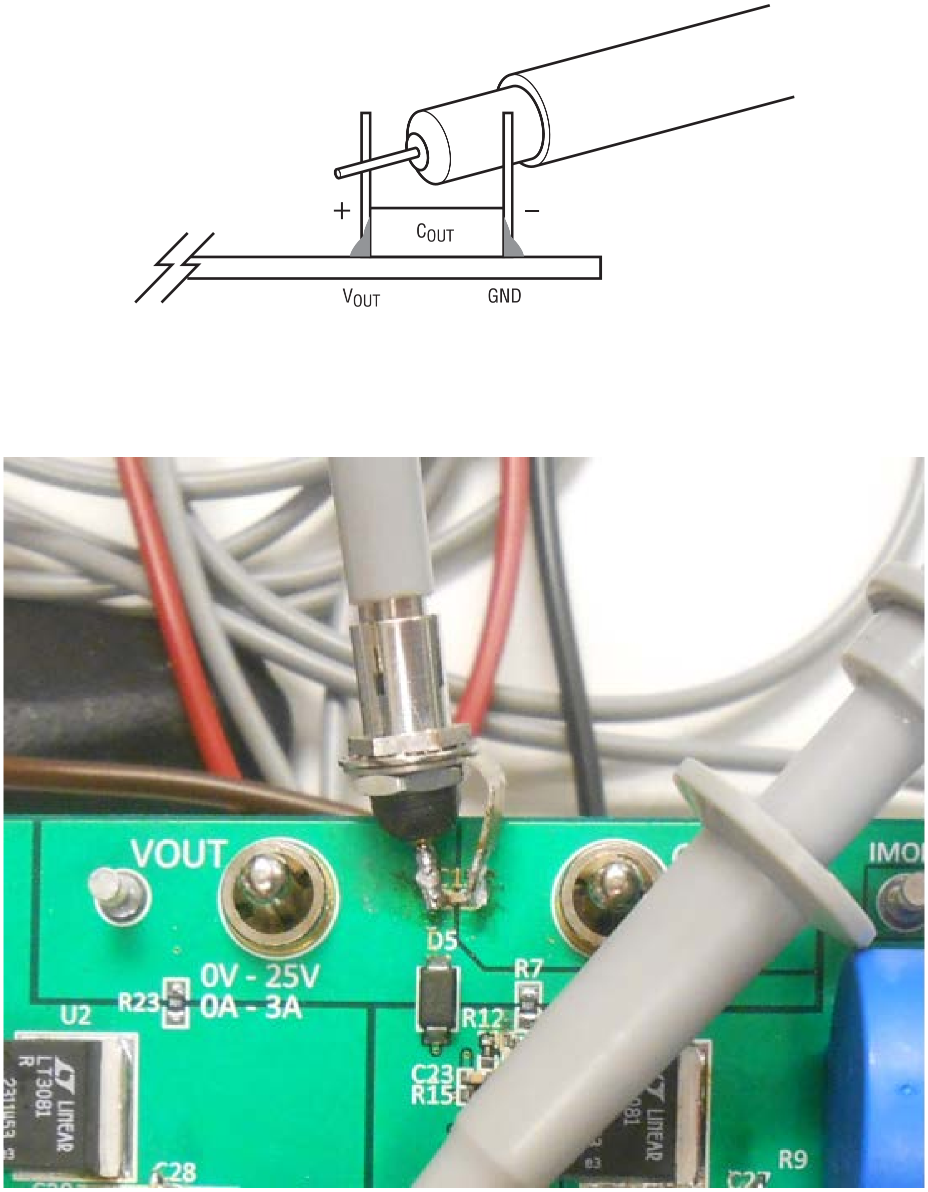

+
–
C_{OUT}
V_{OUT}
GND
VOUT
0V - 25V
0A - 3A
U2
R23
D5
R7
R12
C23
R15
LT3081
LINEAR
C28
R9
C27
IMO

Figure 5. DC2132A Output Voltage Ripple Measurement Method

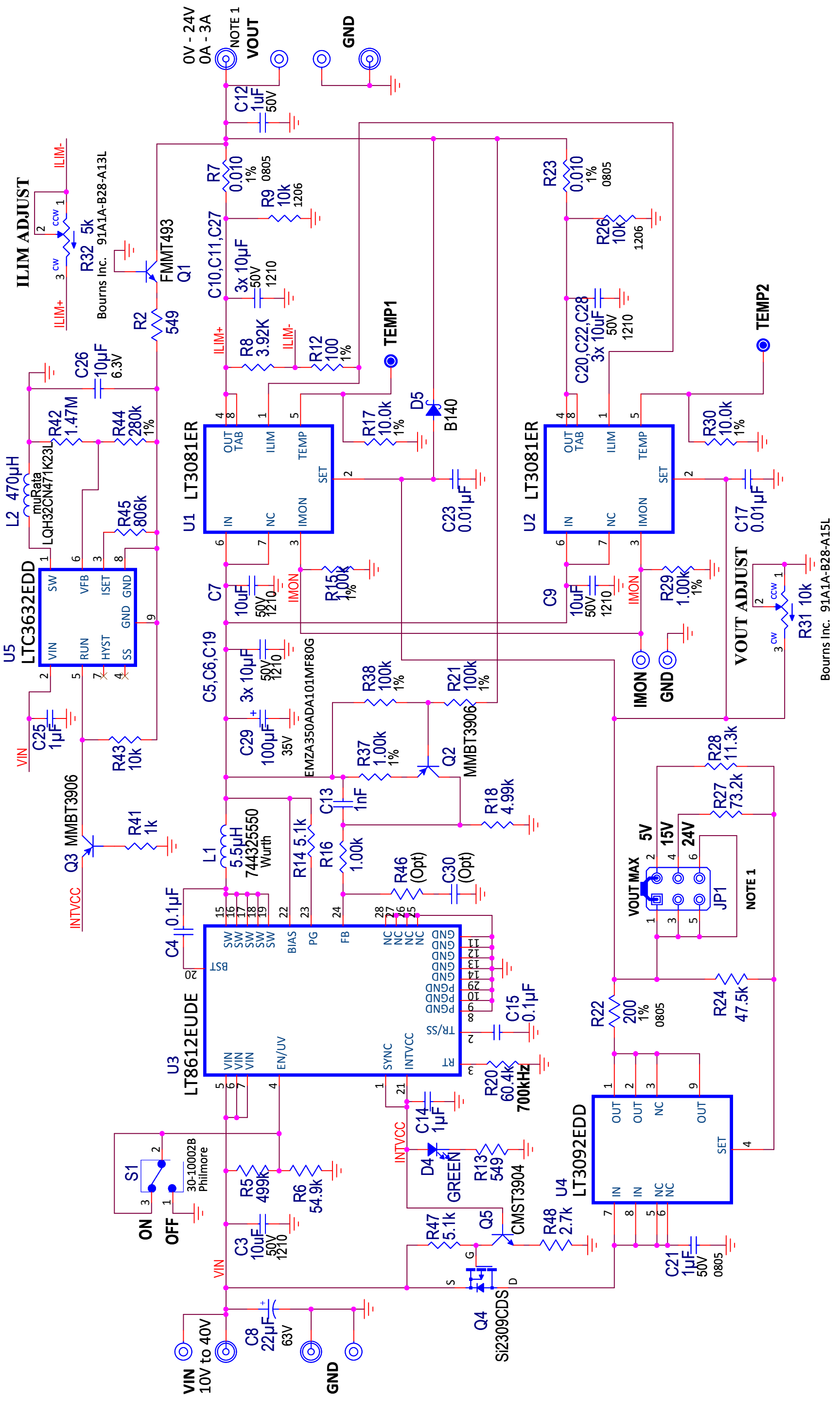
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	12	C3, C5, C6, C7, C9, C10, C11, C19, C20, C22, C27, C28	CAP., X5R 10µF 50V 20% 1210	TAIYO YUDEN UMK325BJ106MM-T
2	1	C4	CAP., X5R 0.1µF 50V 10% 0603	TDK C1608X5R1H104K
3	1	C12	CAP., X5R 1µF 50V 10% 0603	TDK C1608X5R1H105K
4	1	C13	CAP., NPO 1nF 25V 5% 0603	AVX 06033A102JAT2A
5	1	C14	CAP., X5R 1µF 25V 10% 0603	TDK C1608X5R1E105K
6	1	C15	CAP., X7R 0.1µF 25V 10% 0603	AVX 06033C104KAT2A
7	2	C17, C23	CAP., X7R 0.01µF 100V 10% 0603	AVX 06031C103KAT2A
8	1	C21	CAP., X7R 1µF 50V 10% 0805	MURATA GRM21BR71H105KA12L
9	1	C25	CAP., X7R 1µF 16V 10% 0603	MURATA GCM188R71C105KA64L
10	1	C26	CAP., X5R 10µF 6.3V 20% 0603	TDK C1608X5R0J106M
11	1	C29	CAP., ALUM. ELECT. 100µF 35V ±20% F80	NIPPON CHEMI-CON EMZA350ADA101MF80G
12	1	D5	SCHOTTKY DIODE, 1A/40V SMA	DIODES/ZETEX B140-13-F
13	1	L1	INDUCTOR, 5.5µH	WÜRTH ELEKTRONIK 744325550
14	1	L2	INDUCTOR, 470µH ±10% 1210	MURATA LQH32CN471K23L
15	1	Q1	TRANSISTOR, NPN SOT-23	DIODES/ZETEX FMMT493TA
16	2	Q2, Q3	TRANSISTOR, PNP SOT-23	DIODES/ZETEX MMBT3906-7-F
17	1	Q4	MOSFET, SINGLE P-CHANNEL 60V SOT-23	VISHAY SI2309CDS-T1-GE3
18	1	Q5	TRANSISTOR, NPN SOT-23	CENTRAL SEMI. CORP. CMST3904TR
19	1	R2	RES., CHIP 549Ω 0.10W 1% 0603	VISHAY CRCW0603549RFKEA
20	1	R5	RES., CHIP 499k 0.10W 1% 0603	VISHAY CRCW0603499KFKEA
21	1	R6	RES., CHIP 54.9k 0.10W 1% 0603	VISHAY CRCW060354K9FKEA
22	2	R7, R23	RES., 0.010Ω 0.125W 1% 0805	VISHAY WSL0805R0100FEA
23	1	R8	RES., CHIP 3.92k 0.10W 1% 0603	VISHAY CRCW06033K92FKEA
24	2	R9, R26	RES., CHIP 10k 0.25W 5% 1206	VISHAY CRCW120610K0JNED
25	1	R12	RES., CHIP 100Ω 0.10W 1% 0603	VISHAY CRCW0603100RFKEA
26	2	R14, R18	RES., CHIP 4.99k 0.10W 1% 0603	VISHAY CRCW06034K99FKEA
27	3	R15, R29, R37	RES., CHIP 1.00k 0.10W 1% 0603	VISHAY CRCW06031K00FKEA
28	2	R17, R30	RES., CHIP 10.0k 0.10W 1% 0603	VISHAY CRCW060310K0FKEA
29	1	R20	RES., CHIP 60.4k 0.10W 1% 0603	VISHAY CRCW060360K4FKEA
30	2	R21, R38	RES., CHIP 100k 0.10W 1% 0603	VISHAY CRCW0603100KFKEA
31	1	R22	RES., CHIP 200Ω 0.125W 1% 0805	VISHAY CRCW0805200RFKEA
32	1	R24	RES., CHIP 47.5k 0.10W 1% 0603	VISHAY CRCW060347K5FKEA
33	1	R27	RES., CHIP 73.2k 0.10W 1% 0603	VISHAY CRCW060373K2FKEA
34	1	R28	RES., CHIP 11.3k 0.10W 1% 0603	VISHAY CRCW060311K3FKEA
35	1	R31	POT. 1 TURN 10k ±10%	BOURNS 91A1A-B28-A15L
36	1	R32	POT. 1 TURN 5k ±10%	BOURNS 91A1A-B28-A13L
37	1	R41	RES., CHIP 1k 0.10W 5% 0603	VISHAY CRCW06031K00JNEA
38	1	R42	RES., CHIP 1.47M 0.10W 1% 0603	VISHAY CRCW06031M47FKEA
39	1	R43	RES., CHIP 10k 0.10W 5% 0603	VISHAY CRCW060310K0JNEA
40	1	R44	RES., CHIP 280k 0.10W 1% 0603	VISHAY CRCW0603280KFKEA

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
41	1	R45	RES., CHIP 806k 0.10W 1% 0603	VISHAY CRCW0603806KFKEA
42	1	R47	RES., CHIP 5.1k 0.10W 5% 0603	VISHAY CRCW06035K10JNEA
43	1	R48	RES., CHIP 2.7k 0.10W 5% 0603	VISHAY CRCW06032K70JNEA
44	2	U1, U2	I.C., LINEAR REGULATOR DD-R (07) (1462-REV F)	LINEAR TECH. CORP. LT3081ER#PBF
45	1	U3	I.C., REGULATOR QFN (28) (UDE) 3mm × 6mm	LINEAR TECH. CORP. LT8612EUDE#PBF
46	1	U4	I.C., DC/DC CONVERTER DFN (08) (DD) 3mm × 3mm	LINEAR TECH. CORP. LT3092EDD#PBF
47	1	U5	I.C., STEP-DOWN CONVERTER DFN (08) (DD) 3mm × 3mm	LINEAR TECH. CORP. LTC3632EDD#PBF
Optional Circuit Components				
1	1	C8	CAP., ALUM 22µF 63V 25%	SUN ELECT. IND. 63CE22BS
2	0	C16, C30	OPTIONAL 0603	
3	0	C24	OPTIONAL 1210	
4	1	D4	LED, GRN	OSRAM OPTO SEMI. LG L29K-G2J1-24-Z
5	0	R6, R19, R25, R46	OPTIONAL 0603	
6	1	R13	RES., CHIP 549Ω 0.10W 1% 0603	VISHAY CRCW0603549RFKEA
7	1	R16	RES./JUMPER, CHIP 0Ω 0.25W 0603	VISHAY CRCW06030000Z0EA
8	0	R33	OPTIONAL POT. 10 TURNS 10k	BOURNS 3950S-1-103L
9	0	R34	OPTIONAL POT. 10 TURNS 5k	BOURNS 3950S-1-502L
Hardware				
1	6	E1, E2, E3, E4, E5, E6	TURRET, TESTPOINT	MILL-MAX 2501-2-00-80-00-00-07-0
2	2	E7, E8	TURRET, TESTPOINT	MILL-MAX 2308-2-00-80-00-00-07-0
3	1	JP1	HEADERS, DBL. ROW 2 × 3 2mm CTRS.	SAMTEC TMM-103-02-L-D
4	4	J1, J2, J3, J4	CONNECTOR, BANANA JACK	KEYSTONE 575-4
5	1	S1	SWITCH TOGGLE, SPDT	PHILMORE, 30-10002B
6	1	XJP1	SHUNT, 2mm CTRS.	SAMTEC 2SN-BK-G

SCHEMATIC DIAGRAM


VIN
10V to 40V
GND
C8
22µF
63V
C3
10uF
50V
1210
R5
499k
R6
54.9k
S1
30-10002B
Philmore
ON
OFF
Q4
Si2309CDS
R47
5.1k
Q5
CMST3904
R48
2.7k
D4
GREEN
R13
549
C14
1µF
INTVCC
U3
LT8612EUDE
VIN
EN/UV
SYNC
INTVCC
RT
TR/SS
PGND
GND
NC
FB
PG
BIAS
SW
BST
C4
0.1µF
C15
0.1µF
R20
60.4k
700kHz
L1
5.5µH
744325550
Wurth
R14 5.1k
R16
1.00k
R46
(Opt)
C30
(Opt)
C13
1nF
R37
1.00k
1%
Q2
MMBT3906
R18
4.99k
R38
100k
1%
R21
100k
1%
C29
100µF
35V
EMZA350ADA101MF80G
C5,C6,C19
3x 10µF
50V
1210
C7
10uF
50V
1210
IMON
R15
1.00k
1%
U1 LT3081ER
IN
NC
IMON
SET
OUT
TAB
ILIM
TEMP
C23
0.01µF
D5
B140
R17
10.0k
1%
TEMP1
R8
3.92K
ILIM+
ILIM-
R12
100
1%
C10,C11,C27
3x 10µF
50V
1210
R7
0.010
1%
0805
R9
10k
1206
C12
1µF
50V
0V - 24V
0A - 3A
NOTE 1
VOUT
GND
R2
549
Q1
FMMT493
R32 5k
Bourns Inc. 91A1A-B28-A13L
ILIM ADJUST
CW
CCW
C26
10µF
6.3V
R42
1.47M
R44
280k
1%
L2 470µH
muRata
LQH32CN471K23L
R45
806k
U5
LTC3632EDD
VIN
RUN
HYST
SS
SW
VFB
ISET
GND
C25
1µF
R43
10k
Q3 MMBT3906
R41
1k
U2 LT3081ER
C9
10uF
50V
1210
R29
1.00k
1%
C17
0.01µF
R30
10.0k
1%
TEMP2
C20,C22,C28
3x 10uF
50V
1210
R23
0.010
1%
0805
R26
10k
1206
VOUT ADJUST
R31 10k
Bourns Inc. 91A1A-B28-A15L
IMON
GND
R28
11.3k
R27
73.2k
VOUT MAX
5V
15V
24V
JP1
NOTE 1
R22
200
1%
0805
R24
47.5k
U4
LT3092EDD
IN
NC
OUT
SET
C21
1µF
50V
0805

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

DEMONSTRATION BOARD IMPORTANT NOTICE

Linear Technology Corporation (LTC) provides the enclosed product(s) under the following **AS IS** conditions:

This demonstration board (DEMO BOARD) kit being sold or provided by Linear Technology is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not provided by LTC for commercial use. As such, the DEMO BOARD herein may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including but not limited to product safety measures typically found in finished commercial goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may or may not meet the technical requirements of the directive, or other regulations.

If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

No License is granted under any patent right or other intellectual property whatsoever. **LTC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind.**

LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

Copyright © 2004, Linear Technology Corporation

© LINEAR TECHNOLOGY CORPORATION 2014

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0387.

Devices Connected/Referenced	
ADL6010	Fast Responding, 45 dB Range, 0.5 GHz to 43.5 GHz Envelope Detector
AD7091R	1 MSPS, Ultralow Power, 12-Bit ADC in 10-Lead LFCSP and MSOP
HMC547	GaAs MMIC, SPDT, Nonreflective Switch, DC to 28 GHz

Calibration-Free Return Loss Measurement System

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

- CN-0387 Return Loss Measurement Evaluation Board (EV-VSWR-SDZ)
- System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

- Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 accurately measures return loss in a wireless transmitter from 1 GHz to 28 GHz without any need for system calibration.

The design is implemented on a single circuit board using a nonreflective RF switch; a microwave RF detector; and a 12-bit, precision analog-to-digital converter (ADC). To evaluate the circuit over the widest possible frequency range, a dual-port directional coupler with SMA connectors was used instead of a narrow-band, surface-mount directional coupler.

The circuit measures return loss of up to 20 dB over an input power range of 25 dB (return losses in excess of 20 dB can be measured over a smaller input power range).

A unique feature of the circuit is that it calculates return loss using a simple ratio of the digitized voltages from the RF detector, thereby eliminating the need for system calibration.

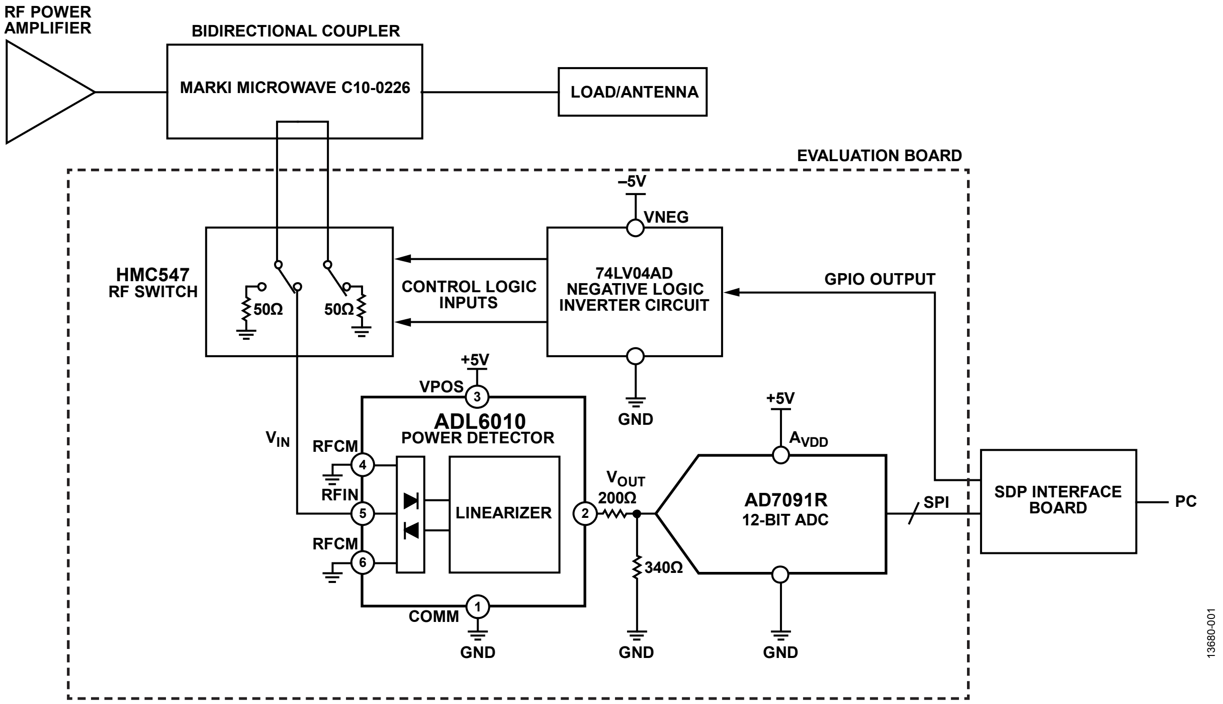

RF POWER AMPLIFIER
BIDIRECTIONAL COUPLER
MARKI MICROWAVE C10-0226
LOAD/ANTENNA
EVALUATION BOARD
–5V
VNEG
HMC547 RF SWITCH
50Ω
50Ω
CONTROL LOGIC INPUTS
74LV04AD NEGATIVE LOGIC INVERTER CIRCUIT
GPIO OUTPUT
GND
+5V
VPOS
3
ADL6010 POWER DETECTOR
V_{IN}
RFCM
4
RFIN
5
RFCM
6
LINEARIZER
2
V_{OUT}
200Ω
340Ω
+5V
A_{VDD}
AD7091R 12-BIT ADC
SPI
SDP INTERFACE BOARD
PC
COMM
1
GND
GND
GND
13680-001

Figure 1. Voltage Standing Wave Ratio (VSWR) Evaluation Board Measurement Setup (All Connections and Decoupling Not Shown)

Rev. A
Circuits from the Lab® reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
©2015 Analog Devices, Inc. All rights reserved.

CIRCUIT DESCRIPTION

An RF signal between 1 GHz and 28 GHz is fed through an RF coupler (Marki Microwave C10-0226) to a matched 50 Ω load or antenna as shown in Figure 1. The forward and reverse coupled ports are connected to the HMC547, a single-pole/double-throw (SPDT) nonreflective switch. The switch input is toggled between the forward and reverse coupled ports, while terminating the opposite port in 50 Ω, so that both coupled ports always see a 50 Ω load.

The output port of the RF switch drives the ADL6010, a microwave RF detector that can operate from 500 MHz to 43.5 GHz. The output voltage level of the detector is directly proportional to the amplitude of the input signal. The ADL6010 is a linear-in-V/V detector, having a nominal slope of 2.1 V/V.

The AD7091R 12-bit ADC samples the power detector output voltage at a rate of 1 MSPS. (Lower sampling rates can also be used, resulting in lower power consumption in the ADC).

The AD7091R converts the analog voltage to a digital code. The EVAL-SDP-CB1Z (SDP-B) interface board then uses serial peripheral interface (SPI) communications to control the ADC and sends results to a PC for system evaluation and return loss calculation. The VSWR, return loss, and reflection coefficient are then calculated using the ratio between the forward and reverse coupled voltages sampled by the ADC.

Return Loss Calculation

The following derivation shows the relationship between the ratio of forward and reverse voltages and the return loss of the system. This relationship is fundamental to the calibration-free nature of the system.

The system transfer function of the detector in its linear operating region can be expressed using the familiar straight-line equation,

$$y = mx + c$$

where:
m is the slope.
c is the intercept.

Using actual circuit parameters,

$$V_{OUT} = m \times V_{IN} + c \tag{1}$$

As noted previously, m is nominally 2.1, but can vary with frequency and from device to device. The value of c is typically close to zero.

Rewriting Equation 1 in terms of V_{IN},

$$\Rightarrow V_{IN} = \frac{V_{OUT} - c}{m} \tag{2}$$

Converting this equation to power,

$$\Rightarrow P_{IN} = \frac{\left(\frac{V - c}{m}\right)^2}{R} \tag{3}$$

Then converting to dBm,

$$P_{IN_{dBm}} = 10 \times \log\left(1000 \times \frac{\left(\frac{V_{OUT} - c}{m}\right)^2}{R}\right) \tag{4}$$

If the ADC is included, the equation becomes

$$P_{IN_{dBm}} = 10 \times \log\left(1000 \times \frac{\left(\frac{CODE - c'}{m'}\right)^2}{R}\right) \tag{5}$$

where:
m' is the slope of the detector and ADC combined signal chain.
c' is the intercept of the detector and ADC combined signal chain.

The return loss is the difference between the forward and reverse power in dBm:

$$P_{F_{dBm}} - P_{R_{dBm}} = 10 \times \log\left(\frac{1000 \times \frac{\left(\frac{CODE_F - c'}{m'}\right)^2}{R}}{1000 \times \frac{\left(\frac{CODE_R - c'}{m'}\right)^2}{R}}\right) \tag{6}$$

$$\Rightarrow P_{F_{dBm}} - P_{R_{dBm}} = 10 \times \log\left(\frac{(CODE_F - c')^2}{(CODE_R - c')^2}\right) \tag{7}$$

Because c' is close to zero, and because $CODE_F$ and $CODE_R$ are generally much greater than c', the formula reduces to

$$P_{F_{dBm}} - P_{R_{dBm}} = 10 \times \log\left(\frac{CODE_F^{\,2}}{CODE_R^{\,2}}\right) \tag{8}$$

The derivation in this section shows that return loss can be calculated without the need for calibration, because the formula does not include the slope (m') or intercept (c') of the signal chain.

RF Switch

The HMC547 is a nonreflective SPDT RF switch with a frequency range of dc to up to 28 GHz. As shown in the Figure 2 block diagram, the switch internally terminates either input at 50 Ω, while the other input is fed to the RFC output. The switch has a fast switching time of typically 6 ns. The A and B logic inputs of this switch are controlled by negative voltage logic of −5 V high and 0 V low. A recommended control circuit is included in the HMC547 data sheet. The circuit consists of a 5.1 V Zener diode level shifter that drives 74LV04AD inverters. The inverters are powered between −5 V and 0 V, rather than 0 V and +5 V. The complete power supply circuit is shown in the detailed schematic contained in the CN-0387 Design Support Package, available at www.analog.com/CN0387-DesignSupport.

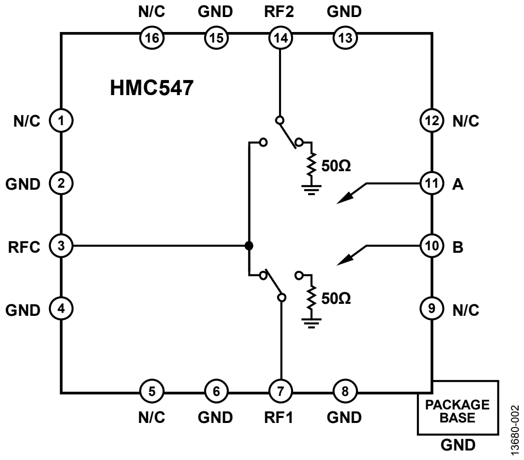

N/C
GND
RF2
GND
16
15
14
13
HMC547
N/C 1
GND 2
RFC 3
GND 4
12 N/C
11 A
10 B
9 N/C
50Ω
50Ω
5
6
7
8
N/C
GND
RF1
GND
PACKAGE BASE
GND
13680-002

Figure 2. HMC 547 Top View

Power Detector

The ADL6010 power detector has a linear-in-V/V characteristic, which is key to this application. To power this device, apply a +5 V dc voltage to the VPOS pin and round to the COMM pin, as shown in Figure 3.

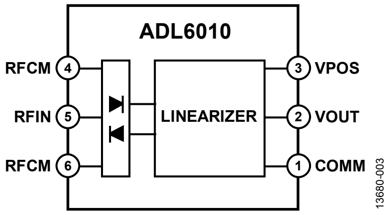

ADL6010
RFCM 4
RFIN 5
RFCM 6
LINEARIZER
3 VPOS
2 VOUT
1 COMM
13680-003

Figure 3. ADL6010 RF/Microwave Detector Functional Diagram

As shown in Figure 4, the output voltage varies with frequency. This variation in transfer function vs. frequency does not degrade the performance of the circuit in any way because the return loss calculation relies on a ratiometric calculation at a specific frequency.

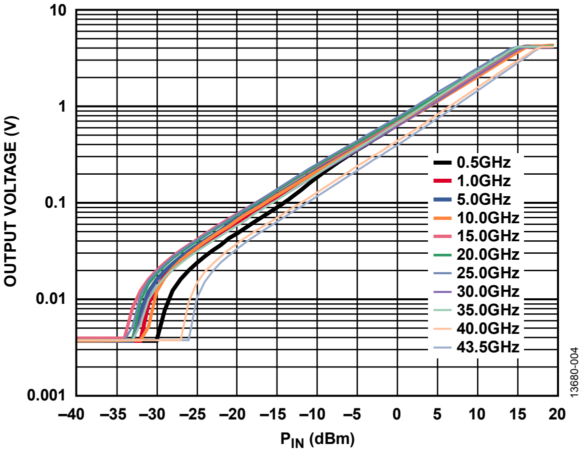


Figure 4. Transfer Function at Frequencies from 500 MHz to 43.5 GHz

Analog-to-Digital Converter

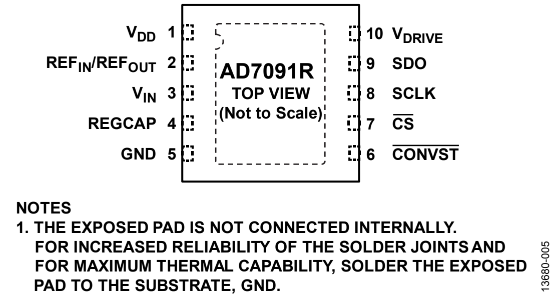

V_{DD} 1
REF_{IN}/REF_{OUT} 2
V_{IN} 3
REGCAP 4
GND 5
AD7091R
TOP VIEW
(Not to Scale)
10 V_{DRIVE}
9 SDO
8 SCLK
7 $\overline{CS}$
6 $\overline{CONVST}$
NOTES
1. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND FOR MAXIMUM THERMAL CAPABILITY, SOLDER THE EXPOSED PAD TO THE SUBSTRATE, GND.
13680-005

Figure 5. AD7091R Analog-to- Digital Converter

The AD7091R is a 12-bit successive approximation register (SAR) ADC, which has a throughput rate of up to 1 MSPS. Although a highly accurate external reference voltage can be used, it is not required in this application. In this circuit, the internal reference of 2.5 V is used, which yields an LSB size of

$$LSB = (2.5\ \text{V})/2^{12} = 610\ \mu\text{V}$$

Because the output voltage of the ADL6010 can reach a maximum voltage of approximately 3 V, it is necessary to attenuate this voltage using a 200 Ω/340 Ω resistor divider between the detector and the ADC, as shown in Figure 1. This divider provides a nominal attenuation of 1.6.

Directional Coupler

A directional coupler couples a portion of the forward or reverse signals to the power detector for measurement. In general, couplers have 4 ports as shown in Figure 6.

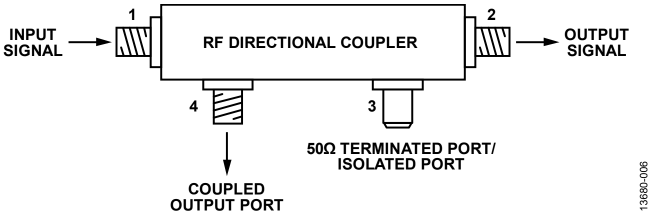

INPUT SIGNAL
1
RF DIRECTIONAL COUPLER
2
OUTPUT SIGNAL
4
3
50Ω TERMINATED PORT/ ISOLATED PORT
COUPLED OUTPUT PORT
13680-006

Figure 6. Directional Coupler

In the Figure 6 configuration, the input signal is coupled to Port 4, and Port 3 is terminated at 50 Ω for nonreflective coupling of the signal. If Port 4 is terminated in 50 Ω instead of Port 3, the reflected signal is coupled to Port 3.

In this circuit, instead of using the 50 Ω termination connected directly to the port as shown previously, both ports are fed to the RF switch inputs. Therefore, the coupler can be regarded as being bidirectional, because the 50 Ω termination is applied by the HCM547 internally to Port 3 or Port 4, depending on the state of the switch.

The RF coupler chosen for this circuit was the Marki Microwave C10-0226 stripline coupler. This coupler has 10 dB coupling, meaning that the coupled signal is 10 dB less than the input signal. A directional coupler with SMA connectors was used in this circuit to demonstrate operation over the widest possible frequency range. A surface-mount coupler can also be used; however, such devices generally have a narrower frequency range.

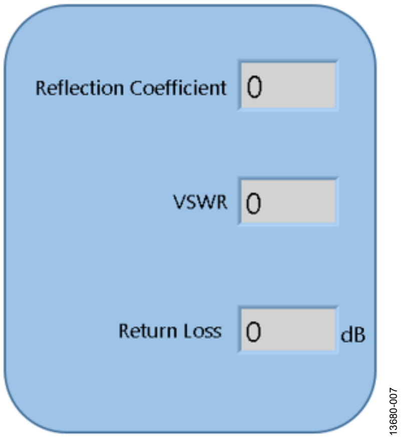
Data Analysis

The EVAL-SDP-CB1Z system demonstration platform (SDP) board is used in conjunction with evaluation software, to capture the data being sampled by the ADC.

The software calculates the return loss using Equation 8, which was derived previously. The reflection coefficient and VSWR are derived from this equation.

$$P_{F_{dBm}} - P_{R_{dBm}} = 10 \times \log\left(\frac{CODE_F{}^2}{CODE_R{}^2}\right) \tag{8}$$

Figure 7 shows the result display panel of the software GUI.



Reflection Coefficient 0

VSWR 0

Return Loss 0 dB

Figure 7. CN-0387 Evaluation Software Display

Detector Sampling Strategy

To accurately measure the return loss of the system, the forward and reverse voltages must be measured with a short time delay between the forward and reverse measurements. Figure 8 shows the sampling sequence performed when sampling continuously.

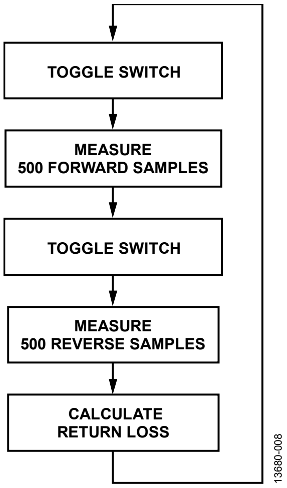


Figure 8. Sampling Sequence

When the RF switch receives the signal to toggle the switch, the switch position changes, and the forward or reverse coupled port signal is fed to the power detector. In the return loss calculation step, 500 forward samples and 500 reverse samples are averaged, and the return loss is calculated from the ratio of averaged forward and reverse voltages.

The ADC samples at a rate of 1 MSPS. Therefore, it takes 500 µs to measure 500 samples. Toggling the switch position using a general-purpose input/output (GPIO) of the SDP-B interface takes approximately 400 µs between forward and reverse cycles. The timing diagram is shown in Figure 9.

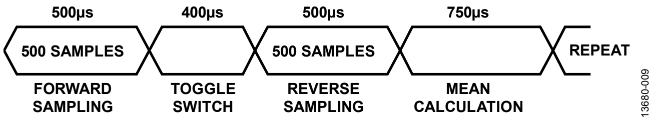


Figure 9. Timing Diagram Representation

The return loss, reflection coefficient, and VSWR are calculated using the resultant average of forward and reverse voltage measurements. To allow results to be clearly read before updating, 50 sample results are averaged before displaying on the GUI results panel.

Complete documentation for the EVAL-VSWR-SDZ board, including schematics, layouts, Gerber files, and bill of materials, is available for download in the CN-0387 Design Support Package at www.analog.com/CN0387-DesignSupport.

COMMON VARIATIONS

As previously noted, a wideband connectorized directional coupler was used in this circuit to enable operation over the widest possible frequency range. Surface-mount directional couplers or printed circuit directional couplers can also be used; however, these devices tend to have narrower frequency ranges.

Directional couplers with higher coupling factors can also be used, which tend to have lower insertion loss. However, it is recommended that the circuit be dimensioned to maximize measurement range. For example, if the maximum system power is +35 dBm, using a 20 dB directional coupler sets the maximum power to the detector at approximately +15 dBm, which is at the upper limit of the input range.

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is needed to perform the evaluations described in this circuit note:

- The EV-VSWR-SDZ evaluation board.
- A suitably rated broadband RF Coupler. For this evaluation, the Marki Microwave C10-0226 was used. However, any coupler with suitable specifications and with a 3.5 mm SMA type connector can be used.
- The EVAL-SDP-CB1Z SDP-B board.
- A signal generator (with output frequency within the range of 500 MHz to 28 GHz).
- A suitable power supply unit with 6 V dc output voltage.
- The CN-0387 Evaluation Software, which can be downloaded from ftp://ftp.analog.com/pub/cftl/CN0387/.
- An SMA attenuator and 50 Ω termination.
- A PC running Windows® 7 connected to the SDP-B board via a USB cable (supplied with the EVAL-SDP-CB1Z).

Setup and Test

To set up and test the VSWR measurement system, set LK6 in Position B and put LK22 in place, and then take the following steps:

1. Turn on all test equipment and wait until all equipment boots up.
2. Connect the input and output coupled ports of the RF coupler to the RF1 and RF2 3.5 mm SMA connections of the evaluation board, respectively, using suitably rated RF cables.
3. Connect the coupler input port to the 50 Ω output of the signal generator.
4. Connect the output of the coupler to a 50 Ω termination or a suitably rated RF attenuator termination.
5. Connect the EVAL-SDP-CB1Z SDP interface board to the EV-VSWR-SDZ evaluation board.
6. Connect the SDP interface board to a PC via the USB cable provided.
7. Connect the power supply from the dc supply to the power and ground of the banana sockets of the evaluation board.
8. Download and install the CN-0387 Evaluation Software onto the PC that is connected to the SDP-B control board.
9. After the software is installed properly, run the executable.
10. Set the output frequency of the signal generator to 2 GHz and set the power level to 15 dBm output. Then turn on the output of the signal generator.
11. In the software display, select **Continuous**, and then click **Capture**. The software continuously repeats measurements; when each measurement is gathered, the GUI display updates with the value of the return loss and the corresponding values of VSWR and reflection coefficient.

Functional Block Diagram of Test Setup

Figure 10 shows the functional block diagram of the test setup.

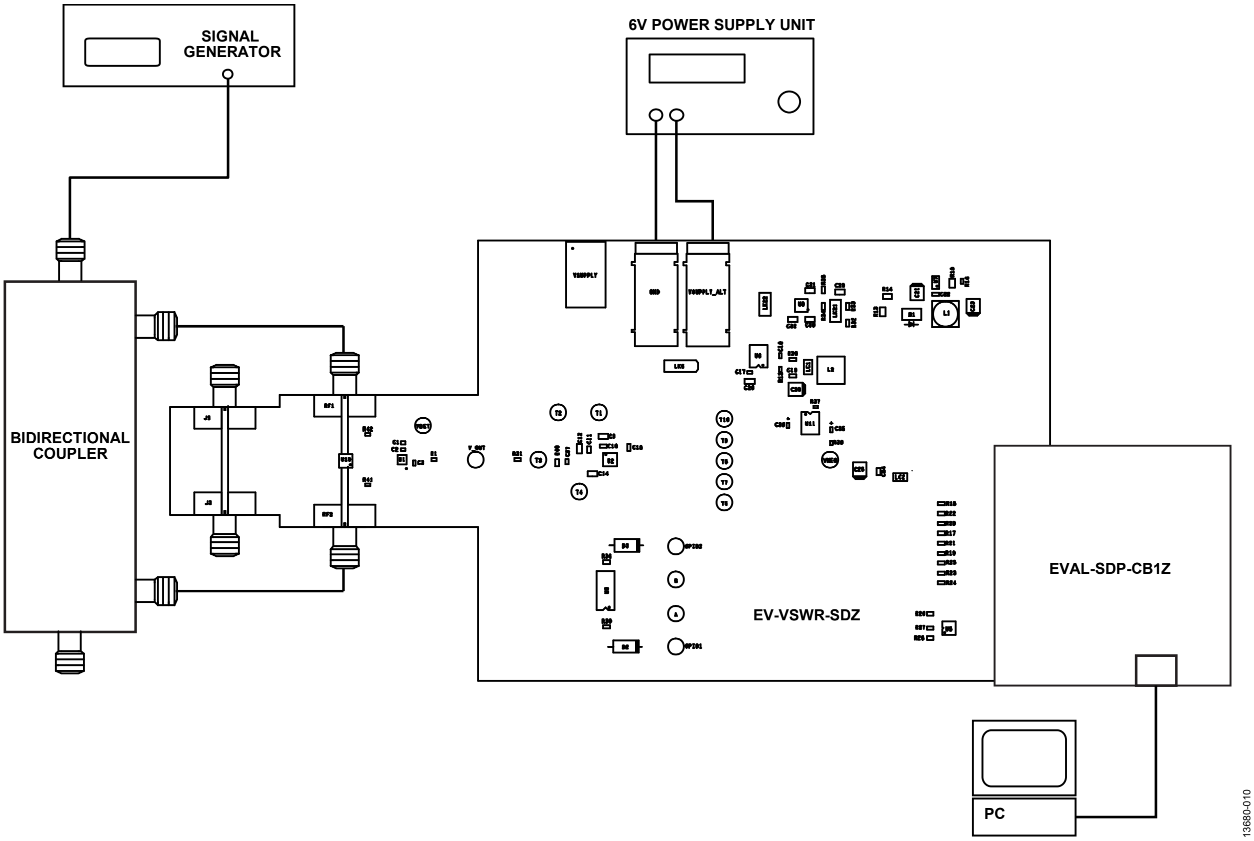


Figure 10. Functional Block Diagram of Test Setup

Test Results

Measurements were gathered manually by adjusting the RF input power levels. Return loss in different output configurations was measured over the power range of the ADL6010.

RF simulations were also run using the Keysight Advanced Design System (ADS). This software is an electronic design simulation tool for RF and microwave applications. Simulations were performed to verify that RF input trace insertion loss and reflection were within certain limits and to simulate the performance of the directional coupler.

The Marki Microwave C10-0226 directional coupler was provided with a simulation model file, an .s4p file. This file contains information that describes the S-parameters of the coupler and can be readily used in ADS within a simulation. Simulations were performed over a frequency range from dc up to the upper frequency limit of the coupler of 26.5 GHz, and the input power was set to 0 dBm for each simulation.

Return Loss Measurement

While testing the EV-VSWR-SDZ evaluation board, a 9 dB attenuator termination was connected to the coupler output to verify that the expected attenuation levels were measured at a chosen frequency as compared to the simulated results.

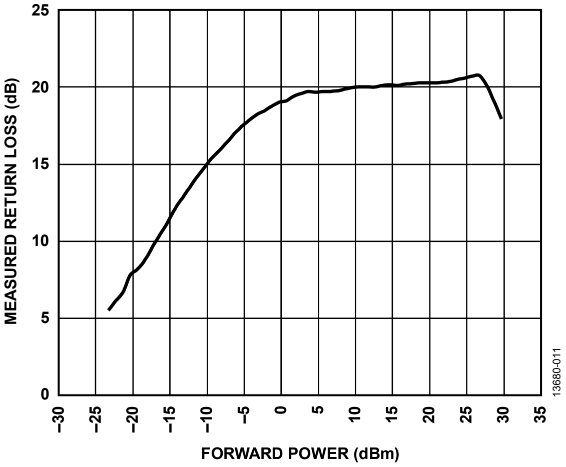


Figure 11. Return Loss Measurement

As shown in Figure 11, within the input power range of 0 dBm to 25 dBm, the return loss measured remains nearly constant at 20 dB. This value is the summation of the forward and reverse attenuations as previously outlined (9 dB + 9 dB), and the forward insertion loss of the coupler at 2 GHz using the Marki Microwave C10-0226. After the input power at the forward coupled port reaches approximately 27 dBm, the return loss reduces significantly. This reduction occurs because the coupled power at the forward coupled port is close to +15 dBm (with 10 dB coupling), which is the upper power limit of the ADL6010. As input power is reduced, the measured return loss begins to reduce due to the reflected power at the reverse coupled port dropping below the lower limit of −30 dBm. Figure 11 illustrates the power range over which the ADL6010 can operate to measure a return loss of 20 dB.

Power Detector Measured Power

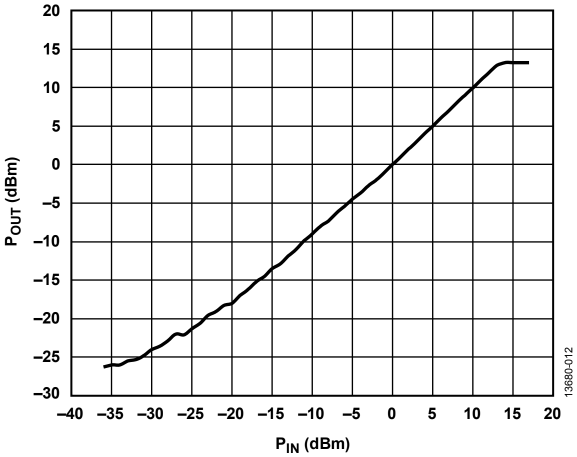


Figure 12. Input Power vs. Measured Coupled Output Power

Figure 12 shows how the measured power changes with input power. A calibration routine was performed at 2 GHz to obtain accurate power measurement at the forward coupled port, at each power level. As the input power rises, the measured power reaches the detector limit of 15 dBm. Similarly, as input power is reduced, the lower limit of the detector is reached and measurement accuracy reduces.

Open Circuit Configuration

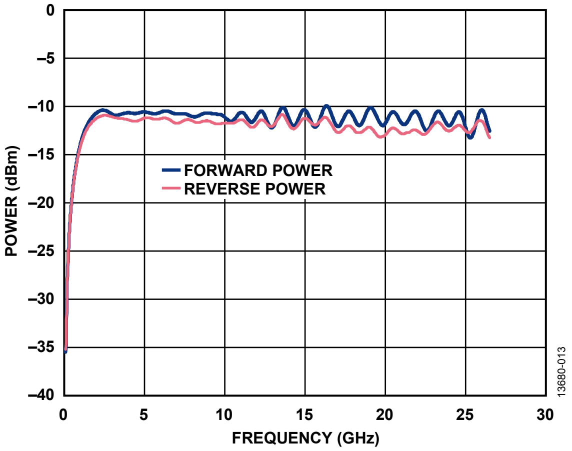


Figure 13. Coupler Forward and Reverse Power vs. Frequency—Open Circuit

Figure 13 shows that the return loss is close to 0 dB as forward and reverse power levels are close in value, compared to the previous 50 Ω termination case.

This open-circuit simulation shows how the majority of the signal is reflected back through the coupler in the opposite direction to the forward wave. The difference in amplitude between the forward and reflected waves is a result of the insertion loss of the coupler across the frequency range. This graph highlights that exact return loss and VSWR measurements vary with the coupler used, due to non-ideal coupler impedance matching across frequency.

Additionally, a threshold return loss can be set to indicate whether there is a mismatch occurring in the system, which is much greater than the coupler return loss.

50 Ω Output Termination Circuit Configuration

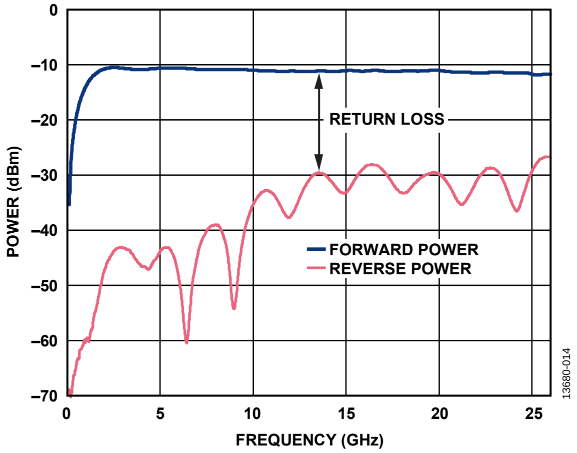


Figure 14. Coupler Forward and Reverse Power vs. Frequency—50 Ω Termination

Figure 14 shows the Marki Microwave C10-0226 RF coupler forward insertion loss and reflected signal for a 50 Ω terminated output with a 0 dBm power level applied to the forward port of the coupler. The coupler is specified to operate from 2 GHz to 26.5 GHz. Therefore, the coupler begins to operate as expected beyond 2 GHz in Figure 14. The simulation uses an ideally matched transmission line of 50 Ω output impedance on the coupler. The return loss at any frequency is the difference between the forward and reverse power. The graph shows that return loss varies with frequency. However, within this frequency range, the return loss is close to 20 dB, which is acceptable because return loss values greater than 20 dB are taken to be negligible.

3 dB Output Attenuator Circuit Configuration

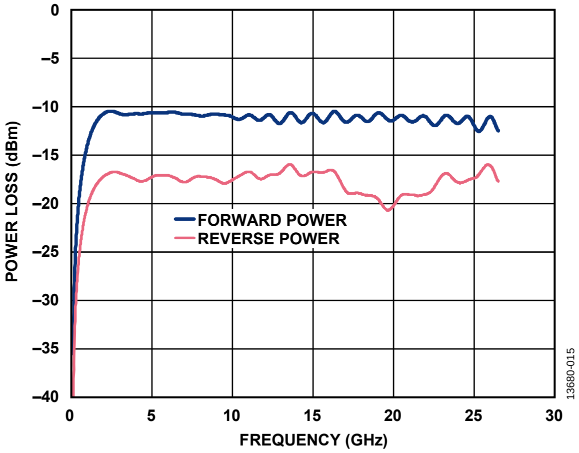


Figure 15. Coupler Forward and Reverse Power vs. Frequency—3 dB Attenuator

In Figure 15, the return loss is relatively stable at 6 dB until up to approximately 15 GHz, after which the loss of the coupler increases and the attenuation increases.

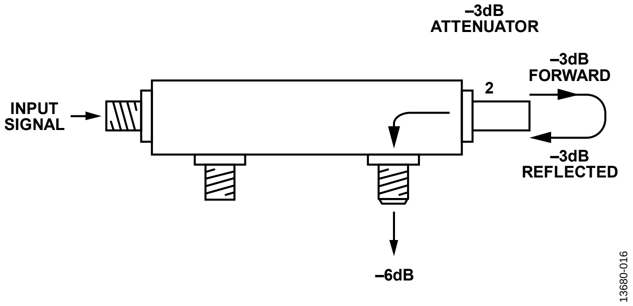


Figure 16. Coupler with 6 dB Attenuation

The 6 dB attenuation is due to the 3 dB coupler attenuating both the incident signal and reflected signal by 3 dB. As shown in Figure 16, the signal first attenuates by 3 dB in the forward direction before being reflected and attenuated by a further 3 dB. The measured reflected signal is the result of the accumulated forward and reverse attenuations.

Calibration Structure Trace Insertion Loss

The RF trace insertion loss was simulated using the layout file of the EV-VSWR-SDZ evaluation board. This layout file was imported into the ADS tool to run a simulation, to determine the losses of the RF traces on the board.

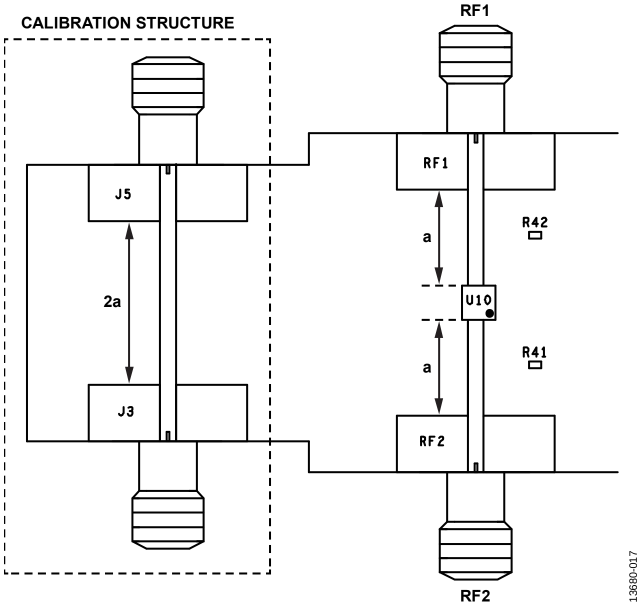


Figure 17. Calibration Structure

The calibration structure shown in Figure 17 on the board section was used in the simulation. This structure was included in the board design to measure the losses from the SMA connector to the switch (Distance A). As shown, the length of the calibration structure is exactly twice the distance from RF1/RF2 to the HMC547 switch (U10). To measure these RF trace losses at a particular frequency, the signal is applied to one of the calibration structure connectors and is then measured on the opposite connector.

The ADS simulation tool was run on this structure from dc to 26.5 GHz to simulate the insertion loss of the RF traces.

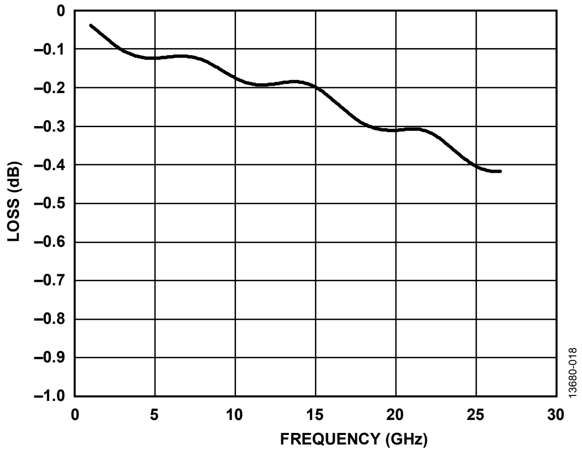


Figure 18. Calibration Structure Loss—Frequency vs. Power

As shown in Figure 18, the insertion loss of the calibration structure reaches a maximum attenuation of approximately −0.4 dB at a frequency of 26.5 GHz.

This insertion loss is considered to be within the acceptable limits for the evaluation board. If this insertion loss is significant, it limits the range of measurement.

A photograph of the EV-VSWR-SDZ board connected to the EVAL-SDP-CB1Z board is shown in Figure 19.

An electrically equivalent replacement part for the HMC547LC3 will be available in June 2016.

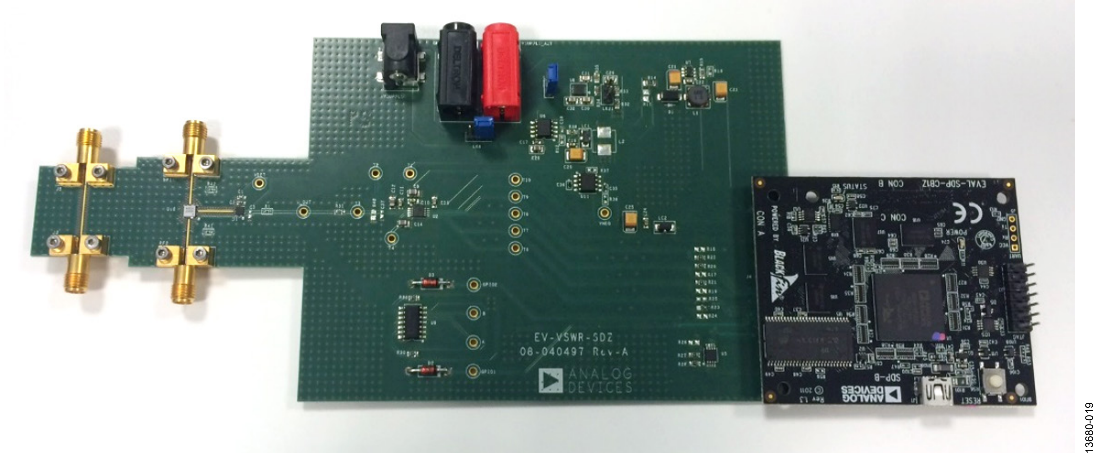


Figure 19. EV-VSWR-SDZ Board Connected to EVAL-SDP-CB1Z Board

LEARN MORE

CN-0387 Design Support Package:
www.analog.com/CN0387-DesignSupport

EVAl-SDP-CB1Z System Demonstration Platform User Guide (UG-277)

EVAL-AD7091RSDZ Evaluation Board User Guide (UG-409)

ADIsimRF Design Tool

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*. Analog Dialogue 39-09, September 2005.

Circuit Note CN-0366. *A 40 GHz Microwave Power Meter with a Range from −30 dBm to +15 dBm*. Analog Devices.

Circuit Note CN-0178. *Software-Calibrated, 50 MHz to 9 GHz, RF Power Measurement System*. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-073 Tutorial. *High Speed Variable Gain Amplifiers (VGAs).* Analog Devices.

MT-101 Tutorial. *Decoupling Techniques.* Analog Devices.

Data Sheets and Evaluation Boards

HMC547LC3 Data Sheet and Evaluation Board

ADL6010 Data Sheet and Evaluation Board

AD7091R Data Sheet and Evaluation Board

REVISION HISTORY

10/15—Rev. 0 to Rev. A
Changes to Setup and Test Section 5

10/15—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab reference designs are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab reference designs in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab reference designs are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab reference designs at any time without notice but is under no obligation to do so.

©2015 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
CN13680-0-10/15(A)

ANALOG DEVICES

Circuit Note

CN-0375

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0375.

Devices Connected/Referenced	
AD9142A	Dual 16-bit, 1.6 GSPS TxDAC+® Digital-to-Analog Converter
ADRF6720	Wideband Quadrature Modulator with Integrated Fractional-N PLL and VCOs
ADL5320	400 MHz to 2700 MHz, ¼ Watt, RF Driver Amplifier

Broadband Low Distortion Transmitter for 3G, 4G, and LTE Communication System

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

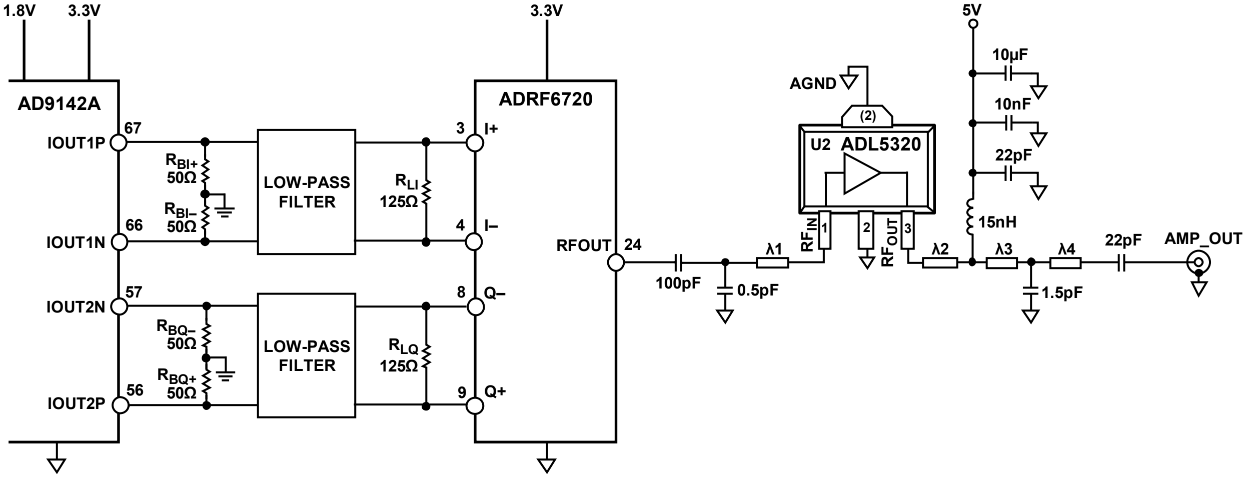
The circuit shown in Figure 1 is a broadband low distortion RF transmitter with a dual high speed TxDAC+ digital-to-analog converter (DAC), a wideband I/Q modulator, and an output driver amplifier.

The devices are well matched, and the direct interface between the DAC and the modulator, and between the modulator and the driver amplifier, offers a compact solution for many RF communications applications including 3G, 4G, and LTE.

CIRCUIT DESCRIPTION

The RF transmitter shown in Figure 1 and Figure 2 utilizes the AD9142A TxDAC, the ADRF6720 phase locked loop (PLL)/ voltage controlled oscillator (VCO) integrated wideband I/Q modulator, and the ADL5320 ¼ W driver amplifier.

Signal biasing and scaling in the DAC-to-modulator interface circuit is controlled by the four ground referenced resistors (R_{BI+}, R_{BI-}, R_{BQ+}, and R_{BQ-}) and the two shunt resistors (R_{LI} and R_{LQ}), respectively. The input and output matching on the ADL5320 driver amplifier is implemented using shunt capacitors at the input and the output. The required matching components and placement are shown in the ADL5320 data sheet.



NOTES
1. SEE ADL5320 DATA SHEET FOR COMPONENT SPACING (λ) VALUES

Figure 1. Simplified Circuit Schematic for I/Q Modulator with DAC and Driver Amplifier (All Connections and Decoupling Not Shown)

Rev. 0

Circuits from the Lab reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
©2015 Analog Devices, Inc. All rights reserved.

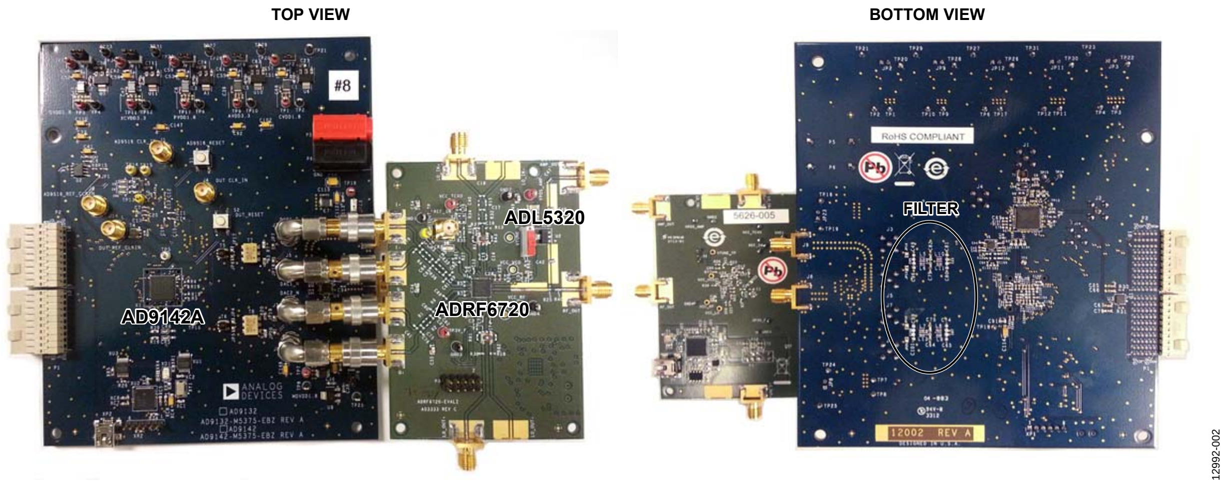

TOP VIEW
BOTTOM VIEW
ADL5320
AD9142A
ADRF6720
FILTER
12992-002

Figure 2. Modified AD9142A Evaluation Board and ADRF6720 Evaluation Board for Circuit Implementation

The nominal and default value of the AD9142A full-scale output current is 20 mA. This current generates the 500 mV dc bias level and a full-scale output voltage swing of 2 V p-p differential on each DAC output pair with the four ground referenced 50 Ω resistors ($R_{BI+} = R_{BI-} = R_{BQ+} = R_{BQ-}$). The 2 V p-p voltage swing can be adjusted by the R_L shunt resistors ($R_L = R_{LI} = R_{LQ}$), which are in parallel with the 500 Ω I/Q input impedance of the ADRF6720 modulator. The 500 mV dc bias level is not affected by this adjustment. For example, with a 100 Ω effective differential load, each single-ended output swings between 250 mV and 750 mV but still maintains an average value of 500 mV.

Figure 3 shows the resulting peak-to-peak differential swing as a function of the R_L swing limiting resistor and the 500 Ω parallel differential input impedance.

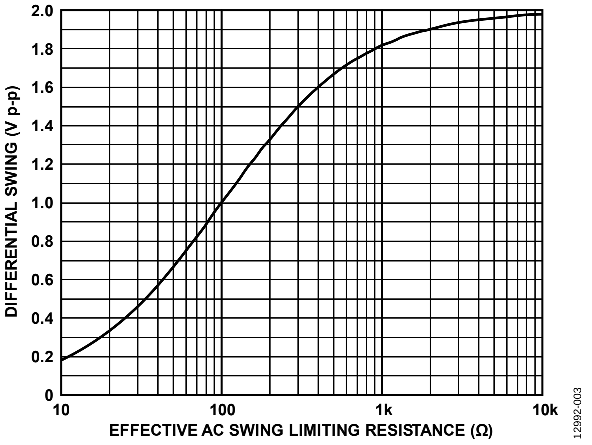


Figure 3. Relationship Between the Effective AC Swing Limiting Resistance and the Peak-to-Peak Voltage Swing with 50 Ω Bias Setting Resistors

I/Q Filtering

An antialiasing filter between the DAC and the modulator is necessary to filter out Nyquist images, common-mode noise, and broadband DAC noise. The filter is placed between the dc bias setting resistors and the ac swing-limiting resistor.

The dc bias-setting resistors set the filter source impedance, and the ac swing limiting resistor in parallel with the ADRF6720 500 Ω input impedance sets the filter load impedance.

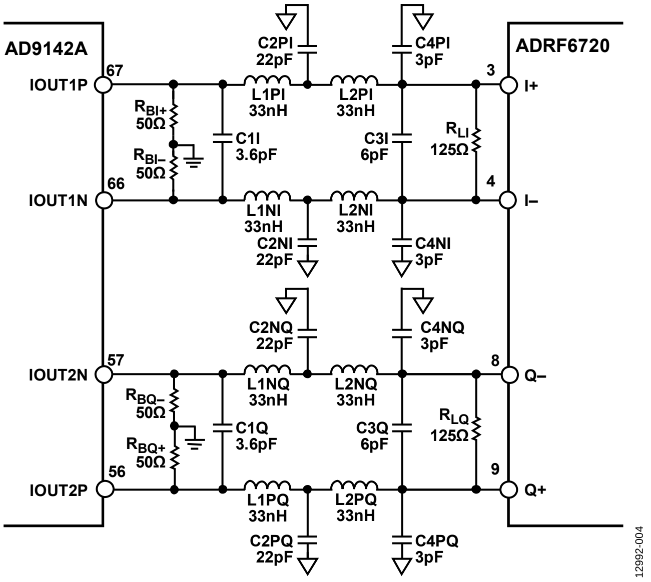

AD9142A
ADRF6720
IOUT1P
67
IOUT1N
66
IOUT2N
57
IOUT2P
56
I+
3
I–
4
Q–
8
Q+
9
C2PI 22pF
C4PI 3pF
L1PI 33nH
L2PI 33nH
RBI+ 50Ω
RBI– 50Ω
C1I 3.6pF
C3I 6pF
RLI 125Ω
L1NI 33nH
L2NI 33nH
C2NI 22pF
C4NI 3pF
C2NQ 22pF
C4NQ 3pF
L1NQ 33nH
L2NQ 33nH
RBQ– 50Ω
RBQ+ 50Ω
C1Q 3.6pF
C3Q 6pF
RLQ 125Ω
L1PQ 33nH
L2PQ 33nH
C2PQ 22pF
C4PQ 3pF
12992-004

Figure 4. Recommended DAC Modulator Interface Topology with f_C = 300 MHz, Fifth-Order, Butterworth Filter

System Level Simulation

Figure 5 shows the simulated cascaded performance of the DAC, the I/Q modulator and the driver amplifier at 2140 MHz. The AD9142A, ADRF6720, and ADL5320 are well matched in terms of dynamic range and gain. Figure 5 shows 39.4 dBm for composite output third-order intercept (OIP3) and approximately −76 dBc adjacent channel leakage ratio (ACLR) performance. The simulation was done using the ADIsimRF Design Tool.

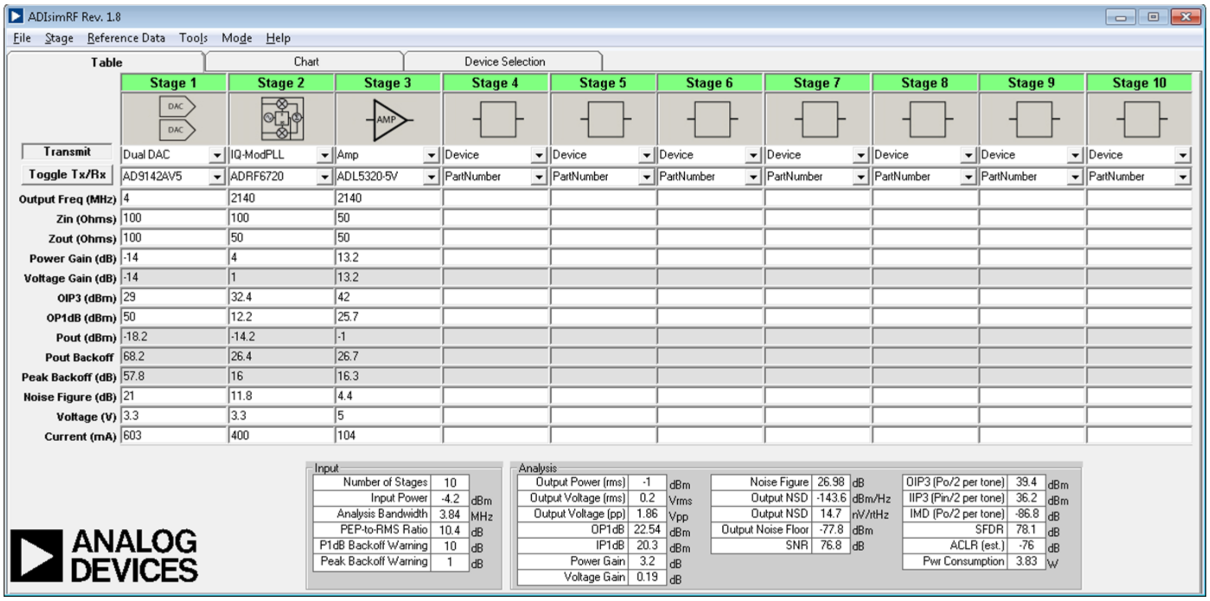
The linearity of the ADRF6720 can be optimized through the MOD_RSEL (Register 0x31, Bits[12:6]) and MOD_CSEL (Register 0x31, Bits[5:0]) settings. These settings control the amount of antiphase distortion to the baseband input stages to correct for distortion.

Figure 6 through Figure 11 show the measured plots of the output second-order intercept (OIP2) and OIP3 optimization at zero IF, 100 MHz, and 200 MHz complex IF by varying the settings of the MOD_RSEL register and the MOD_CSEL register in the ADRF6720.

Figure 6, Figure 7, and Figure 8 show optimized OIP3 performance every 32 steps on the MOD_RSEL axis; OIP3 performance does not vary significantly as a function of MOD_CSEL at zero IF. However, there is more sensitivity to MOD_CSEL at the higher IF frequencies.

Through MOD_RSEL and MOD_CSEL optimization, OIP3 is approximately 42 dBm at zero IF, 45 dBm at 100 MHz IF, and 48 dBm at 200 MHz IF.

The RSEL and CSEL adjustment do not impact OIP2 performance significantly; however, there is some degradation at high IF frequencies.



	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7	Stage 8	Stage 9	Stage 10
Transmit	Dual DAC	IQ-ModPLL	Amp	Device	Device	Device	Device	Device	Device	Device
Toggle Tx/Rx	AD9142AV5	ADRF6720	ADL5320-5V	PartNumber	PartNumber	PartNumber	PartNumber	PartNumber	PartNumber	PartNumber
Output Freq (MHz)	4	2140	2140							
Zin (Ohms)	100	100	50							
Zout (Ohms)	100	50	50							
Power Gain (dB)	-14	4	13.2							
Voltage Gain (dB)	-14	1	13.2							
OIP3 (dBm)	29	32.4	42							
OP1dB (dBm)	50	12.2	25.7							
Pout (dBm)	-18.2	-14.2	-1							
Pout Backoff	68.2	26.4	26.7							
Peak Backoff (dB)	57.8	16	16.3							
Noise Figure (dB)	21	11.8	4.4							
Voltage (V)	3.3	3.3	5							
Current (mA)	603	400	104							

Input

Number of Stages	10	
Input Power	-4.2	dBm
Analysis Bandwidth	3.84	MHz
PEP-to-RMS Ratio	10.4	dB
P1dB Backoff Warning	10	dB
Peak Backoff Warning	1	dB

Analysis

Output Power (rms)	-1	dBm
Output Voltage (rms)	0.2	Vrms
Output Voltage (pp)	1.86	Vpp
OP1dB	22.54	dBm
IP1dB	20.3	dBm
Power Gain	3.2	dB
Voltage Gain	0.19	dB

Noise Figure	26.98	dB
Output NSD	-143.6	dBm/Hz
Output NSD	14.7	nV/rtHz
Output Noise Floor	-77.8	dBm
SNR	76.8	dB

OIP3 (Po/2 per tone)	39.4	dBm
IIP3 (Pin/2 per tone)	36.2	dBm
IMD (Po/2 per tone)	-86.8	dB
SFDR	78.1	dB
ACLR (est.)	-76	dB
Pwr Consumption	3.83	W

Figure 5. ADIsimRF Design Tool Screenshot Showing Cascaded Performance of the AD9142A, ADRF6720, and ADL5320

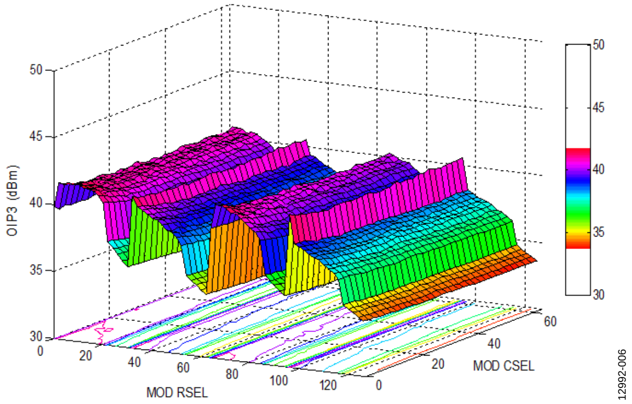


Figure 6. OIP3 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, Zero IF, Output Power of ADL5320 = 11 dBm

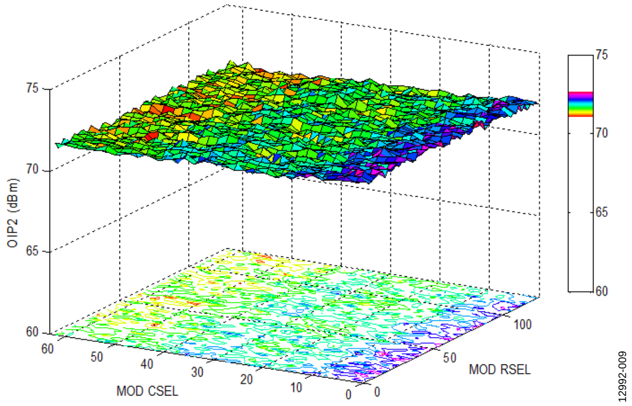


Figure 9. OIP2 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, Zero IF, Output Power of ADL5320 = 11 dBm

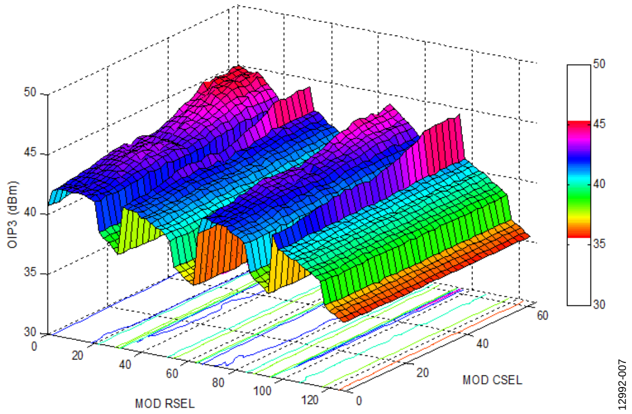


Figure 7. OIP3 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, 100 MHz IF, 2340 MHz LO, Output Power of ADL5320 = 11 dBm

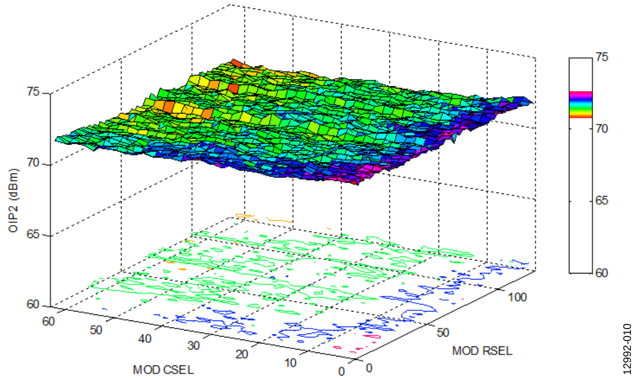


Figure 10. OIP2 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, 100 MHz IF, 2340 MHz LO, Output Power of ADL5320 = 11 dBm

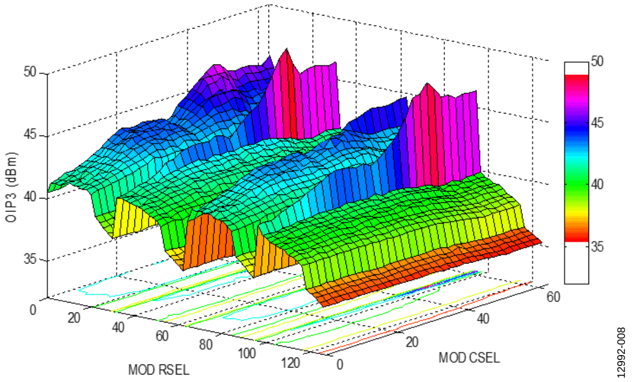


Figure 8. OIP3 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, 200 MHz IF, 2340 MHz LO, Output Power of ADL5320 = 11 dBm

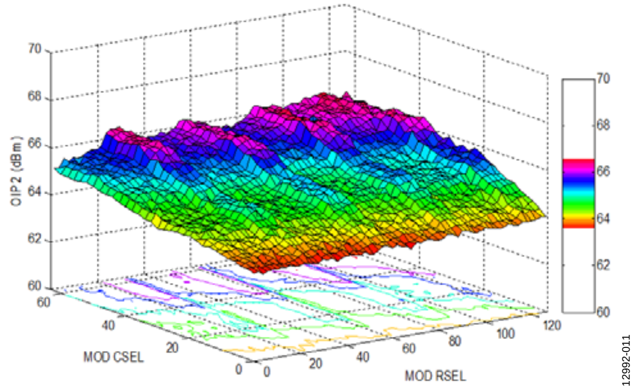


Figure 11. OIP2 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, 200 MHz IF, 2340 MHz LO, Output Power of ADL5320 = 11 dBm

Choosing an Output Power Level

While the circuit can achieve output power levels up to 12 dBm, operation at that level is not practical, especially with modulated carriers with high peak-to-average ratios. To achieve an acceptable level of distortion, significant backoff is required. Adjacent channel power ratio (ACPR) has become a popular metric for assessing the system level distortion.

Figure 12 and Figure 13 show the measured ACPR vs. output power at the ADL5320 output for three IF cases in single carrier WCDMA (Test Model 1-64) and LTE (Test Model 1_1 64QAM) cases, respectively. The system achieves an ACPR of approximately −75 dB to −80 dB at the −2 dBm to +6 dBm output power range. In the case of an LTE signal, ACPR is defined as the ratio of the power in the carrier (in a bandwidth of 4.515 MHz) to the power in an adjacent channel (channel spacing = 5 MHz), also measured in a 4.515 MHz bandwidth.

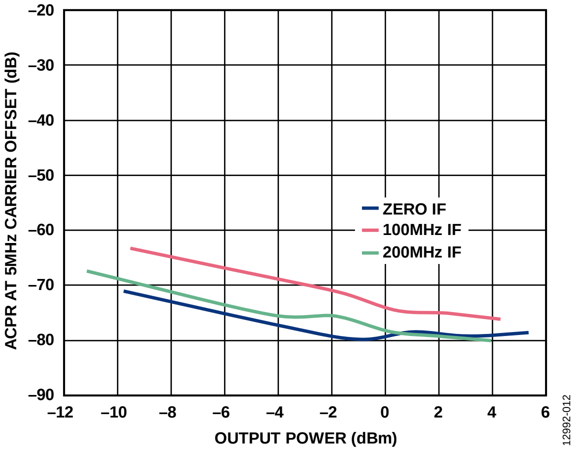


Figure 12. ACLR vs. Output Power at ADL5320 Amplifier Output, Zero IF, Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C WCDMA TM1-64

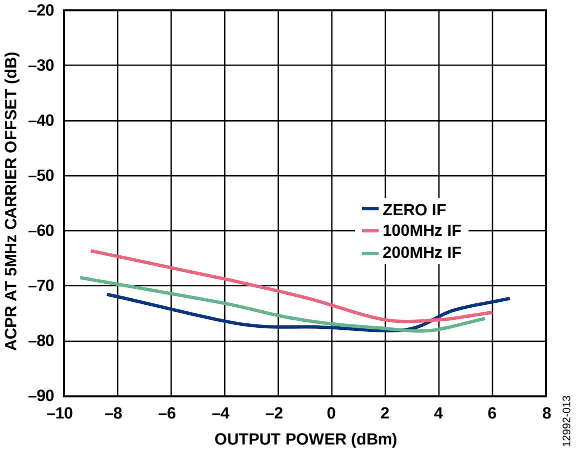


Figure 13. ACLR vs. Output Power at ADL5320 Amplifier Output, OIP3 Optimized RSEL and CSEL on ADRF6720, 1C LTE TM1_1 64QAM

OIP2 and OIP3 can be improved by the MOD_RSEL and MOD_CSEL adjustment shown in the previous section, and accordingly, the ACPR improvement is shown in Figure 13 and Figure 14. The improvement is more noticeable at high output power levels.

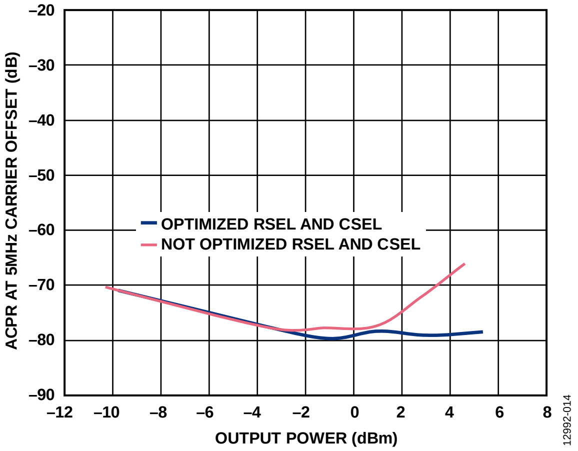


Figure 14. ACLR vs. Output Power at ADL5320 Amplifier Output, Zero IF, Optimized and Not Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C WCDMA TM1-64

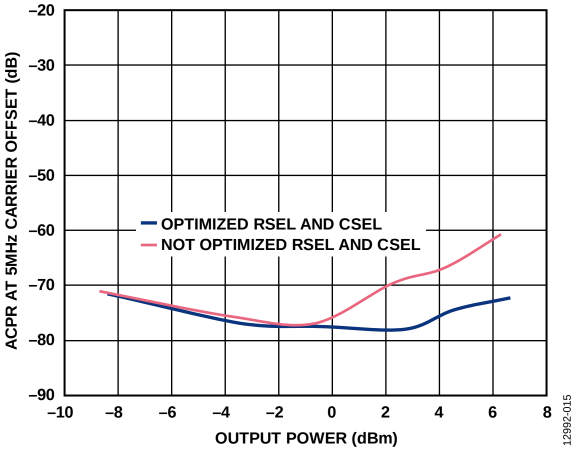
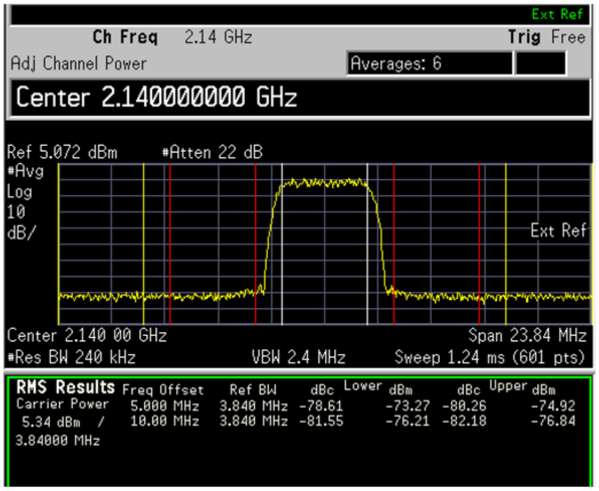


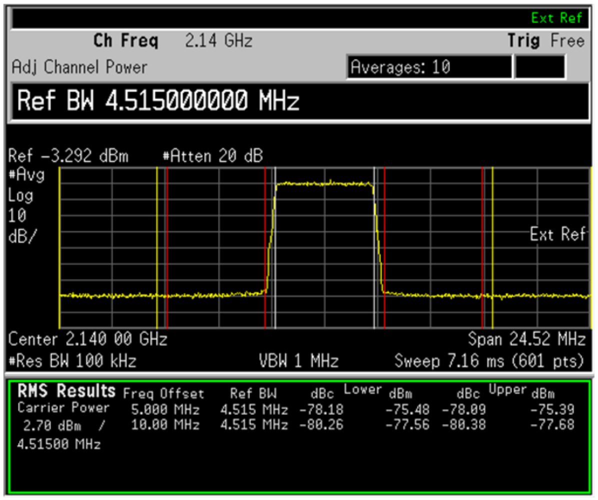
Figure 15. ACLR vs. Output Power at ADL5320 Amplifier Output, Zero IF, Optimized and Not Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C LTE TM1_1 64QAM

The spectrum plots of the single WCDMA and LTE at 2140 MHz are shown in Figure 16 and Figure 17, respectively.



```
Ext Ref
Ch Freq    2.14 GHz                               Trig  Free
Adj Channel Power                     Averages: 6
Center 2.140000000 GHz
Ref 5.072 dBm      #Atten 22 dB
#Avg
Log
10
dB/                                                Ext Ref
Center 2.140 00 GHz                          Span 23.84 MHz
#Res BW 240 kHz          VBW 2.4 MHz    Sweep 1.24 ms (601 pts)
RMS Results  Freq Offset  Ref BW     dBc  Lower dBm      dBc  Upper dBm
Carrier Power 5.000 MHz   3.840 MHz  -78.61     -73.27   -80.26     -74.92
 5.34 dBm  /  10.00 MHz   3.840 MHz  -81.55     -76.21   -82.18     -76.84
3.84000 MHz
```

Figure 16. Adjacent Channel Power Performance at ADL5320 Amplifier Output, Zero IF, Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C WCDMA TM1-64



```
Ext Ref
Ch Freq    2.14 GHz                               Trig  Free
Adj Channel Power                     Averages: 10
Ref BW 4.515000000 MHz
Ref -3.292 dBm     #Atten 20 dB
#Avg
Log
10
dB/                                                Ext Ref
Center 2.140 00 GHz                          Span 24.52 MHz
#Res BW 100 kHz          VBW 1 MHz      Sweep 7.16 ms (601 pts)
RMS Results  Freq Offset  Ref BW     dBc  Lower dBm      dBc  Upper dBm
Carrier Power 5.000 MHz   4.515 MHz  -78.18     -75.48   -78.09     -75.39
 2.70 dBm  /  10.00 MHz   4.515 MHz  -80.26     -77.56   -80.38     -77.68
4.51500 MHz
```

Figure 17. Adjacent Channel Power Performance at ADL5320 Amplifier Output, Zero IF, Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C LTE TM1_1 64QAM

PCB Layout Recommendations

Take special care in the layout of the DAC/modulator/amplifier interface. The following are recommendations for PCB layout:

- Keep all I/Q differential trace lengths well matched.
- Place the filter termination resistors as close as possible to the modulator input.
- Place the DAC output 50 Ω resistors as close as possible to the DAC.
- Use thick trace widths through the filter network to reduce signal loss.
- Place vias around all DAC output traces, filter networks, modulator output traces, LO input traces, amplifier input traces, and amplifier output traces.
- Route LO and modulator outputs on different layers or at 90° angles to each other to prevent coupling.

COMMON VARIATIONS

The DAC and modulator interface described in this circuit note can be used between any TxDAC digital-to-analog converter that is set for 20 mA full-scale current and the I/Q modulators that require 0.5 V baseband dc bias levels. Examples of TxDACs include the AD9779A, AD9788, AD9125, AD9144, and AD9148. I/Q modulators include the ADL5370/ADL5371/ADL5372/ADL5373/ADL5374/ADL5385/ADL5386, and the ADRF6701/ADRF6702/ADRF6703/ADRF6704 PLL/VCO integrated families.

For operation at higher power, the ADL5324 ½ W driver amplifier is recommended. The ADL5320 and ADL5324 must be tuned to the frequency at which they will be operating. The data sheets of both devices contain tables that provide recommended values for tuning components at popular operating frequencies.

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is needed. Equivalents can be substituted.

- AD9142A evaluation board (AD9142-M5375-EBZ) modified with SMA connectors added to allow direct connection to TxDAC current outputs.
- ADRF6720 evaluation board (ADRF6720-EVALZ)
- Analog Devices, Inc., Digital Pattern Generator (DPG)
- Signal generator for clock (R&S SMIQ 03B)
- Signal generator for reference input of ADRF6720 (R&S SMIQ 03B)
- Spectrum analyzer (Agilent E4440A)
- Power supply (Agilent E3631A, two needed)

Setup and Test

1. Connect the set up and measurement system as shown in Figure 18.
2. Set the power supply to 5 V for the AD9142A evaluation board.
3. Set the power supply to 3.3 V for the ADRF6720.evaluation board.
4. Set the power supply to 5 V for the ADL5320 on the ADRF6720 evaluation board.
5. Set the signal generator for the clock to 1.5 GHz at 5 dBm, and set the signal generator for the ADRF6720 reference input to 153.6 MHz at 4 dBm.
6. Turn on the power supply and the signal generators. Set the spectrum analyzer at 2140 MHz.
7. Set up the AD9142A through the USB using the AD9142A SPI control software, as shown in Figure 19, and run. See the AD9142A Evaluation Board Quick Start Guide.
8. Set up the DPG, as shown in Figure 20, and run. See the AD9142A Evaluation Board Quick Start Guide.
9. Set up the ADRF6720, as shown in Figure 21, and run. See the ADRF6720-EVALZ User Guide (UG-689).

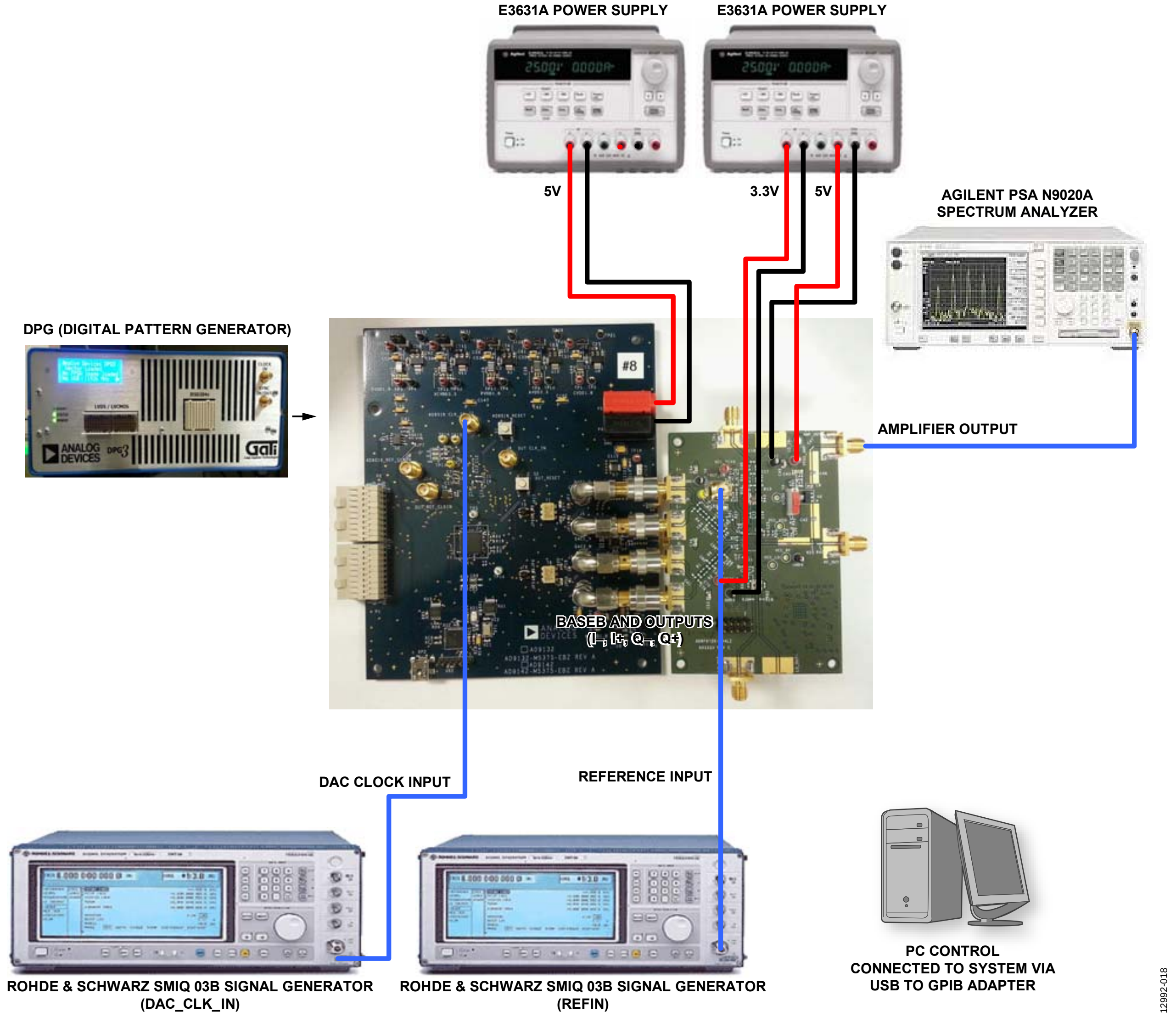
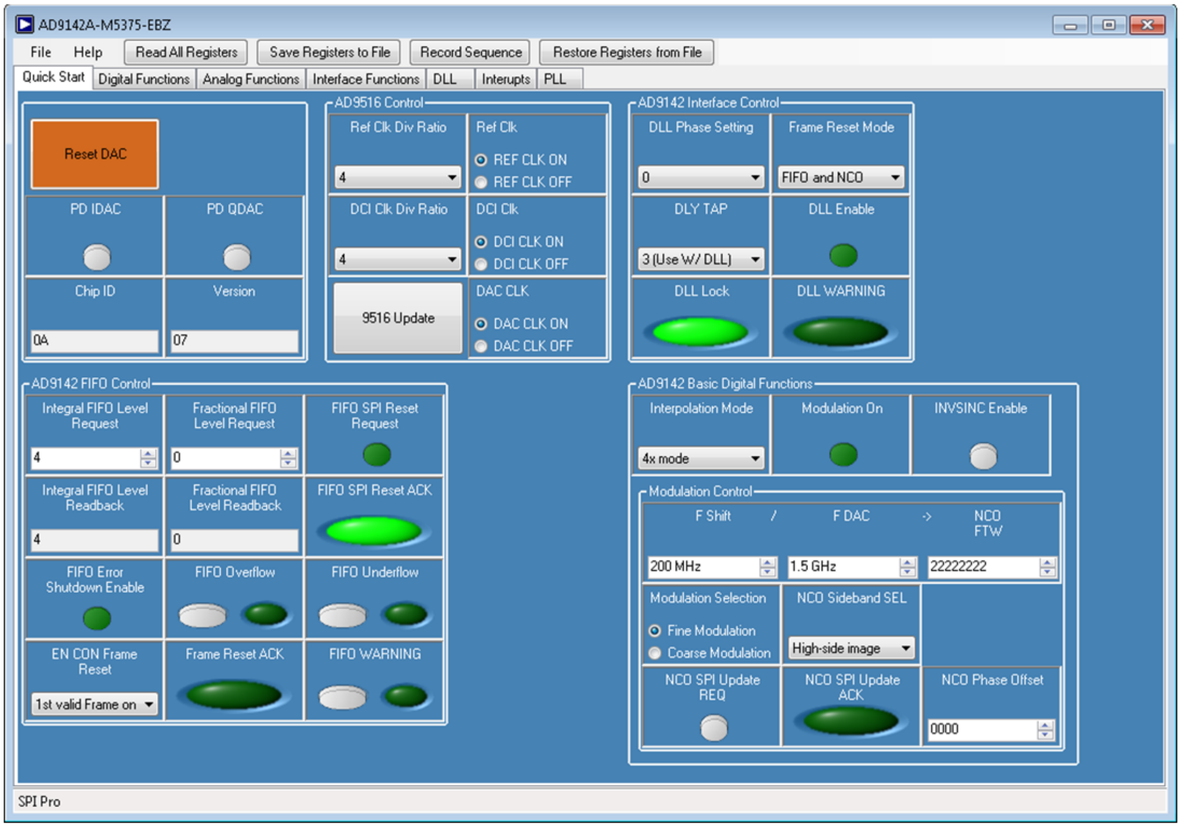

E3631A POWER SUPPLY
E3631A POWER SUPPLY
5V
3.3V
5V
AGILENT PSA N9020A
SPECTRUM ANALYZER
DPG (DIGITAL PATTERN GENERATOR)
AMPLIFIER OUTPUT
BASEB AND OUTPUTS
(I−, I+, Q−, Q+)
DAC CLOCK INPUT
REFERENCE INPUT
ROHDE & SCHWARZ SMIQ 03B SIGNAL GENERATOR
(DAC_CLK_IN)
ROHDE & SCHWARZ SMIQ 03B SIGNAL GENERATOR
(REFIN)
PC CONTROL
CONNECTED TO SYSTEM VIA
USB TO GPIB ADAPTER
12992-018

Figure 18. Test Setup


AD9142A-M5375-EBZ
File
Help
Read All Registers
Save Registers to File
Record Sequence
Restore Registers from File
Quick Start
Digital Functions
Analog Functions
Interface Functions
DLL
Interupts
PLL
Reset DAC
PD IDAC
PD QDAC
9516 Update
SPI Pro
12992-019

Chip ID: 0A
Version: 07

AD9516 Control
Ref Clk Div Ratio: 4
Ref Clk: ● REF CLK ON ○ REF CLK OFF
DCI Clk Div Ratio: 4
DCI Clk: ● DCI CLK ON ○ DCI CLK OFF
DAC CLK: ● DAC CLK ON ○ DAC CLK OFF

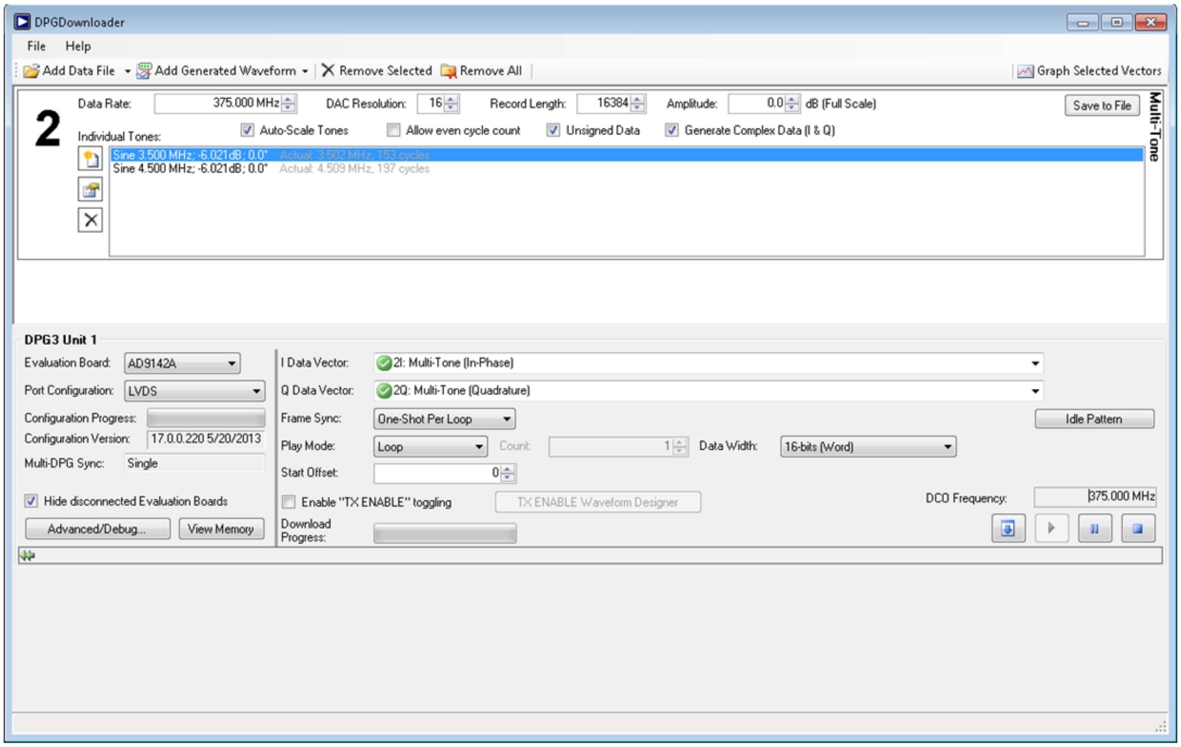
AD9142 Interface Control
DLL Phase Setting: 0
Frame Reset Mode: FIFO and NCO
DLY TAP: 3 (Use W/ DLL)
DLL Enable
DLL Lock
DLL WARNING

AD9142 FIFO Control
Integral FIFO Level Request: 4
Fractional FIFO Level Request: 0
FIFO SPI Reset Request
Integral FIFO Level Readback: 4
Fractional FIFO Level Readback: 0
FIFO SPI Reset ACK
FIFO Error Shutdown Enable
FIFO Overflow
FIFO Underflow
EN CON Frame Reset: 1st valid Frame on
Frame Reset ACK
FIFO WARNING

AD9142 Basic Digital Functions
Interpolation Mode: 4x mode
Modulation On
INVSINC Enable

Modulation Control
F Shift / F DAC -> NCO FTW
200 MHz / 1.5 GHz -> 22222222
Modulation Selection: ● Fine Modulation ○ Coarse Modulation
NCO Sideband SEL: High-side image
NCO SPI Update REQ
NCO SPI Update ACK
NCO Phase Offset: 0000

Figure 19. SPI Control User Interface Setup for AD9142A


DPGDownloader
File
Help
Add Data File
Add Generated Waveform
Remove Selected
Remove All
Graph Selected Vectors
Save to File
Multi-Tone
2
Idle Pattern
TX ENABLE Waveform Designer
Advanced/Debug...
View Memory
12992-020

Data Rate: 375.000 MHz
DAC Resolution: 16
Record Length: 16384
Amplitude: 0.0 dB (Full Scale)

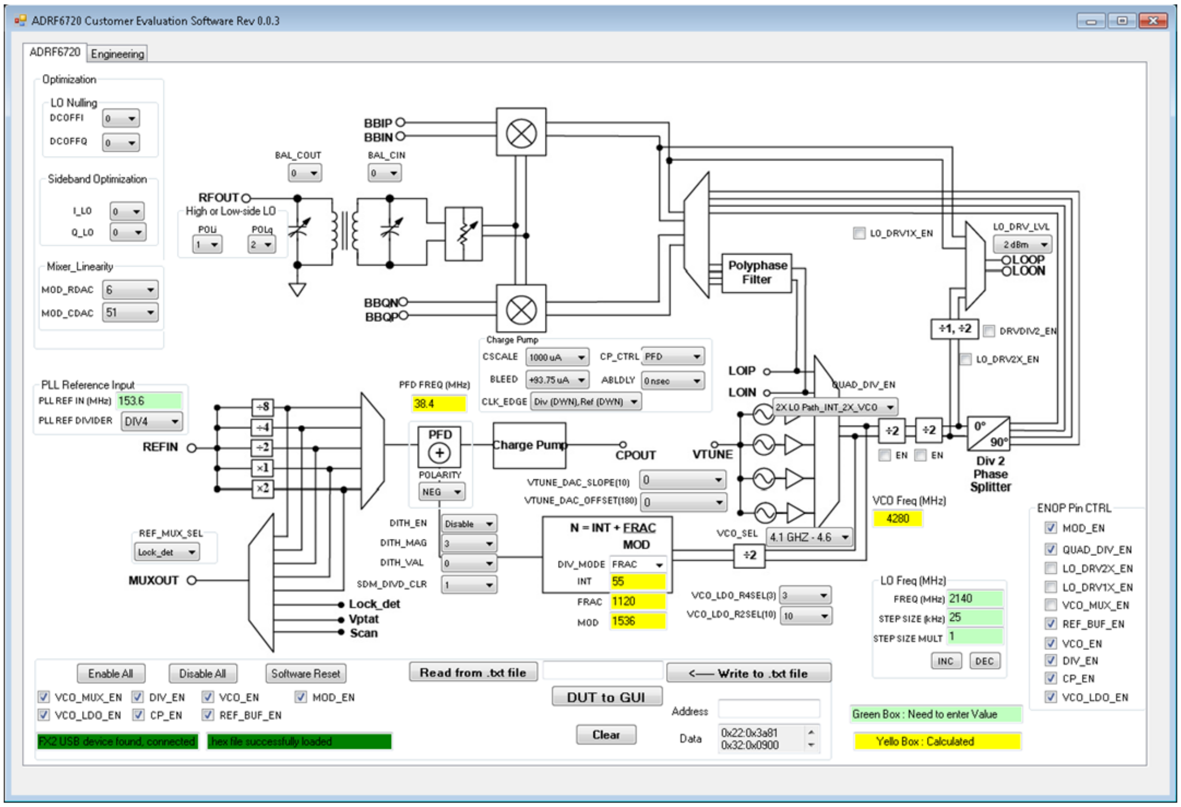
☑ Auto-Scale Tones ☐ Allow even cycle count ☑ Unsigned Data ☑ Generate Complex Data (I & Q)

Individual Tones:
Sine 3.500 MHz; -6.021dB; 0.0° Actual: 3.502 MHz, 153 cycles
Sine 4.500 MHz; -6.021dB; 0.0° Actual: 4.509 MHz, 197 cycles

DPG3 Unit 1
Evaluation Board: AD9142A
Port Configuration: LVDS
Configuration Progress:
Configuration Version: 17.0.0.220 5/20/2013
Multi-DPG Sync: Single
☑ Hide disconnected Evaluation Boards

I Data Vector: 2I: Multi-Tone (In-Phase)
Q Data Vector: 2Q: Multi-Tone (Quadrature)
Frame Sync: One-Shot Per Loop
Play Mode: Loop
Count: 1
Data Width: 16-bits (Word)
Start Offset: 0
☐ Enable "TX ENABLE" toggling
DCO Frequency: 375.000 MHz
Download Progress:

Figure 20. Setting Up the DPG Using the DPG Downloader Software



ADRF6720 Customer Evaluation Software Rev 0.0.3

ADRF6720 | Engineering

Optimization

LO Nulling
DCOFFI 0
DCOFFQ 0

Sideband Optimization
I_LO 0
Q_LO 0

Mixer_Linearity
MOD_RDAC 6
MOD_CDAC 51

BAL_COUT 0
BAL_CIN 0

High or Low-side LO
POLi 1
POLq 2

PLL Reference Input
PLL REF IN (MHz) 153.6
PLL REF DIVIDER DIV4

PFD FREQ (MHz) 38.4

Charge Pump
CSCALE 1000 uA
CP_CTRL PFD
BLEED +93.75 uA
ABLDLY 0 nsec
CLK_EDGE Div (DWN),Ref (DWN)

POLARITY NEG

VTUNE_DAC_SLOPE(10) 0
VTUNE_DAC_OFFSET(180) 0

REF_MUX_SEL Lock_det

DITH_EN Disable
DITH_MAG 3
DITH_VAL 0
SDM_DIVD_CLR 1

DIV_MODE FRAC
INT 55
FRAC 1120
MOD 1536

VCO_SEL 4.1 GHZ - 4.6
QUAD_DIV_EN 2X LO Path_INT_2X_VCO

VCO_LDO_R4SEL(3) 3
VCO_LDO_R2SEL(10) 10

☐ LO_DRV1X_EN
LO_DRV_LVL 2 dBm
☐ DRVDIV2_EN
☐ LO_DRV2X_EN
☐ EN ☐ EN

VCO Freq (MHz) 4280

LO Freq (MHz)
FREQ (MHz) 2140
STEP SIZE (kHz) 25
STEP SIZE MULT 1

ENOP Pin CTRL
☑ MOD_EN
☑ QUAD_DIV_EN
☐ LO_DRV2X_EN
☐ LO_DRV1X_EN
☐ VCO_MUX_EN
☑ REF_BUF_EN
☑ VCO_EN
☑ DIV_EN
☑ CP_EN
☑ VCO_LDO_EN

☑ VCO_MUX_EN ☑ DIV_EN ☑ VCO_EN ☑ MOD_EN
☑ VCO_LDO_EN ☑ CP_EN ☑ REF_BUF_EN

FX2 USB device found, connected
.hex file successfully loaded

Address
Data 0x22:0x3a81
0x32:0x0900

Green Box : Need to enter Value
Yello Box : Calculated

BBIP
BBIN
BBQN
BBQP
RFOUT
Polyphase Filter
LOIP
LOIN
LOOP
LOON
÷1, ÷2
÷2
÷2
0°
90°
Div 2 Phase Splitter
÷2
CPOUT
VTUNE
Charge Pump
PFD
N = INT + FRAC/MOD
REFIN
÷8
÷4
÷2
×1
×2
MUXOUT
Lock_det
Vptat
Scan
Enable All
Disable All
Software Reset
Read from .txt file
<— Write to .txt file
DUT to GUI
Clear
INC
DEC
12992-021

Figure 21. Setting Up the ADRF6720 Using the ADRF6720 Control Software

LEARN MORE

CN-0375 Design Support Package: www.analog.com/CN0375-DesignSupport

Circuit Note CN-0016. *Interfacing the ADL5370 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0017. *Interfacing the ADL5371 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0018. *Interfacing the ADL5372 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0019. *Interfacing the ADL5373 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0020. *Interfacing the ADL5374 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0021. *Interfacing the ADL5375 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0134. *Broadband Low Error Vector Magnitude (EVM) Direct Conversion Transmitter.* Analog Devices.

Circuit Note CN-0144. *Broadband Low Error Vector Magnitude (EVM) Direct Conversion Transmitter Using LO Divide-by-2 Modulator.* Analog Devices.

Circuit Note CN-0205. *Interfacing the ADL5375 I/Q Modulator to the AD9122 Dual Channel, 1.2 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0243. *High Dynamic Range RF Transmitter Signal Chain using Single External Frequency Reference for DAC Sample Clock and IQ Modulator LO Generation.* Analog Devices.

Nash, Eamon. AN-1039 Application Note. *Correcting Imperfections in IQ Modulators to Improve RF Signal Fidelity.* Analog Devices.

Zhang, Yi. AN-1100 Application Note. *Wireless Transmitter I/Q Balance and Sideband Suppression.* Analog Devices.

AN-1237 Application Note. *Precise Control of I/Q Modulator Output Power Using the ADL5386 Quadrature Modulator and the AD5621 12-Bit DAC.* Analog Devices.

ADIsimPLL Design Tool

ADIsimRF Design Tool

UG-689, ADRF6720-EVALZ User Guide

AD9142A Evaluation Board Quick Start User Guide

Analog Devices Data Pattern Generator (DPG)

Data Sheets and Evaluation Boards

AD9142A Data Sheet

ADRF6720 Data Sheet

AD9142-M-5375-EBZ Evaluation Board

ADRF6720-EVALZ Evaluation Board

REVISION HISTORY

1/15—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab reference designs are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab reference designs in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab reference designs are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab reference designs at any time without notice but is under no obligation to do so.

©2015 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
CN12992-0-1/15(0)

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0374.

Devices Connected/Referenced	
ADL5380	400 MHz to 6000 MHz Quadrature Demodulator
ADA4940-2	Ultralow Power, Low Distortion ADC Driver
AD7903	Dual Differential 16-Bit, 1 MSPS PulSAR 12.0 mW ADC
ADR435	Ultralow Noise XFET 5.0 V Voltage Reference with Current Sink and Source Capability

RF-to-Bits Solution Offers Precise Phase and Magnitude Data to 6 GHz

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

- **ADL5380 Evaluation Board (ADL5380-EVALZ)**
- **ADA4940-2 Evaluation Board (ADA4940-2ACP-EBZ)**
- **AD7903 Evaluation Board (EVAL-AD7903SDZ)**
- **System Demonstration Platform (EVAL-SDP-CB1Z)**

Design and Integration Files

- **Schematics, Layout Files, Bill of Materials**

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 precisely converts a 400 MHz to 6 GHz RF input signal to its corresponding digital magnitude and digital phase. The signal chain achieves 0° to 360° of phase measurement with 1° of accuracy at 900 MHz. The circuit uses a high performance quadrature demodulator, a dual differential amplifier, and a dual differential 16-bit, 1 MSPS successive approximation analog-to-digital converter (SAR ADC).

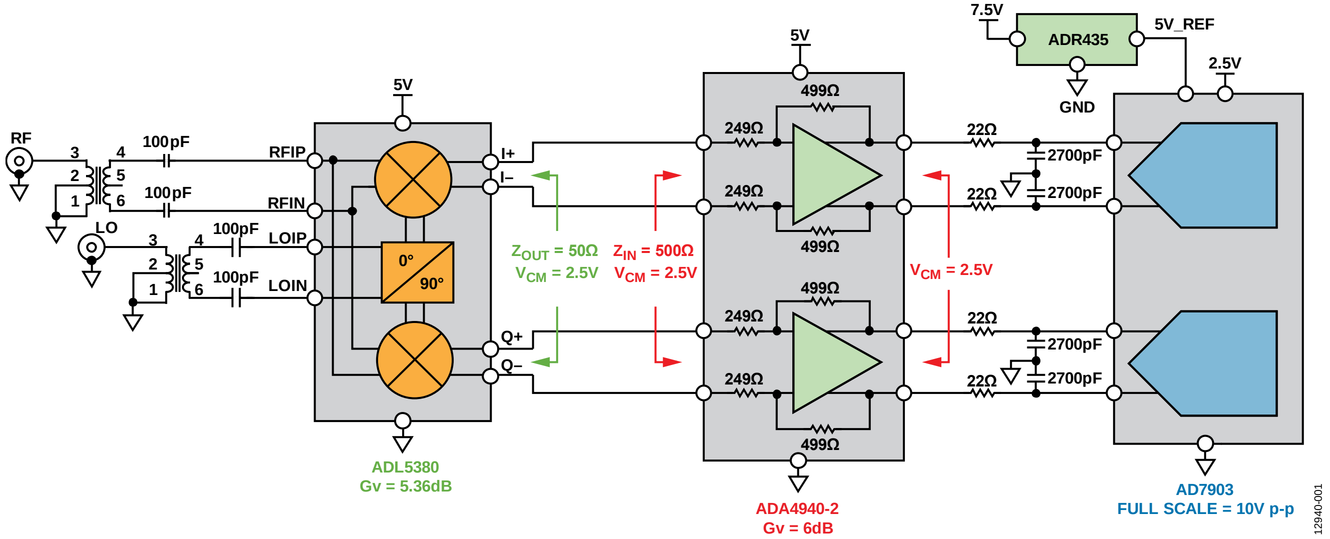

RF
3
4
2
5
1
6
100pF
100pF
RFIP
RFIN
LO
3
4
2
5
1
6
100pF
100pF
LOIP
LOIN
5V
0°
90°
I+
I–
Q+
Q–
ADL5380
Gv = 5.36dB
Z_{OUT} = 50Ω
V_{CM} = 2.5V
Z_{IN} = 500Ω
V_{CM} = 2.5V
5V
249Ω
249Ω
249Ω
249Ω
499Ω
499Ω
499Ω
499Ω
ADA4940-2
Gv = 6dB
V_{CM} = 2.5V
22Ω
22Ω
22Ω
22Ω
2700pF
2700pF
2700pF
2700pF
7.5V
ADR435
GND
5V_REF
2.5V
AD7903
FULL SCALE = 10V p-p
12940-001

Figure 1. Simplified Receiver Subsystem for Magnitude and Phase Measurements (All Connections and Decoupling Not Shown)

Rev. 0

Circuits from the Lab reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
www.analog.com
Fax: 781.461.3113
©2015 Analog Devices, Inc. All rights reserved.

CIRCUIT DESCRIPTION

Quadrature Demodulator

A quadrature demodulator provides an in-phase (I) signal and a quadrature (Q) signal that are exactly 90° out of phase. The I and Q signals are vector quantities; therefore, the amplitude and phase shift of the received signal can be calculated using trigonometric identities, as shown in Figure 2. The local oscillator (LO) input is the original transmitted signal and the RF input is the received signal. The demodulator generates a sum and difference term. Both the RF and LO signals are at the exact same frequency, $\omega_{LO} = \omega_{RF}$, and therefore the high frequency sum term is filtered, while the difference term resides at dc. The received signal has a different phase (φ_{RF}) than that of the transmitted signal (φ_{LO}), and this phase shift can be represented as $\varphi_{LO} - \varphi_{RF}$.

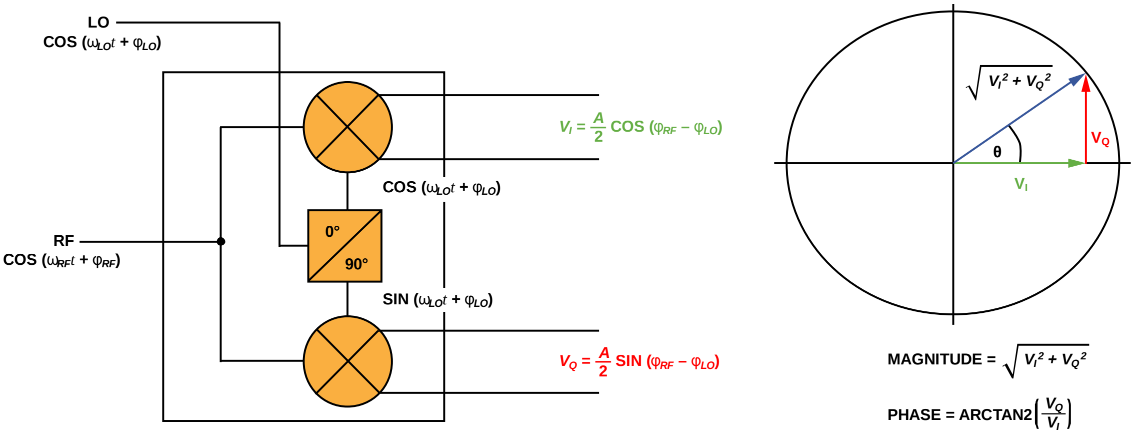
A real-world I/Q demodulator has many imperfections, including quadrature phase error, gain imbalance, and LO to RF leakage, all of which can degrade the quality of the demodulated signal. To select a demodulator, first determine the requirements for RF input frequency range, amplitude accuracy, and phase accuracy.

Powered from a single 5 V supply, the ADL5380 demodulator accepts RF or IF input frequencies from 400 MHz to 6 GHz, making it ideal for the receiver signal chain. Configured to provide a 5.36 dB voltage conversion gain, the differential I and Q outputs of the ADL5380 can drive a 2.5 V p-p differential signal into a 500 Ω load. Its 10.9 dB noise figure (NF), 11.6 dBm first-order intercept (IP1), and 29.7 dBm third-order intercept (IP3) at 900 MHz provide outstanding dynamic range; and its 0.07 dB amplitude balance and 0.2° phase balance achieve excellent demodulation accuracy. Manufactured using an advanced SiGe bipolar process, the ADL5380 is available in a tiny 4 mm × 4 mm, 24-lead LFCSP package.

ADC Driver and High Resolution Precision ADC

The excellent dynamic performance and adjustable output common-mode voltage of the ADA4940-2 fully differential dual amplifier make it ideal for driving high resolution, dual SAR ADCs. Powered from a single 5 V supply, the ADA4940-2 provides ±5 V differential outputs with a 2.5 V common-mode voltage. Configured to provide a gain of 2 (6 dB), it drives the ADC inputs to full-scale. The RC filter (22 Ω/2.7 nF) limits the noise and reduces the kickback coming from the capacitive digital-to-analog converter (DAC) at the ADC input. Manufactured using a proprietary SiGe complementary bipolar process, the ADA4940-2 is available in a tiny 4 mm × 4 mm, 24-lead LFCSP package.

The AD7903 dual 16-bit, 1 MSPS SAR ADC offers excellent precision, with ±0.006% FS gain error and ±0.015 mV offset error. Operating from a single 2.5 V power supply, the AD7903 dissipates only 12 mW at 1 MSPS. The main goal of using a high resolution ADC is to achieve ±1° phase accuracy, especially when the input signal has a small dc amplitude. The 5 V reference required by the ADC is generated by the ADR435 low noise reference.


LO
COS ($\omega_{LO}t + \varphi_{LO}$)
RF
COS ($\omega_{RF}t + \varphi_{RF}$)
0°
90°
COS ($\omega_{LO}t + \varphi_{LO}$)
SIN ($\omega_{LO}t + \varphi_{LO}$)
$V_I = \frac{A}{2}$ COS ($\varphi_{RF} - \varphi_{LO}$)
$V_Q = \frac{A}{2}$ SIN ($\varphi_{RF} - \varphi_{LO}$)
$\sqrt{V_I^2 + V_Q^2}$
θ
V_Q
V_I
MAGNITUDE = $\sqrt{V_I^2 + V_Q^2}$
PHASE = ARCTAN2$\left(\frac{V_Q}{V_I}\right)$
12940-002

$$I = A\cos(\omega_{RF}t + \varphi_{RF}) \times \cos(\omega_{LO}t + \varphi_{LO}) = \frac{A}{2}[\cos(\underbrace{\omega_{RF}t - \omega_{LO}t}_{\substack{\text{Let } \omega_{RF} = \omega_{LO} \\ \text{difference term at dc}}} + \varphi_{RF} - \varphi_{LO}) + \cos(\underbrace{\omega_{RF}t + \omega_{LO}t}_{\text{Sum term gets filtered}} + \varphi_{RF} + \varphi_{LO})]$$

$$V_I = \frac{A}{2}[\cos(\varphi_{RF} - \varphi_{LO})] \tag{1}$$

$$Q = A\cos(\omega_{RF}t + \varphi_{RF}) \times \sin(\omega_{LO}t + \varphi_{LO}) = \frac{A}{2}[\sin(\underbrace{\omega_{RF}t - \omega_{LO}t}_{\substack{\text{Let } \omega_{RF} = \omega_{LO} \\ \text{difference term at dc}}} + \varphi_{RF} - \varphi_{LO}) + \sin(\underbrace{\omega_{RF}t + \omega_{LO}t}_{\text{Sum term gets filtered}} + \varphi_{RF} + \varphi_{LO})]$$

$$V_Q = \frac{A}{2}[\cos(\varphi_{RF} - \varphi_{LO})] \tag{2}$$

Figure 2. Magnitude and Phase Measurement Using a Quadrature Demodulator

COMMON VARIATIONS

The frequency range of the circuit can be extended to lower frequencies by using the ADL5387 30 MHz to 2 GHz quadrature demodulator.

Depending on the specific application, the amplifier between the demodulator and ADC may or may not be necessary. The ADL5380 can interface directly to the AD7903 because the common-mode voltages of both devices are compatible. If using an alternative ADC with a common-mode voltage that is not within the range of the demodulator, an amplifier is necessary to achieve the level translation with minimal power loss.

The AD798x and AD769x family of ADCs can be used as alternatives to the AD7903.

CIRCUIT EVALUATION AND TEST

As shown in Figure 3, the receiver subsystem is implemented using the ADL5380-EVALZ, ADA4940-2ACP-EBZ, EVAL-AD7903SDZ, and EVAL-SDP-CB1Z evaluation kits. These circuit components are optimized for interconnection in the subsystem. Two high frequency, phase-locked input sources provide the RF and LO input signals.

Table 1 summarizes the input and output voltage levels for each of the components in the receiver subsystem. An 11.6 dBm signal at the RF input of the demodulator produces an input within −1 dB of the ADC full-scale range. Table 1 assumes a 500 Ω load, 5.3573 dB conversion gain, and −4.643 dB power gain for the ADL5380, and 6 dB gain for the ADA4940-2. The calibration routine and performance results achieved for this receiver subsystem are discussed in the following sections.

Table 1. Input and Output Voltage Levels of Figure 1

RF Input	ADL5380 Output		AD7903 Input
+11.6 dBm	+6.957 dBm	4.455 V p-p	−1.022 dBFS
0 dBm	−4.643 dBm	1.172 V p-p	−12.622 dBFS
−20 dBm	−24.643 dBm	0.117 V p-p	−32.622 dBFS
−40 dBm	−44.643 dBm	0.012 V p-p	−52.622 dBFS
−68 dBm	−72.643 dBm	466 μV p-p	−80.622 dBFS

Receiver Subsystem Error Calibration

The receiver subsystem contains three major error sources: offset, gain, and phase.

The individual differential dc magnitudes of the I and Q channels have sinusoidal relationships with respect to the relative phase of the RF and LO signals. As a result, the ideal dc magnitude of the I and Q channels can be calculated as follows:

$$\text{Voltage } I_{CHANNEL} = \text{Max I/Q Output} \times \cos(\theta) \quad (3)$$

$$\text{Voltage } Q_{CHANNEL} = \text{Max I/Q Output} \times \sin(\theta) \quad (4)$$

As the phase moves through the polar grid, some locations ideally produce the same voltage. For example, the voltage on the I (cosine) channel should be identical with phase shifts of +90° or −90°. However, a constant phase shift error, independent of the relative phase of RF and LO, causes the subsystem channel to generate different results for input phases that should produce the same dc magnitude. This is illustrated in Figure 4 and Figure 5, where two different output codes are generated when the input should be at 0 V. In this case, the −37° phase shift is much larger than expected in a real-world system containing phase-locked loops. The result is +90° actually appearing as +53°, and −90° as −127°.

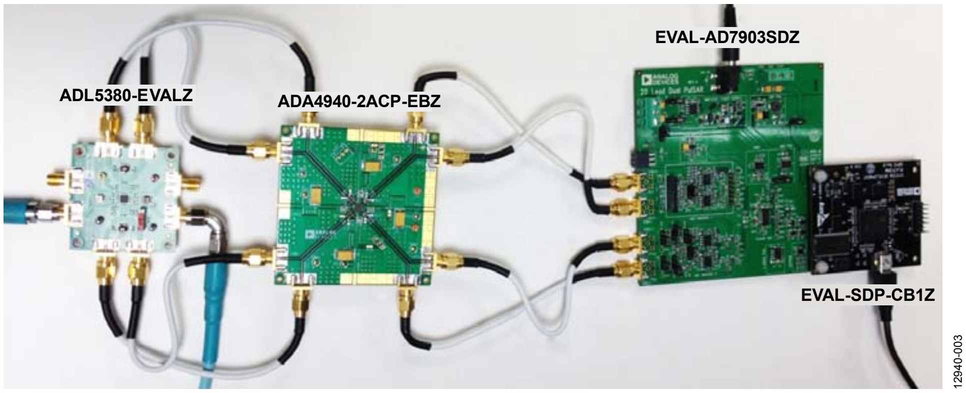


Figure 3. Receiver Subsystem Evaluation Platform

Table 2 Measured Phase Shift for 0 dBm RF Input

Input Phase RF to LO	Average I Channel Output Code	Average Q Channel Output Code	I Channel Voltage	Q Channel Voltage	Measured Phase	Measured Receiver Subsystem Phase Shift
−180°	−5851.294	+4524.038	−0.893 V	+0.690 V	+142.29°	−37.71°
−90°	−4471.731	−5842.293	−0.682 V	−0.891 V	−127.43°	−37.43°
0°	+5909.982	−4396.769	+0.902 V	−0.671 V	−36.65°	−36.65°
+90°	+4470.072	+5858.444	+0.682 V	+0.894 V	+52.66°	−37.34°
+180°	−5924.423	+4429.286	−0.904 V	+0.676 V	+143.22°	−36.78°

Results were gathered in 10° steps from −180° to +180°, with the uncorrected data generating the elliptical shapes shown in Figure 4 and Figure 5. This error can be accounted for by determining the amount of additional phase shift present in the system. Table 2 shows that the system phase shift error is constant throughout the transfer function.

System Phase Error Calibration

With a step size of 10°, the average measured phase shift error was −37.32° for the system shown in Figure 3. With this additional phase shift known, the adjusted subsystem dc voltages can now be calculated. The variable φ_{PHASE_SHIFT} is defined as the average observed additional system phase shift. The dc voltage generated in the phase-compensated signal chain can be computed as

$$\text{Voltage } I_{CHANNEL} = \text{Max I/Q Output} \times (\cos(\theta_{TARGET})\cos(\varphi_{PHASE\_SHIFT}) - \sin(\theta_{TARGET})\sin(\varphi_{PHASE\_SHIFT})) \quad (5)$$

$$\text{Voltage } Q_{CHANNEL} = \text{Max I/Q Output} \times (\sin(\theta_{TARGET})\cos(\varphi_{PHASE\_SHIFT}) + \cos(\theta_{TARGET})\sin(\varphi_{PHASE\_SHIFT})) \quad (6)$$

Equation 5 and Equation 6 provide the target input voltage for a given phase setting. The subsystem has now been linearized, and the offset error and gain error can now be corrected. The linearized I and Q channel results can also be seen in Figure 4 and Figure 5. A linear regression on the data sets generates the best fit line shown in the figures. This line is the measured subsystem transfer function for each conversion signal chain.

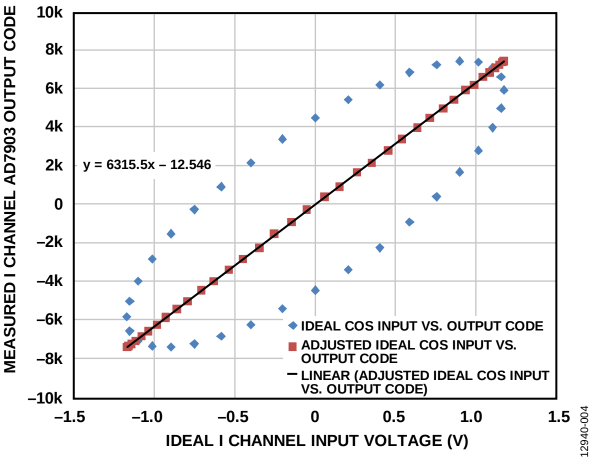


Figure 4. Linearized I Channel Results

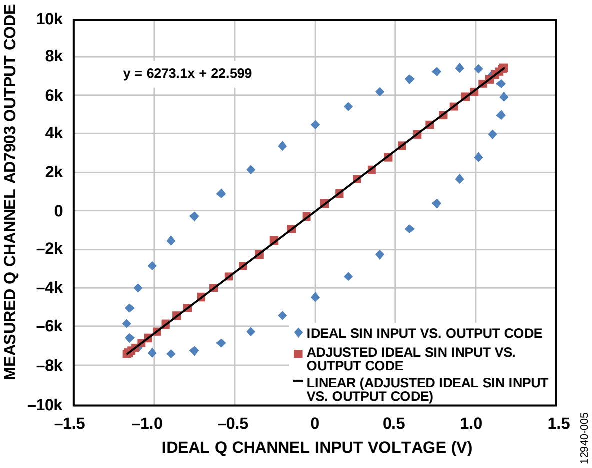


Figure 5. Linearized Q Channel Results

System Offset and Gain Error Calibration

The offset of each signal chain within the receiver subsystem is ideally 0 LSB; however, the measured offsets were −12.546 LSB and +22.599 LSB for the I and Q channels, respectively. The slope of the best fit line represents the slope of the subsystem. The ideal subsystem slope can be calculated as

$$\text{Ideal Slope} = \frac{\text{Max Code} - \text{Min Code}}{+V_{REF} - (-V_{REF})} = \frac{65{,}535 - 0}{+5 - (-5)} = 6553.5\,\frac{\text{Codes}}{\text{V}} \quad (7)$$

The results in Figure 4 and Figure 5 show that that measured slopes were 6315.5 and 6273.1 for the I and Q channels, respectively. These slopes must be adjusted to correct the system gain error. Correcting for gain error and offset error ensures that the signal magnitude computed using Equation 1 matches the ideal signal magnitude. The offset correction is the opposite of the measured offset error:

$$\text{Offset Error Correction} = -\text{Measured Offset Error} \quad (8)$$

The gain error correction coefficient is

$$\text{Gain Error Correction} = \frac{\text{Ideal Slope}}{\text{Measured Slope}} \quad (9)$$

The received conversion result can be corrected by

$$\mathit{Corrected\ Output\ Code} = \frac{\mathit{Received\ Output\ Code} \times \mathit{Ideal\ Slope}}{\mathit{Measured\ Slope}} + \mathit{Offset\ Error\ Correction} \quad (10)$$

The calibrated dc input voltage of the subsystem is calculated as

$$\mathit{Measured\ Signal\ Input\ Voltage} = \frac{2 \times V_{REF} \times \mathit{Corrected\ Output\ Code}}{2^N - 1} \quad (11)$$

Use Equation 11 on both the I and Q channels to compute the perceived analog input voltage for each subsystem signal chain. These fully adjusted I and Q channel voltages are used to compute the RF signal amplitude as defined by the individual dc signal magnitudes. To evaluate the accuracy of the full calibration routine, convert the collected results to ideal subsystem voltages produced at the output of the demodulator as if no phase shift error were present; multiply the average dc magnitude computed previously by the sinusoidal fraction of the measured phase at each trial with the computed phase shift error removed. The calculation is as follows:

$$\mathit{Fully\ Corrected\ I\ Channel\ Voltage} = \mathit{Average\ Post\ Calibration\ Magnitude} \times (\cos(\theta_{MEASURED})\cos(\varphi_{PHASE\_SHIFT}) + \sin(\theta_{MEASURED})\sin(\varphi_{PHASE\_SHIFT})) \quad (12)$$

$$\mathit{Fully\ Corrected\ Q\ Channel\ Voltage} = \mathit{Average\ Post\ Calibration\ Magnitude} \times (\sin(\theta_{MEASURED})\cos(\varphi_{PHASE\_SHIFT}) - \cos(\theta_{MEASURED})\sin(\varphi_{PHASE\_SHIFT})) \quad (13)$$

where:

φ_{PHASE_SHIFT} is the phase error previously computed.

Average Post Calibration Magnitude is the dc magnitude result from Equation 1 that has been compensated for offset error and gain error.

Table 3 shows the results of the calibration routine at various target phase inputs for the 0 dBm RF input amplitude case. The calculations performed in Equation 12 and Equation 13 are the correction factors to be built into any system intended to sense phase and magnitude in the manner described in this circuit note.

Table 3. Results Achieved at Certain Target Phase Inputs with 0 dBm RF Input Amplitude

Target Phase	I Channel Fully Corrected Input Voltage	Q Channel Fully Corrected Input Voltage	Fully Corrected Phase Result	Absolute Measured Phase Error
−180°	−1.172 V	+0.00789 V	−180.386°	0.386°
−90°	−0.00218 V	−1.172 V	−90.107°	0.107°
0°	+1.172 V	+0.0138 V	+0.677°	0.676°
+90°	+0.000409 V	+1.171 V	+89.98°	0.020°
+180°	−1.172 V	−0.0111 V	+180.542°	0.541°

Figure 6 is a histogram of the measured absolute phase error showing better than 1° accuracy for every 10° step from −180° to +180°.

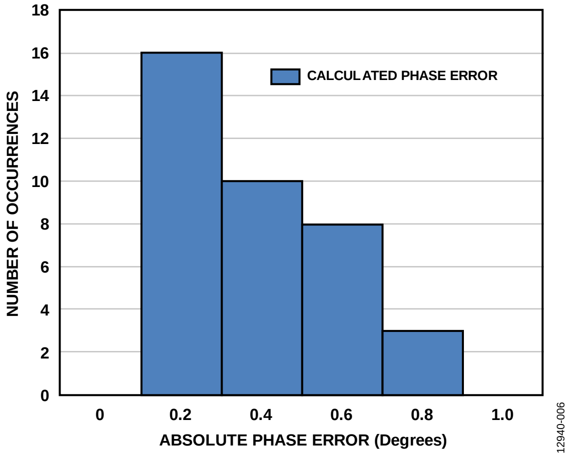


Figure 6. Measured Absolute Phase Error Histogram for 0 dBm Input Level with 10° Phase Steps

For accurate phase measurements at any given input level, the perceived phase shift error (φ_{PHASE_SHIFT}) of RF relative to LO must be constant. If the measured phase shift error begins to change as a function of the target phase step (θ_{TARGET}) or amplitude, the calibration routine presented in this section begins to lose accuracy. Evaluation results at room temperature show that the phase shift error is relatively constant for RF amplitudes ranging from a maximum of 11.6 dBm to approximately −20 dBm at 900 MHz.

Figure 7 shows the dynamic range of the receiver subsystem along with the corresponding amplitude-induced additional phase error. As the input amplitude decreases past −20 dBm, the phase error calibration accuracy begins to degrade. The system user must determine the acceptable level of signal chain error to determine the minimum acceptable signal magnitude.

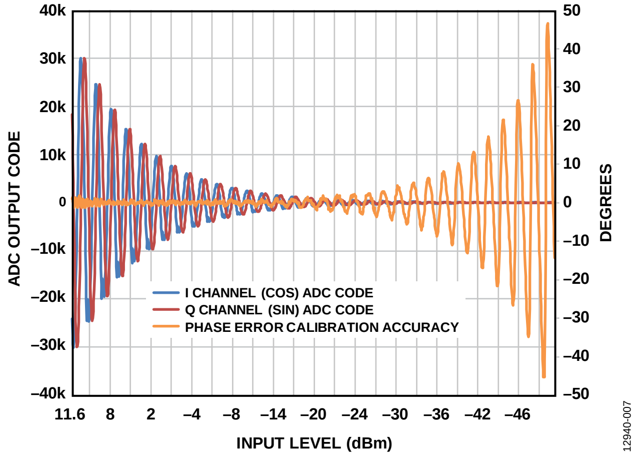


Figure 7. Dynamic Range of Receiver Subsystem and Corresponding Additional Phase Error

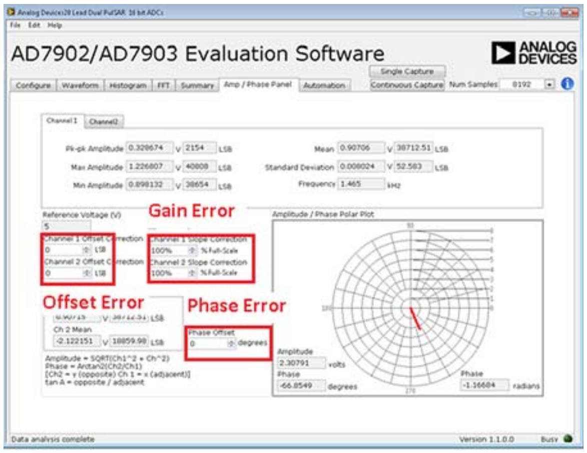
The results shown in Figure 7 were collected with a 5 V ADC reference. The magnitude of the ADC reference can be reduced, providing a smaller quantization level for the system, which provides an incremental improvement in phase error accuracy for small signals but increases the chance for system saturation. To increase system dynamic range, another option is to implement an oversampling scheme that increases the noise-free bit resolution of the ADC. Every doubling in samples averaged provides a ½ LSB increase in system resolution. The oversampling ratio for a given resolution increase is calculated as follows:

$$Oversampling\ Ratio = 2^{2N} \quad (14)$$

where N is the number of bits increase.

Oversampling reaches a point of diminishing returns when the noise amplitude is no longer sufficient to randomly change the ADC output code from sample to sample. At this point, the effective resolution of the system can no longer be increased. The bandwidth reduction from oversampling is not a significant concern because the system is measuring signals with a slowly changing magnitude.

The AD7903 evaluation software is available with a calibration routine that allows the user to correct the ADC output results for the three sources of error: phase, gain, and offset. The user must collect uncorrected results with their system to determine the calibration coefficients calculated in this circuit note. Figure 8 shows the **Amp/Phase Panel** tab of the GUI with the calibration coefficients highlighted. When the coefficients are determined, this tab can also be used to deliver phase and magnitude results from the demodulator. The polar plot provides a visual indication of the observed RF input signal. The amplitude and phase calculations are performed using Equation 1 and Equation 2. The oversampling ratio can be controlled by adjusting the number of samples per capture using the **Num Samples** drop-down box.


Analog Devices 28 Lead Dual PulSAR 16 bit ADCs
File
Edit
Help
AD7902/AD7903 Evaluation Software
Single Capture
Configure
Waveform
Histogram
FFT
Summary
Amp / Phase Panel
Automation
Continuous Capture
Channel 1
Channel2
Gain Error
Offset Error
Phase Error
Amplitude / Phase Polar Plot
12940-008

Num Samples 8192

Pk-pk Amplitude 0.328674 V 2154 LSB

Max Amplitude 1.226807 V 40808 LSB

Min Amplitude 0.898132 V 38654 LSB

Mean 0.90706 V 38712.51 LSB

Standard Deviation 0.008024 V 52.583 LSB

Frequency 1.465 kHz

Reference Voltage (V) 5

Channel 1 Offset Correction 0 LSB

Channel 2 Offset Correction 0 LSB

Channel 1 Slope Correction 100% % Full-Scale

Channel 2 Slope Correction 100% % Full-Scale

Ch 2 Mean -2.122151 V 18859.98 LSB

Phase Offset 0 degrees

Amplitude = SQRT(Ch1^2 + Ch^2)
Phase = Arctan2(Ch2/Ch1)
[Ch2 = y (opposite) Ch 1 = x (adjacent)]
tan A = opposite / adjacent

Amplitude 2.30791 volts

Phase -66.8549 degrees

Phase -1.16684 radians

Data analysis complete

Version 1.1.0.0 Busy

Figure 8. Receiver Subsystem Calibration GUI

Equipment Needed

The following equipment are used to evaluate the circuit.

- A Windows® XP, Windows Vista (32-bit), or Windows 7 (32-bit) PC with USB port
- The ADL5380-EVALZ, ADA4940-2ACP-EBZ, EVAL-AD7903SDZ, and EVAL-SDP-CB1Z evaluation boards
- Two RF signal generators with phase control (such as the R&S SMT06)
- A digital multimeter
- 5 V and 9 V power supplies
- The AD7903 evaluation software, used to digitally process the resulting magnitude and phase information

Figure 9 shows a block diagram of the test setup.

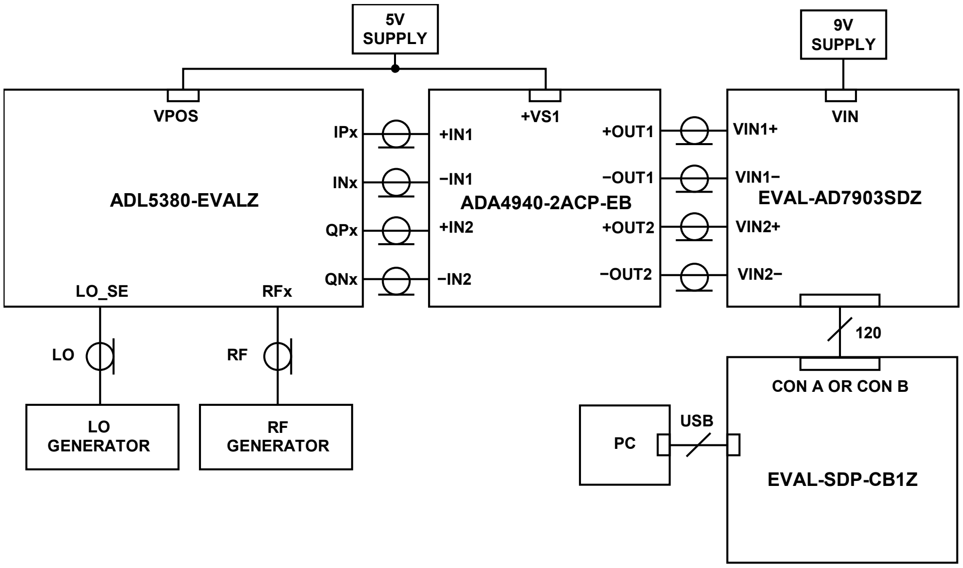

5V SUPPLY
9V SUPPLY
VPOS
ADL5380-EVALZ
IPx
INx
QPx
QNx
LO_SE
RFx
+VS1
+IN1
−IN1
ADA4940-2ACP-EB
+IN2
−IN2
+OUT1
−OUT1
+OUT2
−OUT2
VIN
VIN1+
VIN1−
EVAL-AD7903SDZ
VIN2+
VIN2−
120
CON A OR CON B
EVAL-SDP-CB1Z
USB
PC
LO
RF
LO GENERATOR
RF GENERATOR
12940-009

Figure 9. Test Setup Functional Diagram

LEARN MORE

CN-0374 Design Support Package: www.analog.com/CN0374-DesignSupport

UG-609. EVAL-AD7903SDZ Evaluation Board User Guide. Analog Devices.

UG-018. Evaluation Board for High Speed Differential Amplifiers. Analog Devices.

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*. Analog Dialogue 39-09, September 2005.

ADIsimRF Design Tool.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

Ryan Curran, Qui Luu, Maithil Pachchigar. *RF-to-Bits Solution Offers Precise Phase and Magnitude Data for Material Analysis.* Analog Dialogue 48-4, October 2014.

Data Sheets and Evaluation Boards

ADL5380 Data Sheet and Evaluation Board

ADA4940-2 Data Sheet and Evaluation Board

AD7903 Data Sheet and Evaluation Board

REVISION HISTORY

1/15—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab reference designs are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab reference designs in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab reference designs are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab reference designs at any time without notice but is under no obligation to do so.

©2015 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

CN12940-0-1/15(0)

ANALOG DEVICES

Circuit Note
CN-0369

Devices Connected/Referenced	
ADL5801	High IP3,10 MHz to 6 GHz, Active Mixer
HMC512	VCO with Fo/2 & Divide-by-4 SMT, 9.6 GHz to 10.8 GHz
ADF4355-2	Microwave Wideband Synthesizer with Integrated VCO
AD8065	High Performance, 145 MHz FastFET Op Amp
ADP151	Ultralow Noise, 200 mA, CMOS Linear Regulator
ADM7150	800 mA Ultralow Noise, High PSRR, RF Linear Regulator
ADF4002	Phase Detector/PLL Frequency Synthesizer

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0369.

Translation Phase Locked Loop Synthesizer with Low Phase Noise

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

- **CN-0369 Circuit Evaluation Board (EVAL-CN0369-SDPZ)**
- **System Demonstration Platforms (EVAL-SDP-CS1Z)**
- **ADL5801 Evaluation Board (ADL5801-EVALZ)**
- **ADF4355-2 Evaluation Board (EV-ADF4355-2SD1Z)**

Design and Integration Files

- **Schematics, Layout Files, Bill of Materials**

CIRCUIT FUNCTION AND BENEFITS

The circuit block diagram shown in Figure 1 is a low phase noise translation loop synthesizer (also known as an offset loop). This circuit translates the lower 100 MHz reference frequency of the ADF4002 phase locked loop (PLL) up to a higher frequency range of 5.0 GHz to 5.4 GHz, as determined by the frequency of the local oscillator (LO).

The translation loop synthesizer has very low phase noise (<50 fs) in contrast to a synthesizer using only a PLL. The low phase noise is because of the very low N value used by the ADF4002 integer-N PLL, which controls the voltage controlled oscillator (VCO). In this example, the ADF4002 phase frequency detector (PFD) runs at 100 MHz, and N = 1, yielding phase noise performance that is not limited by the N value of the PLL.

Rev. 0
Circuits from the Lab reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
www.analog.com
Fax: 781.461.3113

©2016 Analog Devices, Inc. All rights reserved.

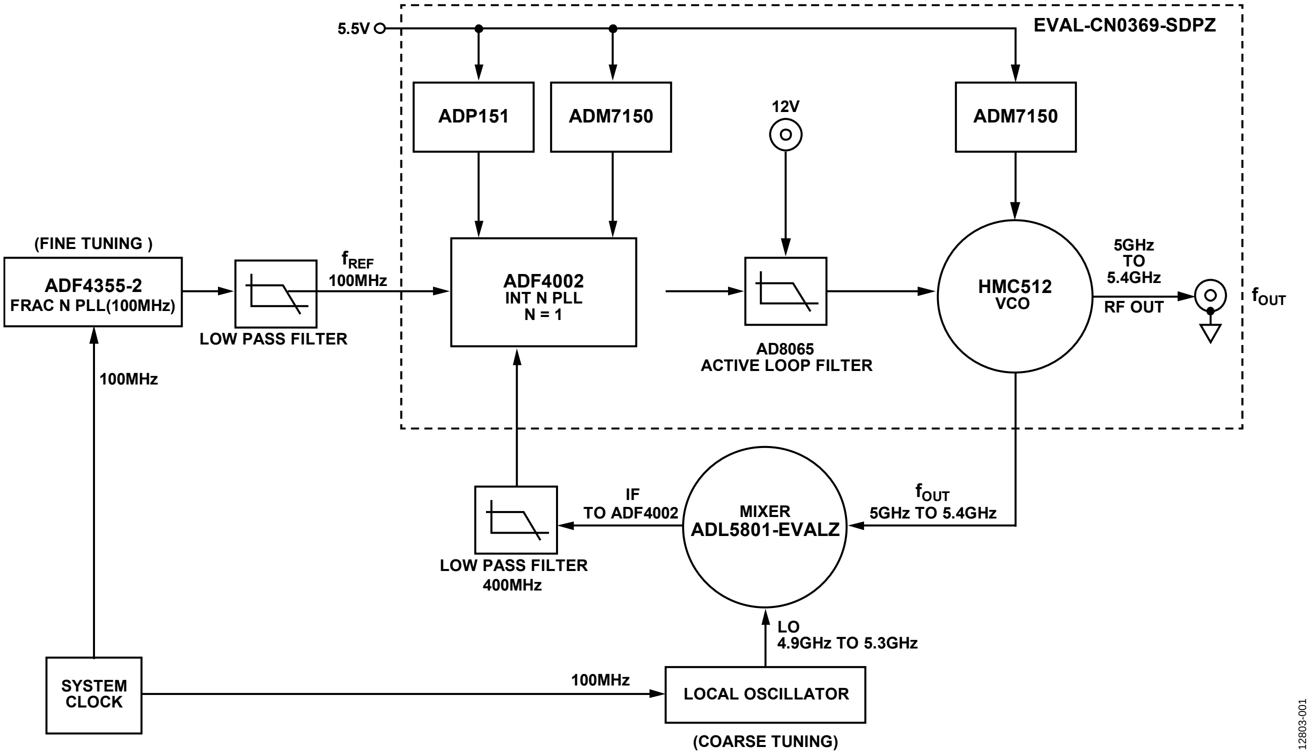

5.5V
EVAL-CN0369-SDPZ
ADP151
ADM7150
12V
ADM7150
(FINE TUNING)
ADF4355-2
FRAC N PLL(100MHz)
f_{REF}
100MHz
LOW PASS FILTER
ADF4002
INT N PLL
N = 1
AD8065
ACTIVE LOOP FILTER
HMC512
VCO
5GHz
TO
5.4GHz
RF OUT
f_{OUT}
100MHz
IF
TO ADF4002
MIXER
ADL5801-EVALZ
f_{OUT}
5GHz TO 5.4GHz
LOW PASS FILTER
400MHz
LO
4.9GHz TO 5.3GHz
SYSTEM
CLOCK
100MHz
LOCAL OSCILLATOR
(COARSE TUNING)
12803-001

Figure 1. Block Diagram of the Translation Loop Synthesizer

CIRCUIT DESCRIPTION

In a standard PLL and VCO frequency synthesizer system, low phase noise is generally the primary objective. The phase noise in a PLL can be described as having two components: a flat noise component known as the PLL figure of merit (FOM), and a 1/f noise profile component known as the PLL 1/f, or flicker noise.

The PLL noise floor, PN_{TOT1}, is given by

$$PN_{TOT1} = PN_{SYNTH} + 20\log_{10}(N) + 10\log_{10}(f_{PFD}) \quad (1)$$

where:
PN_{SYNTH} is the synthesizer FOM and is device specific.
N is the divider used by the PLL.
f_{PFD} is the frequency of the phase frequency detector.

A PLL whose N value = 1 has a noise floor of $10\log_{10}(f_{PFD})$.

The PLL 1/f noise, PN_{TOT2}, is given by

$$PN_{TOT2} = PN_{1/f} + 20\log_{10}(f_{RF}/1\text{ GHz}) + 10\log_{10}(10\text{ kHz}/f) \quad (2)$$

where:
$PN_{1/f}$ is the data sheet PLL 1/f noise at an offset of 10 kHz from the output RF frequency (normalised to a 1 GHz output).
f_{RF} is the output RF frequency.

The total PLL noise, PN_{TOT}, is given by

$$PN_{TOT} = \sqrt{(PN_{TOT1})^2 + (PN_{TOT2})^2} \quad (3)$$

This equation indicates that the noise sources add in root-sum-square fashion; therefore, the larger noise source dominates.

A PLL with a very low N value has a phase noise dominated by the PLL 1/f noise.

The translation loop synthesizer decouples the required channel spacing from the N divider value to optimize the phase noise of the PLL. In this translation loop synthesizer example, N = 1.

The translation loop synthesizer in Figure 1 locks the higher frequency 4.8 GHz to 5.2 GHz VCO to the 100 MHz f_{REF} signal. The ADL5801 mixer and the LO together perform the divider function of this PLL.

With the LO in the feedback loop, the balance equation at the ADF4002 PLL becomes

$$f_{REF}/R = (f_{OUT} - f_{LO})/N$$

where N and R are the N and R divider values (in this circuit, R = 1 and N = 1).

The output frequency is therefore given by

$$f_{OUT} = f_{LO} + f_{REF}$$

ADF4355-2 Fractional-N Synthesizer

The ADF4355-2 in this circuit provides the reference frequency (f_{REF}) for the translation loop as shown in Figure 2.

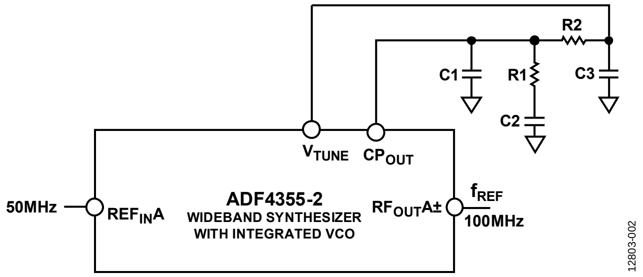

R2
C1
R1
C3
C2
V_{TUNE}
CP_{OUT}
50MHz
$REF_{IN}A$
ADF4355-2
WIDEBAND SYNTHESIZER
WITH INTEGRATED VCO
$RF_{OUT}A\pm$
f_{REF}
100MHz
12803-002

Figure 2. ADF4355-2 and Loop Filter

The ADF4355-2 is a wideband synthesizer with an integrated VCO providing an output frequency range from 55 MHz to 4400 MHz. The ADF4355-2 uses a high-resolution 38-bit modulus that allows very fine frequency resolution with no residual frequency error. The ADF4355-2 in this circuit uses a PFD of 50 MHz, and a loop bandwidth of 100 kHz. The Analog Devices ADIsimPLL tool was used to design and simulate the loop filter. Figure 3 shows the phase noise performance simulated by ADIsimPLL. A loop bandwidth (LBW) of 100 kHz was used, which is sufficient to allow the ADF4355-2 to provide the fine frequency tuning required.

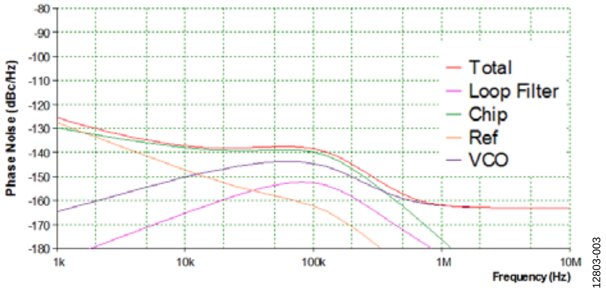
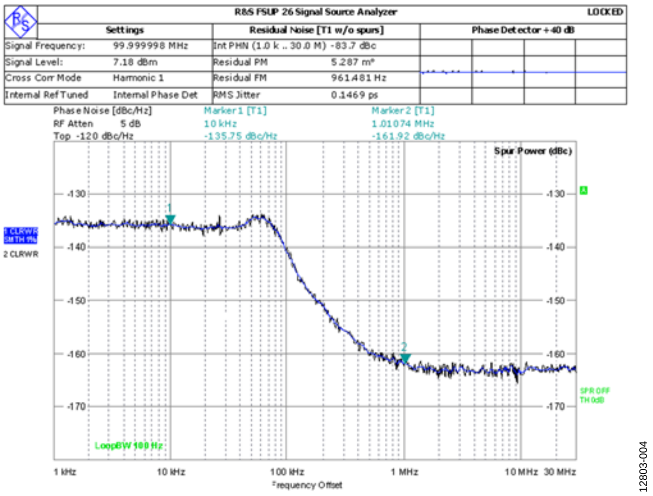


Figure 3. ADF4355-2 Simulated Output Phase Noise at 100 MHz from ADIsimPLL

The ADF4355-2 in this design operates with an internal VCO frequency of 6400 MHz. This high VCO frequency is divided by the maximum divider value of 64 to generate the 100 MHz RF output frequency. Adding a divider to the output of the VCO results in a 6 dB improvement in phase noise for each divide by 2. The divided VCO output contains harmonics inherent to the division process. A 100 MHz low pass filter is inserted at the RF output of the ADF4355-2 to filter these harmonics.

The simulated phase noise at an offset of 10 kHz is −137 dBc. The ADF4355-2 is the reference of choice for this translation loop because of its very low phase noise performance and very fine output frequency resolution.

Figure 4 shows a phase noise plot taken at the RFOUTA of the EV-ADF4355-2SD1Z.



R&S FSUP 26 Signal Source Analyzer LOCKED

Settings		Residual Noise [T1 w/o spurs]	
Signal Frequency:	99.999998 MHz	Int PHN (1.0 k .. 30.0 M)	-83.7 dBc
Signal Level:	7.18 dBm	Residual PM	5.287 m°
Cross Corr Mode	Harmonic 1	Residual FM	961.481 Hz
Internal Ref Tuned	Internal Phase Det	RMS Jitter	0.1469 ps

Phase Noise [dBc/Hz]
RF Atten 5 dB
Top -120 dBc/Hz

Marker 1 [T1]
10 kHz
-135.75 dBc/Hz

Marker 2 [T1]
1.01074 MHz
-161.92 dBc/Hz

Figure 4. ADF4355-2, f_{OUT} = 100 MHz

ADF4002 Translation Loop Frequency Synthesizer

The ADF4002 is the translation loop frequency synthesizer, operating at a high PFD frequency of 100 MHz and a minimum N = 1. Operating at a high PFD frequency decreases the reference spurs and lowers N and thus phase noise. The translation loop frequency synthesizer uses integer-N PLL operation instead of fractional-N for better spurious performance. The ADF4002 meets the requirements for integer-N operation, a low minimum N value, and good phase noise performance. Fractional-N is not required because fine tuning is provided by the reference source. In this circuit, the RF input of the ADF4002 is driven by the 100 MHz IF output of the ADL5801 mixer.

The supply voltage for the ADF4002 internal charge pump is 5 V. However, many wideband VCOs require a tuning voltage of up to 18 V. A tuning voltage of 2 V to 12 V is required to drive the 9.6 GHZ to 10.8 GHz VCO. To accommodate this, an active loop filter is required. The active filter multiplies the output tuning range of the ADF4002 by the gain of the op amp.

The ADF4002 supports a programmable charge pump current feature that allows the user to modify the loop filter dynamics without changing the physical components. In this circuit, the LBW is 1 MHz using a charge pump current of 5 mA. The charge pump current can be modified to reduce or increase the LBW without physically changing the loop filter components.

Active Filter Using the AD8065

The AD8065 op amp has a 24 V supply voltage range, a gain bandwidth product (GBP) of approximately 145 MHz, and low noise (7 nV/√Hz). These features make it ideal for an active filter. For this application, a supply voltage of 12 V for the AD8065 is sufficient to provide the required output swing.

For most PLL applications, a phase margin of 45° to 55° is recommended to maintain a stable loop and to minimize settling time. In an active loop filter, that is, when there is an op amp in a loop filter, an additional pole occurs at the unity gain frequency (or gain bandwidth product) of the op amp. This additional pole adds extra phase lag; therefore, depending on the frequency of the pole, it can render the loop unstable.

The higher the ratio of GBP to LBW, the less phase lag. For example, Table 1 shows that a GBP/LBW ratio of 10 reduces the phase margin by 5.7°. If the GBP/LBW ratio is too low, the phase margin also becomes too low and results in an unstable loop.

Table 1. Phase Lag as a Function of GBP:LBW Ratio

GBP/LBW Ratio	Extra Phase Lag (°)
5 (such as GBP = 1 MHz, LBW = 200 kHz)	11.3
10	5.7
20	2.9

This circuit uses a 1 MHz LBW; therefore, the 145 MHz GBP of the AD8065 results in negligible phase lag (GBP/LBW = 145).

The AD8065 also acts as a buffer to mitigate the input capacitance of the VCO.

HMC512 VCO

The ADF4002 PLL locks the 100 MHz reference frequency to the HMC512 VCO frequency. The HMC512 has a primary frequency range from 9.6 GHz to 10.8 GHz. In this circuit, RFOUT/2 is used for the output signal (f_{OUT}) as well as the feedback RF to the mixer. High reverse isolation is required between the RF output (f_{OUT}) and the mixer to minimize LO to RF leakage. Choosing a VCO with a half frequency output provides reverse isolation. The typical RFOUT/2 power level of 8 dBm requires a 6 dB attenuation pad to reduce the power level to the mixer RF input recommended levels; in effect giving an additional 6 dB of reverse isolation.

The wide loop filter bandwidth high passes the VCO noise within the loop filter bandwidth. Outside the loop filter bandwidth, the VCO noise dominates. Therefore, a low noise VCO is required to achieve the low phase noise benefits from the circuit. The low noise of −110 dBc/Hz at 100 kHz along with the half frequency output of the HMC512 makes it a component of choice as the VCO to generate a 5.0 GHz to 5.4 GHz output in this circuit.

Local Oscillator and ADL5801 Mixer

The mixer selection for the translation loop must meet the following requirements:

- Operates in the required frequency range
- LO power levels matching the LO source
- High RF to LO isolation
- Low noise figure

The ADL5801 meets these requirements.

Figure 5 shows a block diagram of the ADL5801 mixer and the local oscillator. In general, an active mixer such as the ADL5801 (10 MHz to 6000 MHz) provides the required wideband operation, 35 dB to 40 dB of port to port isolation, and allows a typical −6 dBm to 0 dBm LO drive. The LO leakage degrades the spectral purity of the output signal. A low LO drive plus port to port isolation minimize LO to RF and LO to IF leakage.

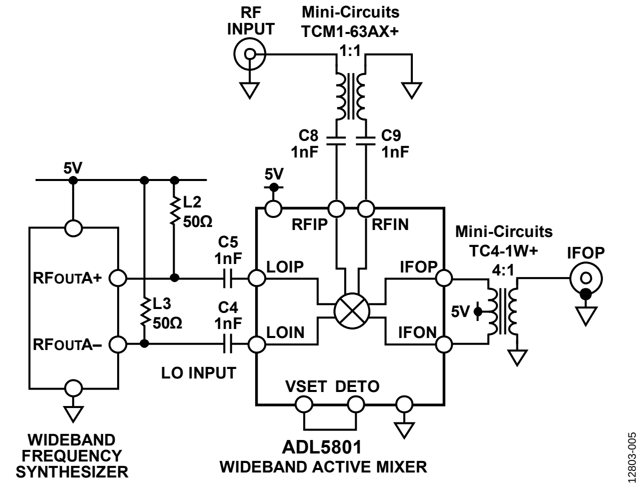

RF
INPUT
Mini-Circuits
TCM1-63AX+
1:1
C8
1nF
C9
1nF
5V
L2
50Ω
5V
C5
1nF
RFIP
RFIN
Mini-Circuits
TC4-1W+
4:1
IFOP
RFOUTA+
LOIP
IFOP
L3
50Ω
C4
1nF
5V
RFOUTA–
LOIN
IFON
LO INPUT
VSET DETO
WIDEBAND
FREQUENCY
SYNTHESIZER
ADL5801
WIDEBAND ACTIVE MIXER
12803-005

Figure 5. ADL5801 Mixer LO input

The local oscillator provides the coarse output frequency tuning in steps of 100 MHz with very low phase noise. For this circuit evaluation, the LO function is provided by a bench signal generator, such as the R&S SMA100.

Translation Loop Design and Performance

The core of this translation loop is the EVAL-CN0369-SDPZ board. Figure 6 shows a block diagram of the EVAL-CN0369-SDPZ, which uses the ADF4002 PLL, the AD8065 active loop filter, and the HMC512 VCO. The loop filter components for the active loop filter are shown in this diagram. ADIsimPLL is used to design the active loop filter.

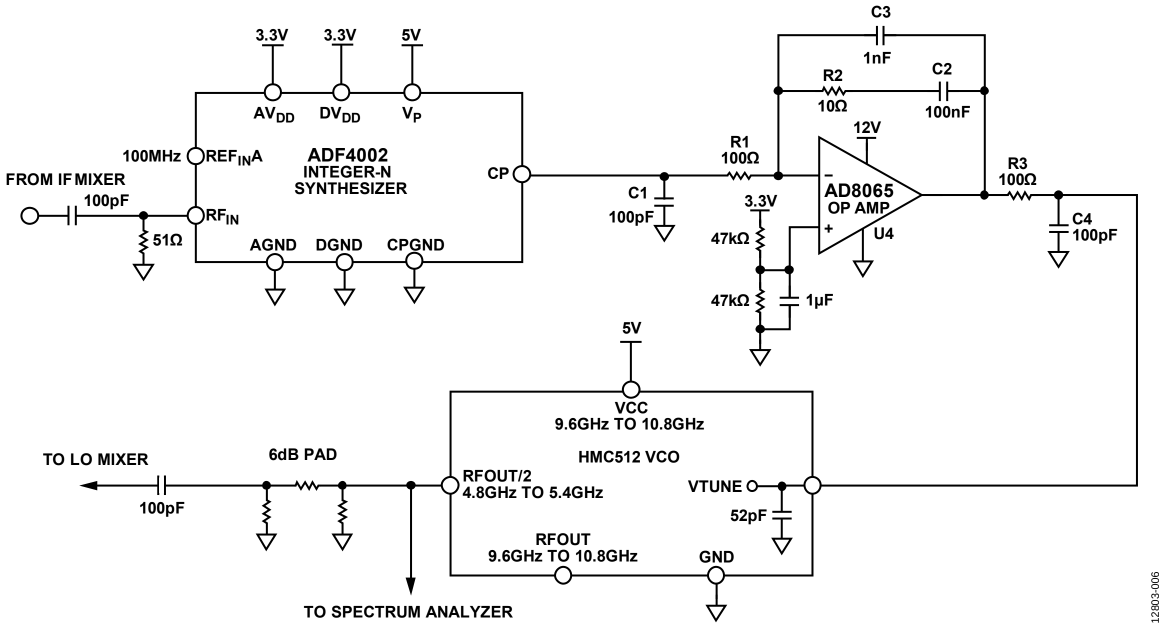

3.3V
3.3V
5V
AVDD
DVDD
VP
100MHz
REFINA
ADF4002
INTEGER-N
SYNTHESIZER
CP
FROM IF MIXER
100pF
RFIN
51Ω
AGND
DGND
CPGND
C3
1nF
R2
10Ω
C2
100nF
12V
R1
100Ω
C1
100pF
3.3V
47kΩ
47kΩ
1µF
AD8065
OP AMP
U4
R3
100Ω
C4
100pF
5V
VCC
9.6GHz TO 10.8GHz
HMC512 VCO
TO LO MIXER
6dB PAD
100pF
RFOUT/2
4.8GHz TO 5.4GHz
VTUNE
52pF
RFOUT
9.6GHz TO 10.8GHz
GND
TO SPECTRUM ANALYZER
12803-006

Figure 6. Block Diagram of EVAL-CN0369-SDPZ

The ADIsimPLL software is also used to design the loop filter of the translation loop PLL.

The simplest way to design a translation loop using ADIsimPLL is to replace the VCO/mixer/filter block with an equivalent VCO. If the VCO used tunes from 5.0 GHz to 5.4 GHz with K_V = 150 MHz/V, and the user mixes it with a 4.9 GHz to 5.3 GHz local oscillator, the PLL sees a VCO that tunes from 400 MHz to 100 MHz with K_V = 150 MHz/V.

Figure 7 shows the ADIsimPLL simulated phase noise and corresponding schematic using the ADF4002, and indicates that the PLL loop locks at 100 MHz with a minimum increase in the phase noise floor.

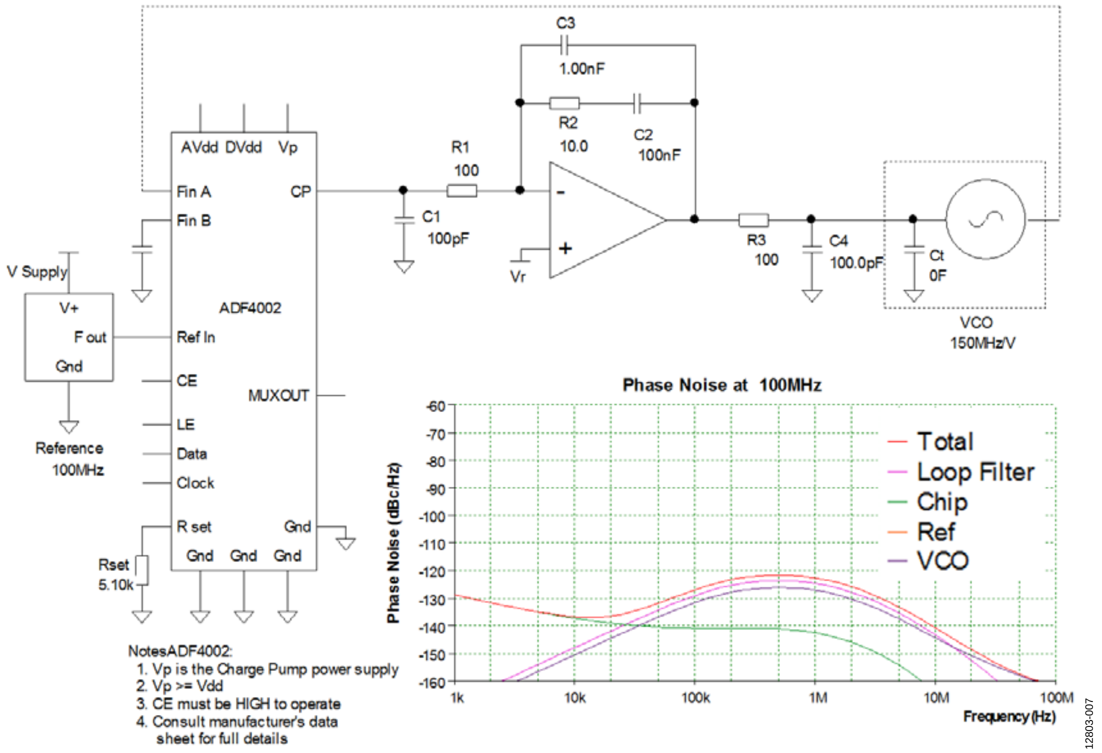

C3
1.00nF
R2
10.0
C2
100nF
R1
100
AVdd DVdd Vp
Fin A
Fin B
CP
C1
100pF
Vr
R3
100
C4
100.0pF
Ct
0F
VCO
150MHz/V
V Supply
V+
F out
Gnd
ADF4002
Ref In
CE
MUXOUT
LE
Data
Clock
R set
Gnd
Gnd Gnd Gnd
Reference
100MHz
Rset
5.10k
NotesADF4002:
1. Vp is the Charge Pump power supply
2. Vp >= Vdd
3. CE must be HIGH to operate
4. Consult manufacturer's data sheet for full details
Phase Noise at 100MHz
Phase Noise (dBc/Hz)
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160
1k
10k
100k
1M
10M
100M
Frequency (Hz)
Total
Loop Filter
Chip
Ref
VCO
12803-007

Figure 7. ADIsimPLL Schematic and Simulated Phase Noise for ADF4002 PLL

Translation Loop: Measured Phase Noise Results vs. Standalone PLL

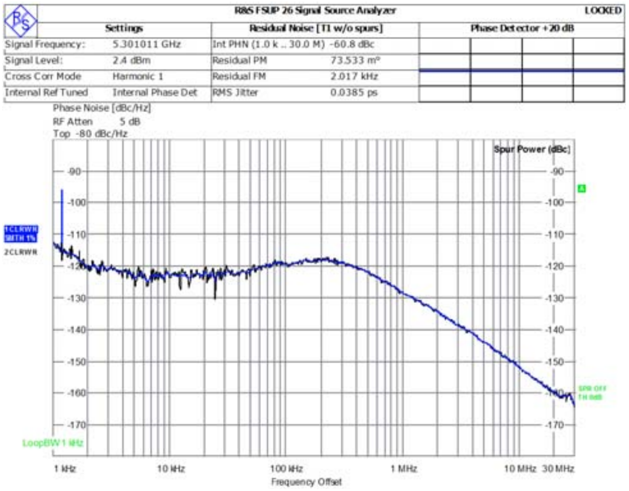
Using the configuration shown in Figure 1, the f_{OUT} rms jitter measures less than 50 fs, as shown in Table 2.

In Table 2, f_{REF} is the reference input to the EVAL-CN0369-SDPZ from the ADF4255-2 evaluation board. The f_{REF} provides the fine tuning for the translation loop. The local oscillator is the LO to the ADL5801-EVALZ mixer evaluation board and provides the coarse tuning for the translation loop. f_{OUT} is the VCO/2 RF output from the EVAL-CN0369-SDPZ.

Table 2. Phase Noise of Translation Loop PLL of Figure 1

f_{REF} (MHz)	Local Oscillator (MHz)	f_{OUT} Frequency (MHz)	f_{OUT} RMS Jitter (fs)
100.00	5300.00	5400.00	43
100.00	5200.00	5300.00	39
100.00	5100.00	5200.00	43
101.01	5100.00	5201.11	43

Figure 8 is a phase noise plot of the f_{OUT} from the translation loop. The reference (f_{REF}) input used in Figure 8 is 101.011 MHz to show the fine tuning performance of the translation loop. The f_{OUT} rms jitter in Figure 8 measures less than 39 fs integrated from 1 kHz to 30 MHz.



R&S FSUP 26 Signal Source Analyzer LOCKED

Settings		Residual Noise [T1 w/o spurs]		Phase Detector +20 dB
Signal Frequency:	5.301011 GHz	Int PHN (1.0 k .. 30.0 M)	-60.8 dBc	
Signal Level:	2.4 dBm	Residual PM	73.533 m°	
Cross Corr Mode	Harmonic 1	Residual FM	2.017 kHz	
Internal Ref Tuned	Internal Phase Det	RMS Jitter	0.0385 ps	

Figure 8. Phase Plot of the Translation Loop f_{OUT}

The f_{OUT} rms jitter measures between 200 fs and 250 fs using the ADF4355-2 as a stand-lone PLL to generate similar frequencies, as shown in Table 3.

For the Table 3 data, f_{REF} is the low noise REFIN source for the EV-ADF4355-2SD1Z evaluation board. f_{OUT} is the RFOUTA(+) of the EV-ADF4355-2SD1Z. RFOUTA(−) is connected to a 50 Ω terminator.

Table 3. Phase Noise of ADF4355-2-Based Standalone PLL

f_{REF} (MHz)	f_{OUT} Frequency (MHz)	f_{OUT} RMS Jitter (fs)
100.00	5400.00	202
100.00	5300.00	220
100.00	5200.00	243
100.00	5201.11	222

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0369-SDPZ circuit board, the EV-ADF4355-2SD1Z evaluation board, and the ADL5801-EVALZ evaluation board. The two EVAL-SDP-CS1Z system demonstration platform (SDP-S) boards are used with the EVAL-CN0369-SDPZ circuit board and the EV-ADF4355-2SD1Z evaluation board. The two boards have a 120-pin mating connectors, allowing quick setup and evaluation of the circuit performance. The SDP-S board connected to the EVAL-CN0369-SDPZ circuit board is used with the integer-N evaluation software to program the ADF4002 on-chip registers. The SDP-S board connected to the EV-ADF4355-2SD1Z board is used with the ADF4355-2 evaluation software to program the ADF4355-2 on-chip registers.

A complete set of documentation for the EVAl-CN0369-SDPZ board including schematics, layout files, and bill of materials can be found in the CN-0369 Design Support package at www.analog.com/CN0369-DesignSupport.

Getting Started

Refer to the EVAL-CN0369-SDPZ user guide (UG-806) for software installation and test setup.

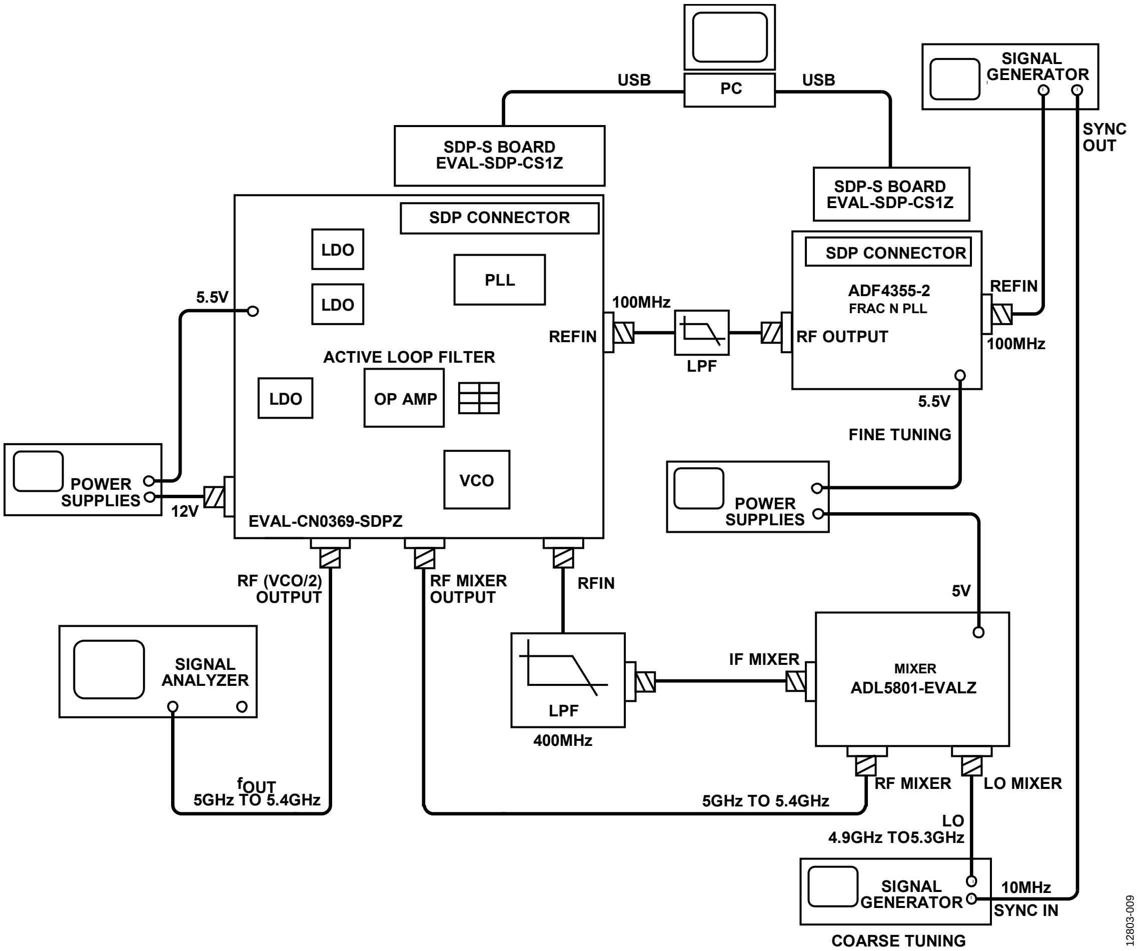

PC
USB
USB
SDP-S BOARD EVAL-SDP-CS1Z
SDP-S BOARD EVAL-SDP-CS1Z
SIGNAL GENERATOR
SYNC OUT
SDP CONNECTOR
LDO
PLL
LDO
5.5V
REFIN
100MHz
LPF
SDP CONNECTOR
ADF4355-2 FRAC N PLL
RF OUTPUT
REFIN
100MHz
ACTIVE LOOP FILTER
LDO
OP AMP
5.5V
FINE TUNING
POWER SUPPLIES
12V
VCO
EVAL-CN0369-SDPZ
POWER SUPPLIES
RF (VCO/2) OUTPUT
RF MIXER OUTPUT
RFIN
5V
SIGNAL ANALYZER
IF MIXER
MIXER ADL5801-EVALZ
LPF
400MHz
fOUT 5GHz TO 5.4GHz
5GHz TO 5.4GHz
RF MIXER
LO MIXER
LO 4.9GHz TO5.3GHz
SIGNAL GENERATOR
10MHz
SYNC IN
COARSE TUNING
12803-009

Figure 9. Block Diagram of the Test Setup

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP, Windows Vista (32-bit), or Windows 7 (32-bit)
- EVAL-CN0369-SDPZ circuit evaluation board
- EV-ADF4355-2SD1Z evaluation board
- Two EVAL-SDP-CS1Z SDP-S boards
- Integer-N v7 and the ADF4355 evaluation software
- Power supplies: 5 V, 5.5 V, and 12 V
- Two RF signal source (R&S SMA100 or equivalent)
- Spectrum analyzer (Agilent FSUP or equivalent)
- TTE 400 MHz low pass filter (or equivalent)
- Mini Circuits 100 MHz low pass filter (or equivalent)

Functional Block Diagram

See Figure 1 for the block diagram. A block diagram of the test setup is shown in Figure 9.

Setup and Test

After setting up the equipment, use standard RF test methods to measure the phase noise and phase jitter of the circuit.

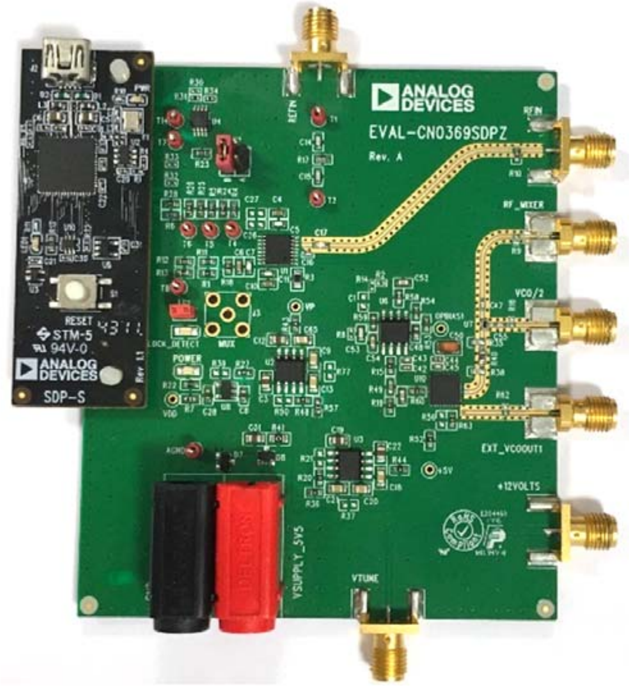


Figure 10. EVAL-CN0369-SDPZ PCB Photo

LEARN MORE

CN-0369 Design Support Package: www.analog.com/CN0369-DesignSupport

EVAL-CN0369-SDPZ User Guide (UG-806)

EV-ADF4355-2SD1Z User Guide (UG-804)

EVAL-SDP-CS1Z System Development Platform User Guide

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-086 Tutorial. *Fundamentals of Phase Locked Loops (PLLs).* Analog Devices.

MT-101 Tutorial. *Decoupling Techniques.* Analog Devices.

ADIsimPLL Design Tool

AN-30. *Ask the Application Engineer-30, PLL Synthesizers.* Analog Devices

Data Sheets and Evaluation Boards

EVAL-CN0369-SDPZ Evaluation Board

ADL5801-EVALZ Evaluation Board

EV-ADF4355-2SD1Z Evaluation Board

EVAL-SDP-CS1Z System Development Platform

ADF4002 Data Sheet

AD8065 Data Sheet

HMC512 Data Sheet

ADL5801 Data Sheet

ADF4355-2 Data Sheet

REVISION HISTORY

11/2016—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab reference designs are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab reference designs in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab reference designs. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab reference designs are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab reference designs at any time without notice but is under no obligation to do so.

©2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

CN12803-0-11/16(0)