

Circuit Note CN-0310

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	Devices Connected/Referenced	
	AD7176-2	24-Bit, 250 kSPS Sigma-Delta ADC with 20 μs Settling
	AD8475	Precision, Selectable Gain, Fully Differential Funnel Amplifier
	ADR445	Ultralow Noise, LDO XFET® 5 V Voltage Reference

24-Bit, 250 kSPS, Single-Supply Data Acquisition System

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7176-2 Circuit Evaluation Board (EVAL-AD7176-2SDZ) System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

It is important to provide fast and high resolution conversion information when sampling industrial level signals. Traditionally, the highest resolution analog-to-digital converters (ADCs) available at sampling rates up to 500 kSPS were 14 bit to 18 bit. The circuit shown in Figure 1 is a single-supply system optimized for sampling industrial level signals with a 24-bit, 250 kSPS sigmadelta (Σ - Δ) ADC. Each of the two differential or four pseudodifferential channels can be scanned at a rate up to 50 kSPS with 17.2 bits of noise-free code resolution.

This circuit solves the problem of acquiring and digitizing the standard industrial signal levels of ± 5 V, ± 10 V, and 0 V to 10 V with precision ADCs having low supply voltages by using an innovative differential amplifier with internal laser trimmed resistors to perform the attenuation and level shifting. Applications for the circuit include process controls (PLC/DCS modules), medical, and scientific multichannel instrumentation and chromatography.

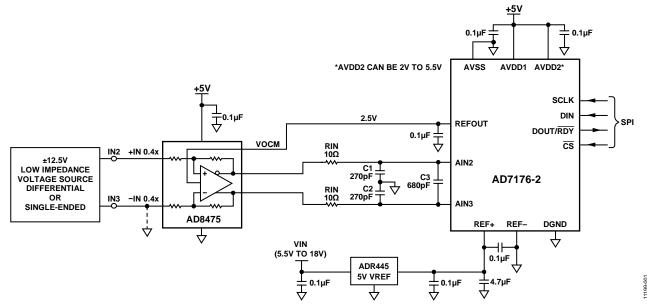


Figure 1. High Precision, 24-Bit ADC Driver for Industrial Signals (Simplified Schematic: All Connections and Decoupling Not Shown)

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CIRCUIT DESCRIPTION

The industrial level signals are applied to the AD8475 precision differential funnel amplifier that attenuates the input by either $0.8 \times$ or $0.4 \times$. Its integrated, trimmed, and matched precision resistors control the attenuation. The resistors allow single-ended or differential inputs up to ± 12.5 V when operating the AD8475 on a single 5 V supply with a gain of $0.4 \times$. The input has overvoltage protection up to ± 15 V.

The linearity of the combined AD8475 and AD7176-2 is maintained when the input signal (using a gain of $0.4\times$) is within a ±10 V single-ended or differential input range, as shown in the limits of the measured INL in Figure 4 where the measurement endpoints are -10 V and +10 V. In this scenario, the output of the AD8475 swings between 0.5 V and 4.5 V.

By applying the desired common-mode voltage to the VOCM pin, the common-mode output is set. In the Figure 1 circuit, the common-mode voltage is set by applying the 2.5 V REFOUT voltage from the AD7176-2 ADC to the VOCM pin of the AD8475.

The AD8475 provides the attenuation and level shifting to drive the sampling capacitor input of the AD7176-2 and consumes only 3.2 mA.

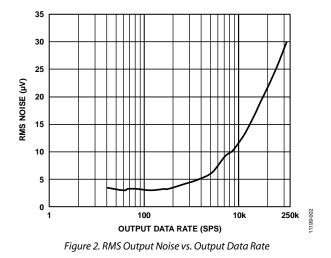
The output of the AD8475 amplifier is connected to an RC filter network that provides differential and common-mode noise filtering and that supplies the dynamic charge required by the AD7176-2 input sampling capacitors. The network also isolates the amplifier output from any kickback from the dynamic switched capacitor input. The common-mode bandwidth (RIN, C1) is 59 MHz. The differential-mode bandwidth ($2 \times RIN$, 0.5C1 + C3) is 9.8 MHz

The AD8475 can also be set up to accept single-ended signals. Ground the $-IN 0.4 \times$ input and apply the single-ended signal to the $+IN 0.4 \times$ input.

The AD7176-2 24-bit, Σ - Δ ADC samples the output of the AD8475 and converts it to a digital result. The rate of conversion and the digital filter characteristic are adjustable for output data rates from 5 SPS to 250 kSPS.

The AD7176-2 is configurable for two fully differential inputs or four pseudo-differential inputs. The ADC allows up to a 50 kSPS channel scan rate. The AD7176-2 noise-free bit performance is 17.2 bits at 250 kSPS, 20.8 bits at 1 kSPS, and 21.7 bits at 50 SPS.

Figure 2 shows the effective rms noise of the total system with the inputs grounded. At a data rate of 250 kSPS, the effective rms noise is approximately 30 μ V rms. When keeping in mind that the linearity of the circuit is best with a ±10 V input at full scale, the full-scale input for the calculation was set to 20 V p-p.



The effective resolution in bits, referred to a full-scale input range of 20 V, can be calculated as

Effective Resolution = $log_2(FSR/RMS Noise)$

Effective Resolution = $\log_2(20 \text{ V}/30 \mu\text{V}) = 19.3$ Bits

Figure 3 shows the effective resolution in bits rms as a function of output data rate, measured with a shorted input.

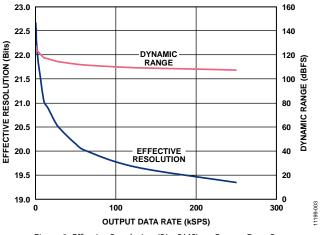


Figure 3. Effective Resolution (Bits RMS) vs. Output Data Rate

Effective resolution can be converted to a noise-free code resolution by first converting the rms noise to approximate peak-to-peak noise by multiplying the rms noise by the factor of 6.6. This is approximately 2.7 bits that then must be subtracted from the effective resolution to get the noise-free code resolution. For the example calculated, 19.3 bits of effective resolution is equal to 16.6 bits of noise-free code resolution. This compares to the AD7176-2 specification of 17.2 noise free bits at a 250 kSPS output data rate with an unbuffered shorted input. Approximately 0.3 bits of this difference results from the fact that only ± 10 V was used as the full-scale range vs. the ± 12.5 V maximum.

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Figure 4 shows the integral nonlinearity of the system expressed in ppm of the full-scale range (FSR) using the endpoint method.

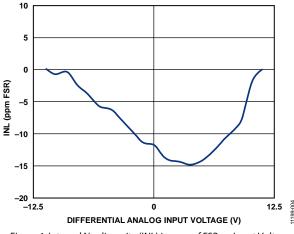


Figure 4. Integral Nonlinearity (INL) in ppm of FSR vs. Input Voltage

Although the circuit is designed primarily to take dc inputs, low frequency ac inputs can also be converted. The distortion performance varies with the analog input amplitude. Figure 5 and Figure 6 show the performance with a -1 dBFS and -6 dBFS, 1 kHz sine wave, respectively. The sine wave input is applied directly to the AD8475 from the Audio Precision 2700 series audio source.

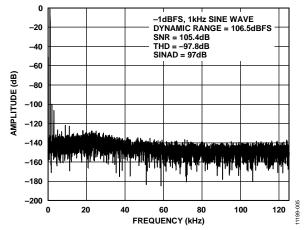


Figure 5. AD8475 to AD7176-2 FFT Performance, 1 kHz, -1 dBFS Input Tone, (16384 Point FFT)

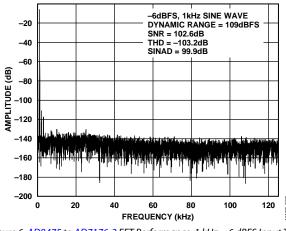


Figure 6. AD8475 to AD7176-2 FFT Performance, 1 kHz, –6 dBFS Input Tone, (16384 Point FFT)

Excellent printed circuit board (PCB) layout, grounding, and decoupling techniques are mandatory for achieving optimum performance in high resolution systems. For details, see Tutorial MT-031, Tutorial MT-101, the AD8475 data sheet, and the AD7176-2 data sheet. Complete schematics and layout of the printed circuit board can be found in the CN-0310 Design Support Package.

COMMON VARIATIONS

In the Figure 1 circuit, the AD8475 0.4× gain option was chosen. If the $0.8\times$ gain option was chosen, the full-scale range would reduce from ±10 V to ±5 V yielding twice the sensitivity.

A second channel using an additional AD8475 can be connected to the AN0/AN1 pins of the AD7176-2.

The ADR445 reference can be replaced with the ADR4550 reference, which has a 300 mV dropout voltage.

CIRCUIT EVALUATION AND TEST

Equipment Required

The following equipment is required:

- The EVAL-AD7176-2SDZ evaluation board and software
- The System Demonstration Platform (EVAL-SDP-CB1Z)
- A precision dc voltage source
- The Audio Precision 2700 Series (ac inputs)
- A PC (Windows 32-bit or 64-bit)
- A 7 V to 9 V dc supply or wall wart

Software Installation

The AD7176-2 evaluation kit includes self-installing software on a CD. The software is compatible with Windows[®] XP (SP2), Windows Vista, and Windows 7 (32 bit or 64 bit). If the setup file does not automatically run, run the **setup.exe** file from the CD.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

After installation from the CD is complete, connect the EVAL-SDP-CB1Z (via either Connector A or Connector B) to the EVAL-AD7176-2SDZ and then connect the EVAL-SDP-CB1Z to the USB port of the PC using the supplied cable.

When the evaluation system is detected, proceed through any dialog boxes that appear. This completes the installation.

Setup and Test

Refer to the UG-478 user guide for complete details of using the software and running the tests.

A functional block diagram of the test setup is shown in Figure 7.

The following minor hardware changes are required to test the circuit in Figure 1:

- Signals are input to the AD8475 from the A2 and A3 inputs on the J8 terminal block.
- Change the SL9 and SL10 solder links to Position C routing the signals from A2 and A3 of J8 to the AD8475 inputs.
- Populate R64 and R74 with 10 Ω, 0603 resistors to connect the AD8475 outputs to the AIN2 and AIN3 pins of the AD7176-2.
- Remove the R110 and R120 resistors on the underside of the board (as shown in the UG-478 user guide).

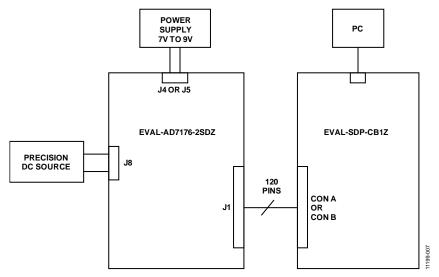


Figure 7. Test Setup Functional Diagram

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LEARN MORE

CN-0310 Design Support Package: http://www.analog.com/CN0310-DesignSupport

UG-478, Evaluation Board for the AD7176-2—24-Bit, 250 kSPS Sigma-Delta ADC with 20 µs Settling.

- Ardizzoni, John. A Practical Guide to High-Speed Printed-Circuit-Board Layout, Analog Dialogue 39-09, September 2005.
- MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise*? Analog Devices.
- MT-022 Tutorial, ADC Architectures III: Sigma-Delta ADC Basics, Analog Devices.
- MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.
- MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.
- MT-074 Tutorial, *Differential Drivers for Precision ADCs*, Analog Devices.
- MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*, Analog Devices.

MT-076 Tutorial, Differential Driver Analysis, Analog Devices. MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD7176-2 Data Sheet

EVAL-AD7176-2SDZ, AD7176-2 Evaluation Board

AD8475 Data Sheet and Evaluation Board

ADR445 Data Sheet

REVISION HISTORY

11/12—Initial Version

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