ANALOG DEVICES

Circuit Note
CN-0279

Circuits from the Lab™ Reference Circuits

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Devices Connected/Referenced	
AD9642	14-Bit, 250 MSPS Analog-to-Digital Converter
ADL5565	6 GHz Ultrahigh Dynamic Range Differential Amplifier

High IF Sampling Receiver Front End with Band-Pass Filter

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit, shown in Figure 1, is a narrow, band-pass receiver front end based on the ADL5565 ultralow noise differential amplifier driver and the AD9642 14-bit, 250 MSPS analog-to-digital converter (ADC).

The third-order, Butterworth antialiasing filter is optimized based on the performance and interface requirements of the amplifier and ADC. The total insertion loss due to the filter network and other components is only 5.8 dB.

The overall circuit has a bandwidth of 18 MHz with a pass-band flatness of 3 dB. The signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) measured with a 127 MHz analog input are 71.7 dBFS and 92 dBc, respectively. The sampling frequency is 205 MSPS, thereby positioning the IF input signal in the second Nyquist zone between 102.5 MHz and 205 MHz.

CIRCUIT DESCRIPTION

The circuit accepts a single-ended input and converts it to differential input using a wide bandwidth (3 GHz) Mini-Circuits TC2-1T 1:2 transformer. The 6 GHz ADL5565 differential amplifier has a differential input impedance of 200 Ω when operating at a gain of 6 dB, and 100 Ω when operating at a gain of 12 dB. A gain option of 15.5 dB is also available.

The ADL5565 is an ideal driver for the AD9642, and the fully differential architecture through the band-pass filter and into the ADC provides good high frequency common-mode rejection, as well as minimizes second-order distortion products. The ADL5565 provides a gain of 6 dB or 12 dB, depending on the input connection. In the circuit, a gain of 12 dB was used to compensate for the insertion loss of the filter network and transformer (approximately 5.8 dB), providing an overall signal gain of 5.5 dB.

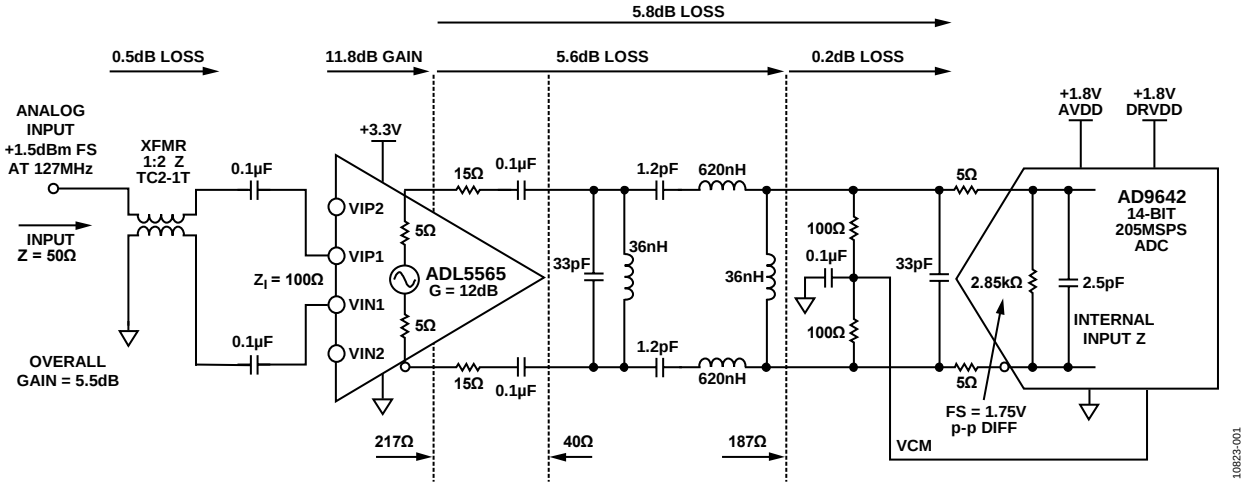

Figure 1. 14-Bit, 250 MSPS Wideband Receiver Front End (Simplified Schematic: All Connections and Decoupling Not Shown)
Gains, Losses, and Signal Levels Measured Values for an Input Frequency of 127 MHz

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An input signal of 1.5 dBm produces a full-scale 1.75 V p-p differential signal at the ADC input.

The antialiasing filter is a third-order, Butterworth filter designed with a standard filter design program. A Butterworth filter was chosen because of its pass-band flatness. A third-order filter yields an ac noise bandwidth ratio of 1.05 and can be designed with the aid of several free filter programs such as Nuhertz Technologies Filter Free, or the quite universal circuit simulator (Qucs) free simulation.

To achieve best performance, load the ADL5565 with a net differential load of 200 Ω. The 15 Ω series resistors isolate the filter capacitance from the amplifier output, and the 100 Ω resistors in parallel with the downstream impedance yield a net load impedance of 217 Ω when added to the 30 Ω series resistance.

The 5 Ω resistors in series with the ADC inputs isolate internal switching transients from the filter and the amplifier.

The 2.85 kΩ input impedance was determined using the downloadable spreadsheet on the AD9642 webpage. Simply use the parallel track mode values at the center of the IF frequency of interest. The spreadsheet shows both the real and imaginary values.

The third-order, Butterworth filter was designed with a source impedance (differential) of 200 Ω, a load impedance (differential) of 200 Ω, a center frequency of 127 MHz, and a 3 dB bandwidth of 20 MHz. The calculated values from a standard filter design program are shown in Figure 1. Because of the high values of series inductance required, the 1.59 µH inductors were decreased to 620 nH, and the 0.987 pF capacitors increased proportionally to 2.53 pF, thereby maintaining the same resonant frequency of 127 MHz, with more realistic component values.

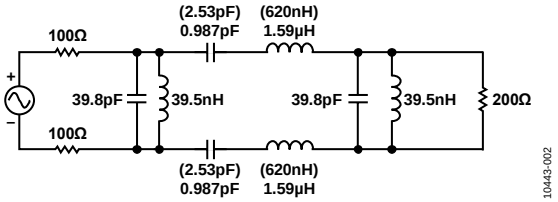

Figure 2. Starting Design for Third-Order, Differential Butterworth Filter with Z_S = 200 Ω, Z_L = 200 Ω, F_C = 127 MHz, and BW = 20 MHz

The internal 2.5 pF capacitance of the ADC was subtracted from the value of the second shunt capacitor to yield a value of 37.3 pF. In the circuit, this capacitor was located near the ADC to reduce/absorb the charge kickback.

The values chosen for the final filter passive components (after adjusting for actual circuit parasitics) are shown in Figure 1.

The measured performance of the system is summarized in Table 1, where the 3 dB bandwidth, 18 MHz centered at 127 MHz. The total insertion loss of the network is approximately 5.8 dB. The frequency response is shown in Figure 3, and the SNR and SFDR performance are shown in Figure 4.

Table 1. Measured Performance of the Circuit

Performance Specifications at −1 dBFS (FS = 1.75 V p-p), Sample Rate = 205 MSPS	Final Results
Center Frequency	127 MHz
Pass-Band Flatness (118 MHz to 136 MHz)	3 dB
SNRFS at 127 MHz	71.7 dBFS
SFDR at 127 MHz	92 dBc
H2/H3 at 127 MHz	93 dBc/92 dBc
Overall Gain at 127 MHz	5.5 dB
Input Drive at 127 MHz	0.5 dBm (−1 dBFS)

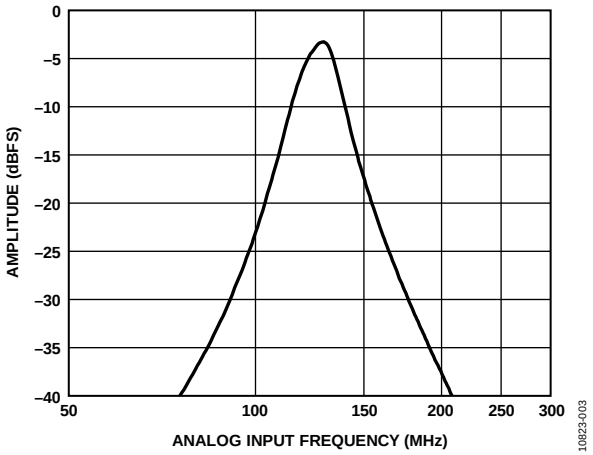

Figure 3. Pass-Band Flatness Performance vs. Frequency

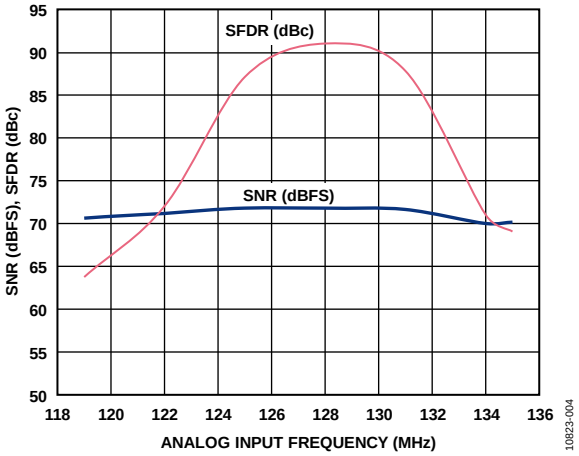

Figure 4. SNR/SFDR Performance vs. Frequency, Sample Rate = 205 MSPS

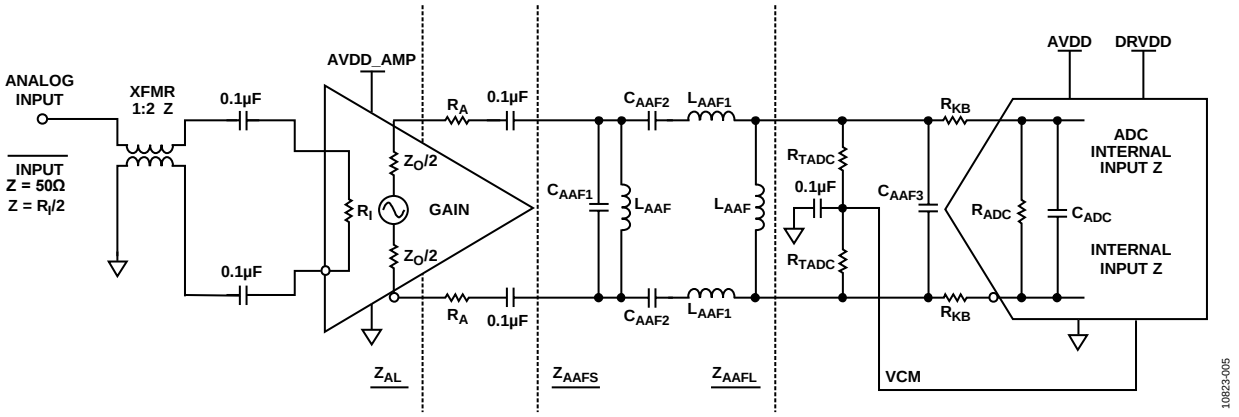

Figure 5. Generalized Differential Amplifier/ADC Interface with Band-Pass Filter

Filter and Interface Design Procedure

In this section, a general approach to the design of the amplifier/ADC interface with a band-pass filter is presented. To achieve optimum performance (bandwidth, SNR, and SFDR), there are certain design constraints placed on the general circuit by the amplifier and the ADC.

1. The amplifier must see the correct dc load recommended by the data sheet for optimum performance.
2. The correct amount of series resistance must be used between the amplifier and the load presented by the filter. This is to prevent undesired peaking in the pass band.
3. The input to the ADC must be reduced by external parallel resistors, and the correct series resistance must be used to isolate the ADC from the filter. This series resistor also reduces peaking.

The generalized circuit shown in Figure 5 applies to most high speed differential amplifier/ADC interfaces and was used as a basis for the band-pass filter. This design approach tends to minimize the insertion loss of the filter by taking advantage of the relatively high input impedance of most high speed ADCs and the relatively low impedance of the driving source (amplifier).

The basic design process is as follows:

1. Set the external ADC termination resistors, R_{TADC}, so that the parallel combination of R_{TADC} and R_{ADC} is between 200 Ω and 400 Ω.
2. Select R_{KB} based on experience and/or the ADC data sheet recommendations, typically between 5 Ω and 36 Ω.
3. Calculate the filter load impedance using

$$Z_{AAFL} = 2R_{TADC} \,||\, (R_{ADC} + 2R_{KB})$$

4. Select the amplifier external series resistor, R_A. Make R_A less than 10 Ω if the amplifier differential output impedance is 100 Ω to 200 Ω. Make R_A between 5 Ω and 36 Ω if the output impedance of the amplifier is 12 Ω or less.
5. Select Z_{AAFL} so that the total load seen by the amplifier, Z_{AL}, is optimum for the particular differential amplifier chosen using the following equation:

$$Z_{AL} = 2R_A + Z_{AAFL}$$

6. Calculate the filter source resistance by

$$Z_{AAFS} = Z_O + 2R_A$$

7. Using a filter design program or tables design the filter using the source and load impedances, Z_{AAFS} and Z_{AAFL}, type of filter, bandwidth, and order. Use a bandwidth that is about 10% higher than the desired bandwidth of the application pass band to ensure flatness in the frequency span.

After running these preliminary calculations, the circuit must be given a quick review for the following items.

1. The value of C_{AAF3} must be at least 10 pF so that it is several times larger than C_{ADC}. This minimizes the sensitivity of the filter to variations in C_{ADC}.
2. The ratio of Z_{AAFL} to Z_{AAFS} must not be more than about 7 so that the filter is within the limits of most filter tables and design programs.
3. The value of C_{AAF1} must be at least 5 pF to minimize sensitivity to parasitic capacitance and component variations.
4. The inductor, L_{AAF}, must be a reasonable value of at least several nH.
5. The value of C_{AFF2} and L_{AAF1} must be reasonable values. Sometimes circuit simulators can make these values too low or too high. To make these values more reasonable, simply ratio these values with better standard value components that maintain the same resonant frequency.

In some cases, the filter design program can provide more than one unique solution, especially with higher order filters. The solution that uses the most reasonable set of component values should always be chosen. Also, choose a configuration that ends in a shunt capacitor so that it can be combined with the ADC input capacitance.

Circuit Optimization Techniques and Trade-Offs

The parameters in this interface circuit are very interactive; therefore, it is almost impossible to optimize the circuit for all key specifications (bandwidth, bandwidth flatness, SNR, SFDR, and gain). However, the peaking, which often occurs in the bandwidth response, can be minimized by varying R_A and R_{KB}.

The value of R_A also affects SNR performance. Larger values, while reducing the bandwidth peaking, tend to slightly increase the SNR because of the higher signal level required to drive the ADC full scale.

Select the R_{KB} series resistor on the ADC inputs to minimize distortion caused by any residual charge injection from the internal sampling capacitor within the ADC. Increasing this resistor also tends to reduce bandwidth peaking.

However, increasing R_{KB} increases signal attenuation, and the amplifier must drive a larger signal to fill the ADC input range.

For optimizing center frequency, pass-band characteristics, the series capacitor, C_{AAF2}, can be varied by a small amount.

Normally, the ADC input termination resistor, R_{TADC}, is selected to make the net ADC input impedance between 200 Ω and 400 Ω, which is typical of most amplifier characteristic load values. Using too high or too low a value can have an adverse effect on the linearity of the amplifier.

Balancing these trade-offs can be somewhat difficult. In this design, each parameter was given equal weight; therefore, the values chosen are representative of the interface performance for all the design characteristics. In some designs, different values can be chosen to optimize SFDR, SNR, or input drive level, depending on system requirements.

The SFDR performance in this design is determined by two factors: the amplifier and ADC interface component values, as shown in Figure 1.

Note that the signal in this design is ac-coupled with the 0.1 µF capacitors to block the common-mode voltages between the amplifier, its termination resistors, and the ADC inputs. Refer to the AD9642 data sheet for further details regarding common-mode voltages.

Passive Component and PC Board Parasitic Considerations

The performance of this or any high speed circuit is highly dependent on proper printed circuit board (PCB) layout. This includes, but is not limited to, power supply bypassing, controlled impedance lines (where required), component placement, signal routing, and power and ground planes. See Tutorial MT-031 and Tutorial MT-101 for more detailed information regarding PCB layout for high speed ADCs and amplifiers. In addition, see the CN-0227 and the CN-0238.

Use low parasitic surface-mount capacitors, inductors, and resistors for the passive components in the filter. The inductors chosen are from the Coilcraft 0603CS series. The surface-mount capacitors used in the filter are 5%, C0G, 0402 type for stability and accuracy.

See the CN-0279 Design Support Package for the complete documentation on the system.

COMMON VARIATIONS

The AD9643 is a dual version of the AD9642.

For lower power and bandwidth, the ADA4950-1 and/or ADL5561/ADL5562 can also be used. These devices are pin compatible with the other singles previously listed.

CIRCUIT EVALUATION AND TEST

This circuit uses a modified AD9642-250EBZ circuit board and the HSC-ADC-EVALCZ FPGA-based data capture board. The two boards have mating high speed connectors, allowing for the quick setup and evaluation of the performance of the circuit. The modified AD9642-250EBZ board contains the circuit evaluated as described in this note, and the HSC-ADC-EVALCZ data capture board is used in conjunction with VisualAnalog® evaluation software, as well as the SPI Controller software to properly control the ADC and capture the data. See User Guide UG-386 for the schematics, BOM, and layout for the AD9642-250EBZ board. The **readme.txt** file in the CN-0279 Design Support Package describes the modifications made to the standard AD9642-250EBZ board. Application Note AN-835 contains complete details on how to set up the hardware and software to run the tests described in this circuit note.

LEARN MORE

CN-0279 Design Support Package:
http://www.analog.com/CN0279-DesignSupport

UG-386 User Guide, Evaluating the AD9642/AD9634/AD6672 Analog-to-Digital Converters

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Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, *Analog Dialogue* 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Quite Universal Circuit Simulator

Nuhertz Technologies, Filter Free Filter Design Program

Reeder, Rob, *Achieve CM Convergence between Amps and ADCs*, Electronic Design, July 2010.

Reeder, Rob, *Mine These High-Speed ADC Layout Nuggets For Design Gold*, Electronic Design, September 15, 2011.

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 1: Power and Ground Planes*, November 2010.

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 2: Using Power and Ground Planes to Your Advantage*, February 2011.

Rarely Asked Questions: *Considerations of High-Speed Converter PCB Design, Part 3: The E-Pad Low Down*, June 2011.

Data Sheets and Evaluation Boards

AD9642 Data Sheet

ADL5565 Data Sheet

Circuit Evaluation Board (AD9642-250EBZ)

Standard Data Capture Platform (HSC-ADC-EVALCZ)

REVISION HISTORY

7/12—Revision 0: Initial Version