High Dynamic Range RF Transmitter Signal Chain Using Single External Frequency Reference for DAC Sample Clock and IQ Modulator LO Generation

CIRCUIT FUNCTION AND BENEFITS

The combination of the ADRF6702 IQ modulator and the AD9122 16-bit dual 1.2 GSPS TxDAC has the dynamic range necessary for a modern high level QAM or OFDM based wireless transmitter as shown in Figure 1. The dynamic range of this circuit is good enough to enable both ZIF (zero IF/ baseband) and CIF (complex IF up to 200 MHz to 300 MHz). The AD9122 has the option of up to 8× interpolation, as well as a 32-bit NCO for very fine IF frequency selectivity.

Overall performance of a transmitter is highly dependent on the dynamic range of the components directly in the signal chain. In a mixed-signal transmitter using a DAC and IQ modulator, the noise floor and distortion characteristics of these components define the overall dynamic range of the signal chain. However, the noise floor of the DAC can also be degraded by sample clock jitter, and the IQ modulator performance is dependent on the noise and spur characteristics of its local oscillator (LO). Using high performance components for sample clock and LO generation is, therefore, key to a high performance transmitter.

In addition, generating these signals physically close to the DAC and modulator on the PCB and using a single external reference can make the design much simpler. Generating the sample clock and LO (LO is very often a multi-GHz signal) separately and at some distance from the DAC and IQ modulator requires great care in the PCB layout. Subtle layout errors can cause coupling to and from these critical signals and degrade overall signal chain performance.

The signal chain performance is also heavily dependent on the DAC/ IQ modulator interface filter. For optimal performance, this passive filter should be designed after careful analysis of the required system specifications.

The ADRF6702 includes an on-board fractional PLL for LO generation so that a low frequency reference (typically less than 100 MHz) is all that is necessary to synthesize the IQ modulator LO. Using the PLL in the AD9516 clock generator allows a single reference to generate both the DAC sample clock and the PLL reference for the ADRF6702.

The circuit in Figure 1 was built using the AD9516-0, but other members of the AD9516 family could be used depending on the desired internal VCO frequency.

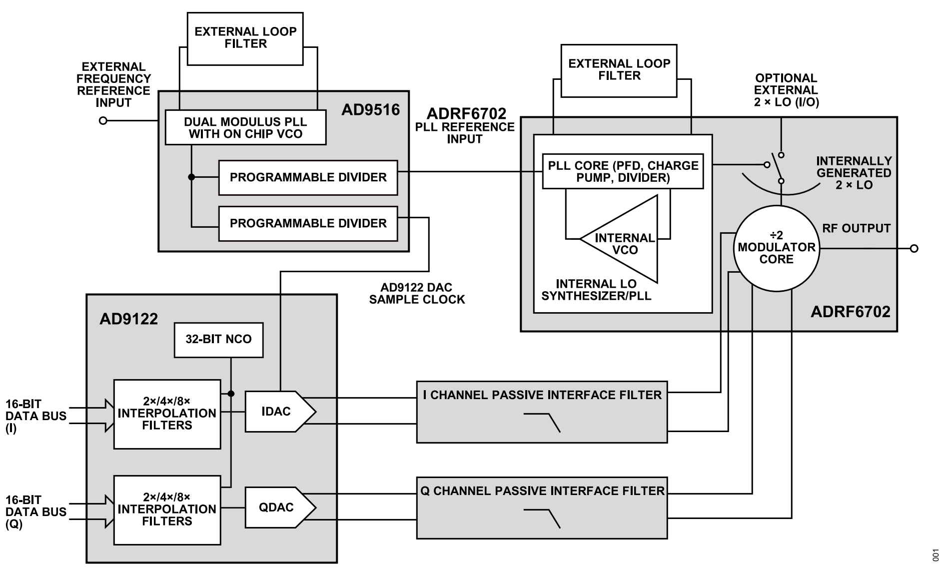

Figure 1. AD9122, ADRF6702, and AD9516 Used in a High Dynamic Range Transmitter

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10/11—Revision 0: Initial Version

CIRCUIT DESCRIPTION

ADRF6702 IQ MODULATOR WITH INTERNAL LO SYNTHESIZER, SYNTHESIZER IQ MODULATOR INTERFACE

The ADRF6702 IQ modulator is a unique device in several respects. In addition to its exceptional dynamic range, it also includes a fractional-N PLL, which allows programming of discrete LO frequency steps of less than 25 kHz while at the same time keeping the overall frequency multiplication small enough to avoid a large increase in phase noise from the reference to the synthesizer output.

Another aspect of the ADRF6702 is the divide-by-2 architecture of the IQ modulator. Traditional IQ modulators accept an LO input frequency at 1× the desired LO. Internally, a distributed RC network creates the desired in-phase and quadrature LO signals from the single LO frequency input. Because this is a passive RC network, the bandwidth over which quadrature modulation accuracy is achieved is limited. Also, for good quadrature accuracy, the external LO should be spectrally pure. Harmonics on the LO with this traditional IQ modulator architecture can degrade the overall modulation accuracy. For this reason, when using a PLL synthesizer to generate an LO signal for an IQ modulator, a sharp band-pass or low-pass filter is often required at the IQ modulator LO input.

In the divide-by-2 LO architecture of the ADRF6702, a simple digital divider is used internally to create nearly perfect quadrature over a wide band. The PLL synthesizer generates the 2× LO internally, so that it does not have to be distributed around the PCB, and no filter is required between the synthesizer and IQ modulator LO because the 2× LO architecture is only sensitive to the edges of the LO signal, not the frequency content.

SAMPLED SIGNAL TO RF, OVERALL SPUR FLOOR

A baseband signal goes through a number of steps on the way to the RF transmit frequency. The signal begins in the discrete (sampled) domain and is synthesized by the DAC into the analog domain. The results of this step are images and distortion products generated by the DAC. As shown in Figure 2, an ideal DAC with no distortion will generate images of a baseband signal that must be filtered before being modulated. The use of interpolation filters such as those in the AD9122 can suppress most of the image energy, but an analog interface filter between DAC and modulator will still be necessary. There is a trade-off, however, between the order of the DAC interpolation and the order of the analog filter. Higher DAC interpolation rates mean lower required analog filter order and vice versa. Figure 3 shows what the DAC output spectrum looks like when using 4× interpolation, as an example.

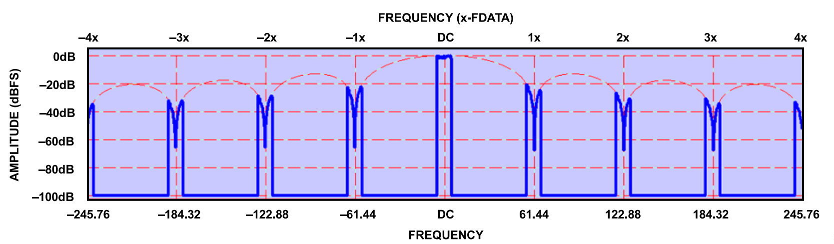

Figure 2. DAC Output Spectrum, Solid Blue Line Represents Baseband Signal and Images, Dotted Red Line Represents DAC Sinc Function

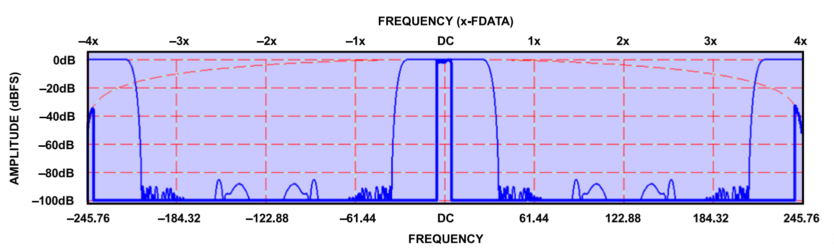

Figure 3. DAC Output Spectrum Using 4× Interpolation, the Thin Blue Line Represents the DAC Interpolation Transfer Function

A MULTITUDE OF SPURIOUS COMPONENTS AT RF

The signal chain can add significant spurious components to the spectrum, due both to modulation products, distortion products, and integer multiples of the LO frequency. It takes into account all of the possibilities for spurious content, which can consist of

$(j \times LO\_freq) + (k \times DAC\_sample\_rate) +$

$(l \times DAC\_NCO\_freq) + (m \times DAC\_input\_IF)$

where:
j, k, l, and m are integers over the range of negative infinity to positive infinity.

DAC/MODULATOR PASSIVE INTERFACE FILTER

The key to reducing the overall spurious spectrum is the analog interface filter between the DAC and the IQ modulator. The design of the interface filter between the DAC and IQ modulator must take into account multiple aspects of performance:

1. Filter topology, order, and 3 dB cutoff frequency
2. At dc, the DAC sees a load impedance equal to the DAC termination resistors (typically a 100 Ω differential impedance) in parallel with the input impedance of the IQ modulator. The IQ modulator impedance is often >1kΩ, so a shunt resistor is often used across the IQ modulator inputs to create a similar load impedance to the source. Unequal filter source and load impedances, as well as parasitics in the signal traces, may add unwanted ripple in the filter pass band.
3. PCB layout. As shown in Figure 4, the I and Q baseband inputs on the ADRF6702 IQ modulator are located on opposite edges of the device. Note the filter layout area within the dotted circles. To route the DAC output signals to these pins, the traces must travel up and then back down to get to the baseband pins on the ADRF6702. These differential signal traces should be of equal length, and any changes in direction of the trace should be done by using 45° bends. If these recommendations are not implemented, in-band ripple, phase, or amplitude response may be degraded in the filter response. Note that with this filter topology, the capacitors can be used differentially (across the signal path) or they can be used in a common-mode connection by placing the filter caps from the signal path pads to ground pads. There are conditions where common-mode capacitors improve performance vs. differential-mode capacitors.

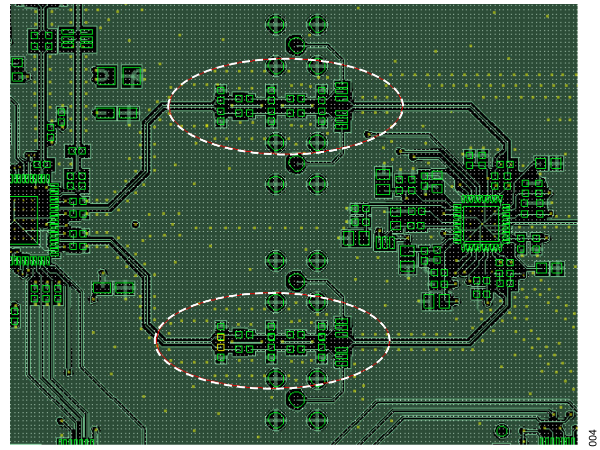

Figure 4. PCB Layout for Transmitter, DAC/Mod Interface Filter Section

4. To achieve optimal performance from the filter, these traces should be 100 Ω differential, or 50 Ω per line. Note that with typical FR4 material, a 50 Ω line results from a T/W ratio of 2:1. If higher impedance lines are desired it should be understood that the impedance of the line is a nonlinear function of T/W (T = board layer thickness, W = width of trace). A thinner line results in a higher impedance line. With typical FR4 layer thicknesses, a 100 Ω line can get very thin, often close to minimum design constraints. One solution to this is to void the ground layer underneath the trace and put another ground layer on the third layer of the PCB. This effectively doubles T and allows for a wider trace.

DAC_MOD INTERFACE FILTER TOPOLOGY

Figure 5 shows a typical topology which gives a 5th order maximally flat Butterworth response for a differential input and output impedance of 100 Ω.. The actual response is given in Figure 6. This filter uses 4.6 pF capacitors at the source and load.

This magnitude of capacitor value (<20 pF) is typical of filters with high cutoff frequencies. Parasitics may have a significant effect on response when using these small capacitor values.

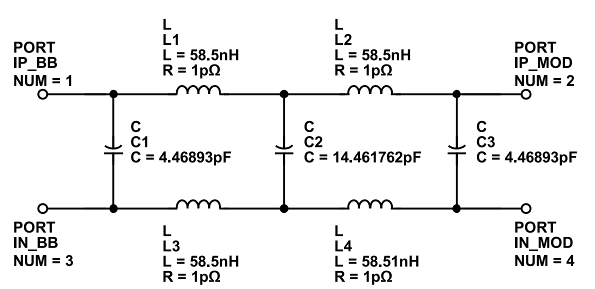

Figure 5. DAC/Mod Interface Filter Topology, 5th Order Butterworth, 3 dB BW = 220 MHz, 100 Ω Differential Input and Output Impedance

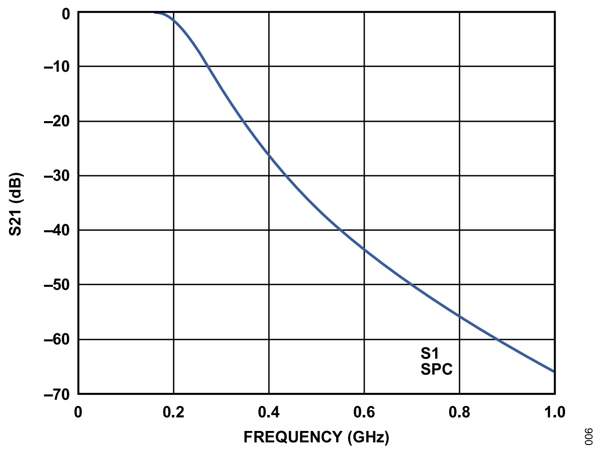

Figure 6. Frequency Response of Filter Topology Given in Figure 5

DAC AND DISTORTION RELATED SPURIOUS COMPONENTS

The use of DAC interpolation filters by themselves can reduce the spurious content at the modulator input and, therefore, the spurious content at RF. However, there may still be significant spurious content. Figure 7 shows the RF output spectrum of the IQ modulator under the following conditions:

- *FLO* = 1940 MHz
- *DAC input data rate* = 300 MSPS
- *DAC interpolation* = 4×
- *DAC NCO frequency* = 150 MHz
- *DAC input IF frequency* = 8 MHz

Note that the strongest spurious component (aside from the fundamental at 2098 MHz) is the 2× component of the DAC clock at 2400 MHz. This is likely a result of common and differential mode components of the DAC output containing some spectrum from the DAC clock. The common-mode rejection of the IQ modulator input rejects much of this signal, but it is still contains significant energy. The next two highest spurs, at 2062 MHz and at 2242 MHz, also seem to be related to DAC clock spurs. The spur at 2242 MHz is easily recognized as 2 × (DAC clock – DAC fundamental) = 2400 − 158. The spur at 2062 MHz is not so obvious, but looks like (3 × LO) − (3 × DAC clock) − 158 = 5820 − 3600 − 158. If the analysis is correct, then we should be able to see significant spur reduction if we can suppress the common-mode component of the DAC clock at the IQ modulator inputs.

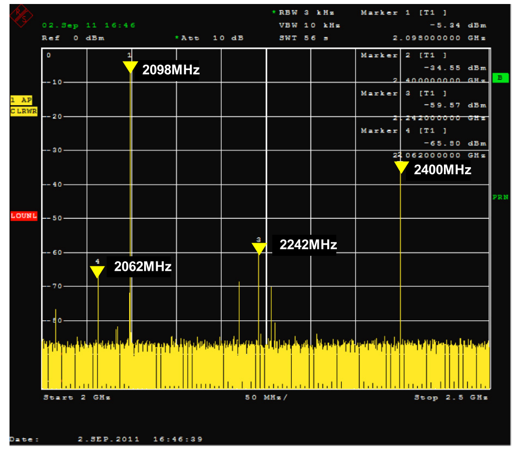

Figure 7. IQ Modulator RF Output with DAC/IQ Mod Filter Absent, LO = 1940 MHz, DAC Input IF = 8 MHz, DAC NCO = 150 MHz, RF = 2098 MHz

Applying the differential Butterworth filter gives significant spur level reduction, as shown in Figure 8. The strongest spurs are still at 2062 MHz, 2242 MHz, and the 2× DAC clock spur at 2400 MHz. All three spurious components have been reduced significantly.

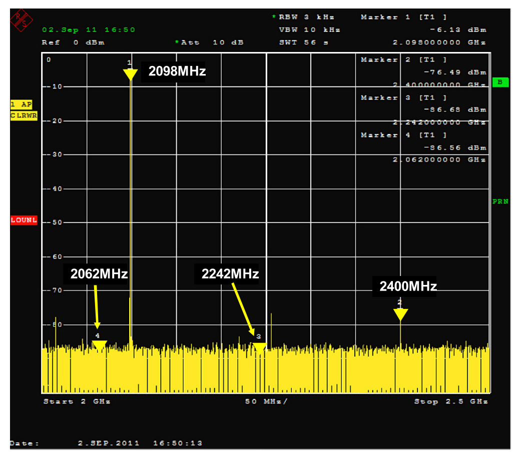

Figure 8. RF Spectrum Using 5th Order Butterworth Filter, Differential Capacitors

The common-mode rejection of the DAC/IQ modulator interface can often be improved by changing the topology of the interface filter. In Figure 9, the input and output 4.7 pF caps are replaced by common-mode capacitors (9.0 pF) from both sides of the filter input and both sides of the filter output to ground. This does not change the overall differential filter mode response but does have an effect on this board on the overall spurious content at RF. The harmonics mentioned earlier at 2062 MHz and 2242 MHz are down a few dB more, and there has been about a 15 dB reduction in the 2× DAC clock component, nearly to the noise floor.

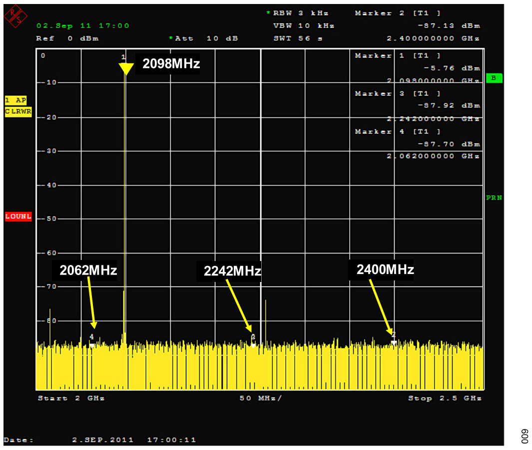

Figure 9. RF Spectrum Using 5th Order Butterworth Filter, Combination of Differential and Common- Mode Capacitors Used in the DAC_Mod Filter

The topology and results shown here may vary from layout to layout, so it is always to the advantage of the designer to experiment with the layout of the filter, specifically which mix of differential and common-mode capacitors results in the lowest overall spur floor.

SYNTHESIZER PATH AND PLL PHASE NOISE

As shown in Figure 1, this circuit uses a single external reference to generate the AD9122 DAC sample clock and the reference clock for the PLL in the ADRF6702. The AD9516 is fundamental in providing the flexibility to do this. The AD9516 contains a PLL and integrated VCO. It also contains a number of outputs that can be programmed for differential LVPECL, LVDS, or single-ended CMOS, with independent divider settings for each output path. In this circuit, one of these output paths is used for the DAC clock and another output is used for the reference input of the fractional-N PLL in the ADRF6702.

The advantage of using a fractional PLL in the ADRF6702 is twofold. First, the fractional PLL allows very fine tuning of the output LO. As an example, with an input frequency of 38.4 MHz and a programmed MOD value in the ADRF6702 of 1536, the LO can be programmed in increments of 25 kHz. The second advantage is that the reference frequency does not have to be equal to LO freq/divider ratio, but can be much higher, leading to a lower divider ratio. Because the output phase noise is a function of the reference phase noise multiplied by the divider ratio, this means inherently lower phase noise at RF.

One of the key metrics in a synthesizer system is the amount of phase noise added by the individual PLL and dividers. Figure 10 shows the noise floor of the spectrum analyzer doing the measurement (green trace), the phase noise of the reference generator (red), and the phase noise of an output tone at an RF frequency of 1961 MHz with an LO of 1940 MHz (yellow). The combination of the PLL in the AD9516 and the ADRF6702 does generate noticeably high close-in phase noise (less than 500 kHz offset from carrier) but does not contribute significant wideband noise to the system. The loop filters for the VCOs in both the AD9516 and ADRF6702 are set to bandwidths of ~100 kHz in the measurement circuit. Close-in phase noise may be reduced by lowering the bandwidth of these loop filters. System specifications should be reviewed to determine how much close-in phase noise can be tolerated for a given system.

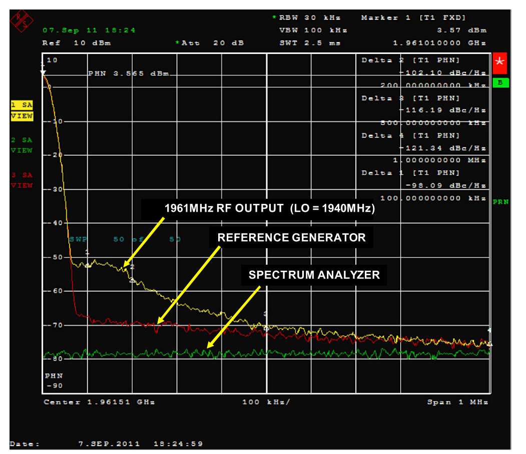

Figure 10. Spectrum Analyzer Noise Floor, Reference Phase Noise, and RF Output Phase Noise