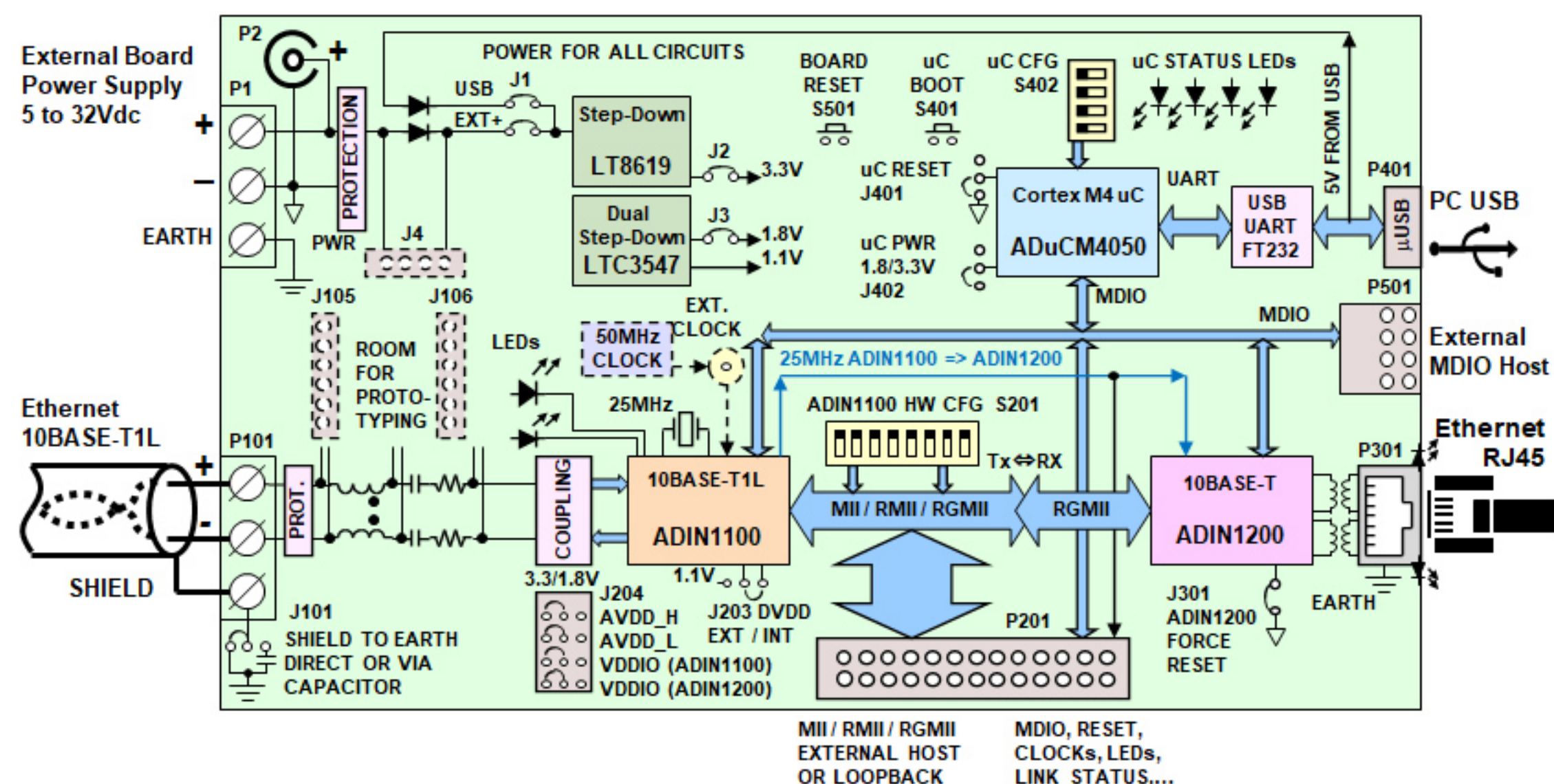


EVAL-ADIN1100EBZ

10BASE-T1L PHY Application / Evaluation Board
and Media Converter to 10BASE-T Ethernet

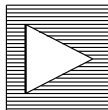
BLOCK DIAGRAM:



CONTENT:

- Page 1: BLOCK DIAGRAM:
- Page 2: ADIN1100 10BASE-T1L PHY
- Page 3: ADIN1200 10BASE-T PHY
- Page 4: ADuCM4050 Cortex M4 uC
- Page 5: Power and other circuits

REVISIONS				
REV	DESCRIPTION	DATE	APPROVED	

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	EVAL-ADIN1100EBZ ADIN1100, ADIN1200 LT8619, LTC3547, ADuCM4050			
	DESIGN VIEW Michal Brychta	DRAWING NO. 02_067422		REV C
	PTD ENGINEER Patrick Duignan	SIZE C	SCALE 1:1	SHEET 1 OF 5

ADIN1200 10BASE-T PHY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ADIN1200 MDIO PHY Address

X100b ~ 0x04 or 0x0C ~ 4d or 12d

E_RXD0 = TXD0 pull-down in ADIN1100

E_RXD1 = TXD1 pull-down in ADIN1100

E_RXD2 = TXD2 pull-up R303

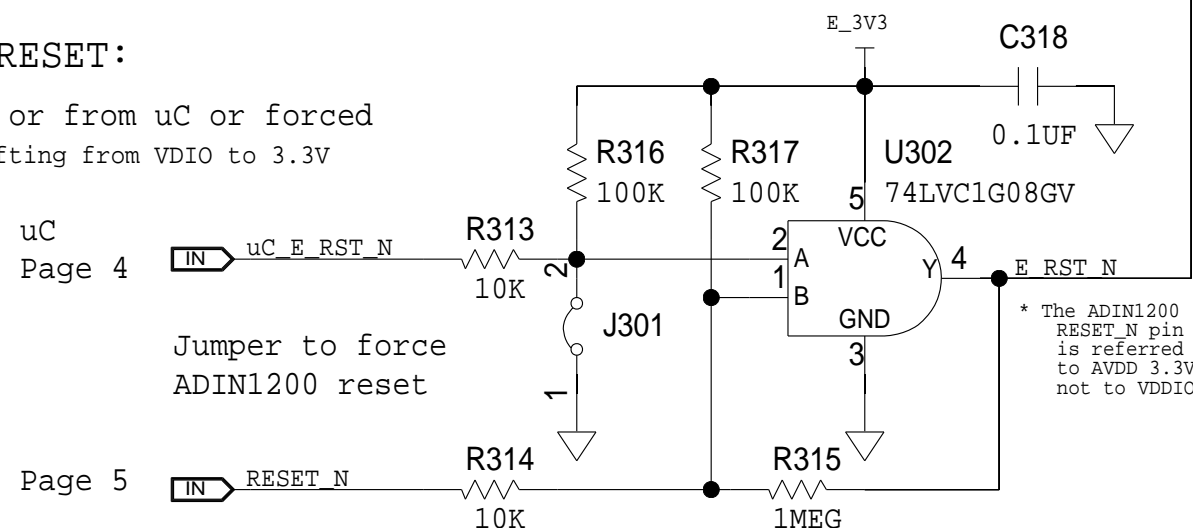
E_RXD3 = TXD3 = MEDIA_CNV by switch

uC
Page 4

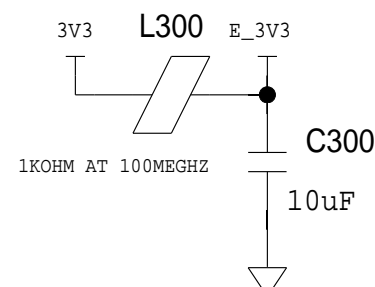
ADIN1100
Page 2

ADIN1200 RESET:

from global or from uC or forced
Also level shifting from VDDIO to 3.3V

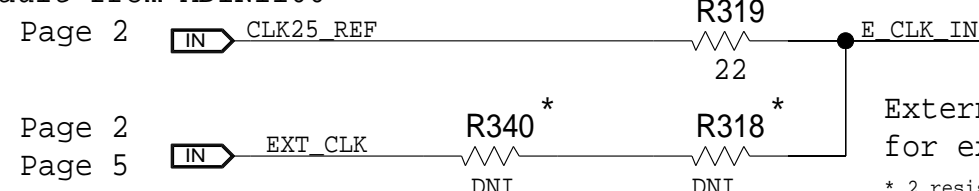


ADIN1200 POWER



ADIN1200 CLOCK

Default from ADIN1100



External clock option
for experiments

* 2 resistors default
not inserted to disconnect
a long unused track on PCB

ADIN1200 HW CONFIGURATION:

MDIX mode: Auto MDIX, Prefer MDI

CFG1-CFG0: Software Power Down
(PHY stays in reset after power up)

RJ45 with
integrated
transformer

P5
74984104400
WURTH ELEKTRONIK



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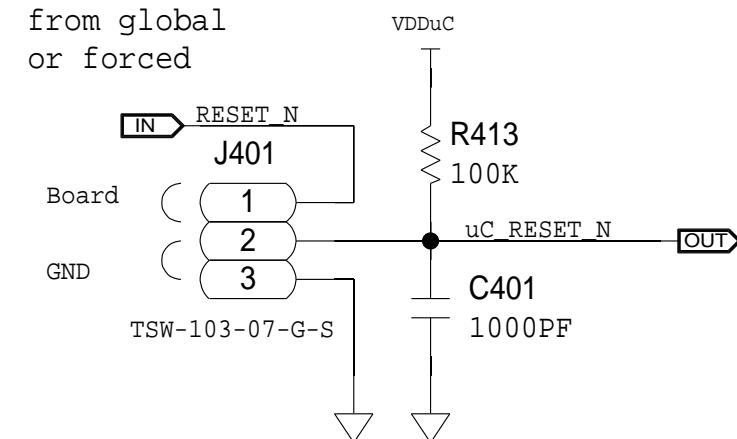
SCHEMATIC

EVAL-ADIN1100EBZ ADIN1100, ADIN1200 LT8619, LTC3547, ADuCM4050			
DESIGN VIEW Michal Brychta	DRAWING NO. 02_067422		REV C
PTD ENGINEER Patrick Duignan	SIZE C	SCALE 1:1	SHEET 3 OF 5

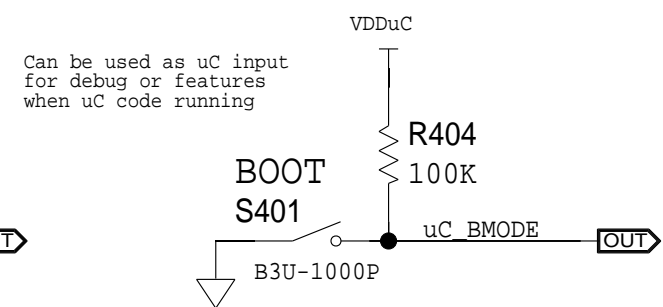
ADuCM4050 Cortex M4 uC

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

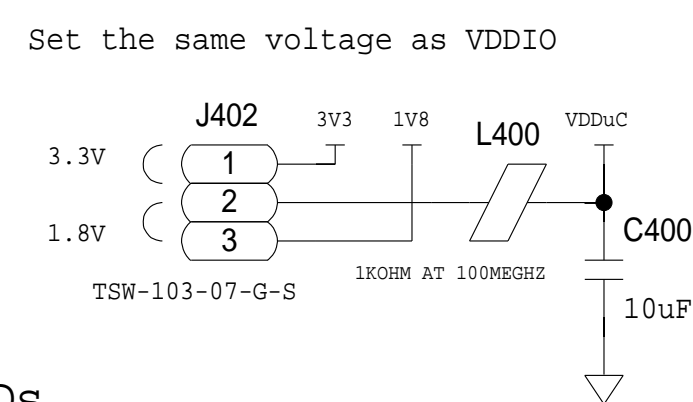
uC RESET
from global
or forced



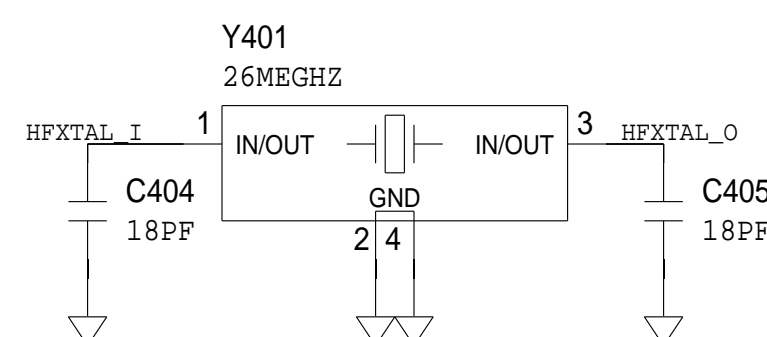
uC (UART) Bootload



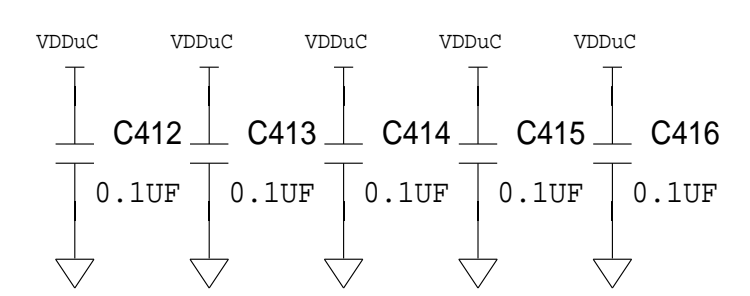
uC Power Selection



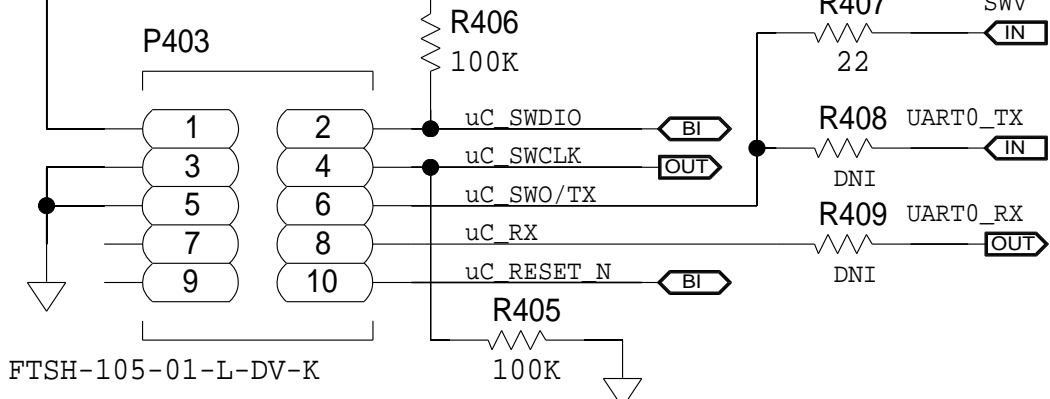
uC Clock



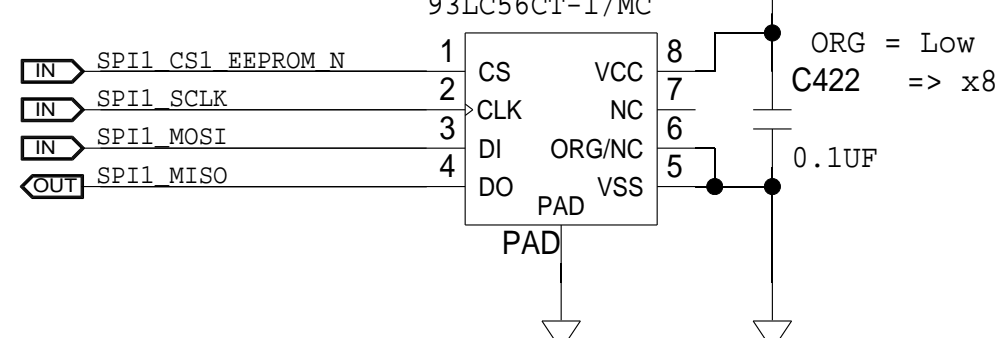
uC Decoupling Caps



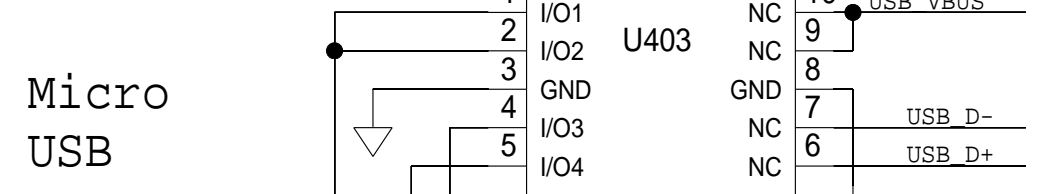
uC JTAG



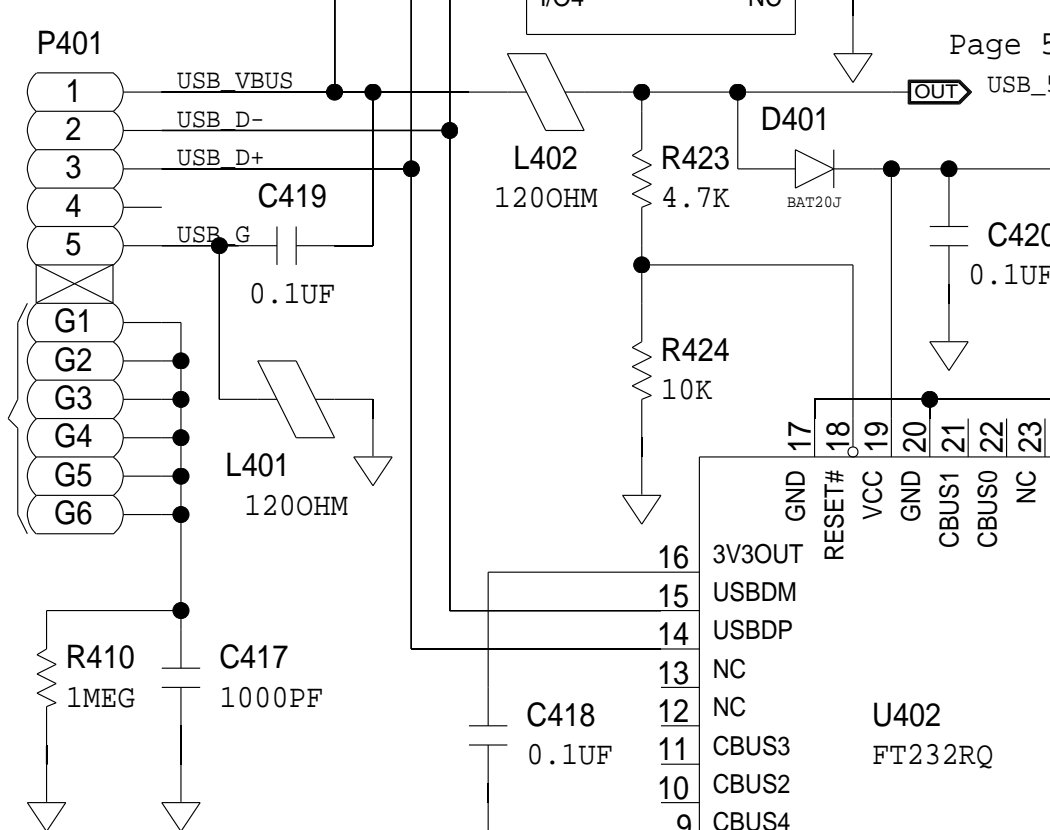
EEPROM



USB UART

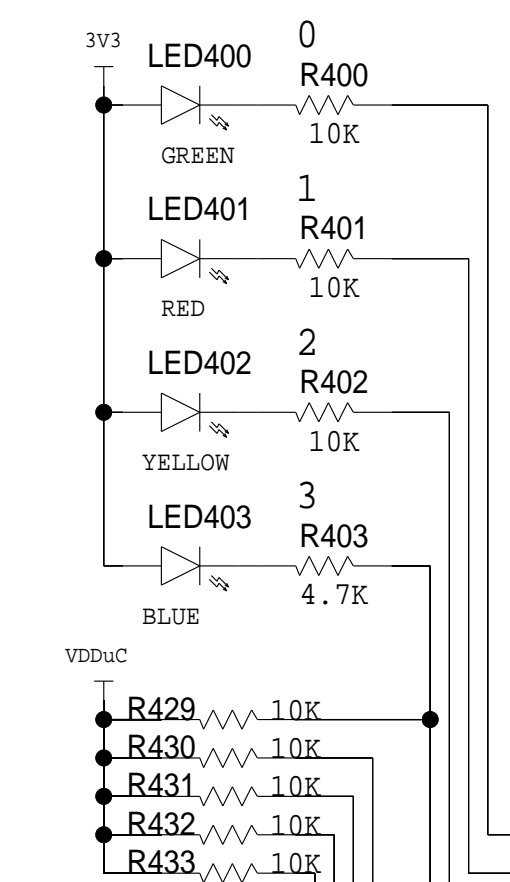


Micro USB

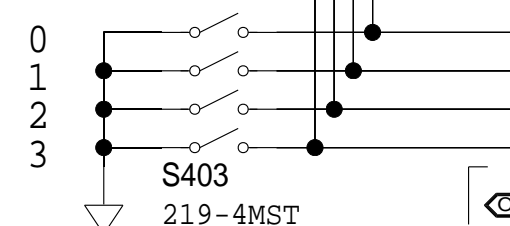


FT232 is always powered, either from USB VBUS or from board 3.3V. Otherwise draws power from VCCIO and affects RXD and TXD. When powered from board 3.3V, held in reset and takes only <100uA.

uC STATUS LEDs



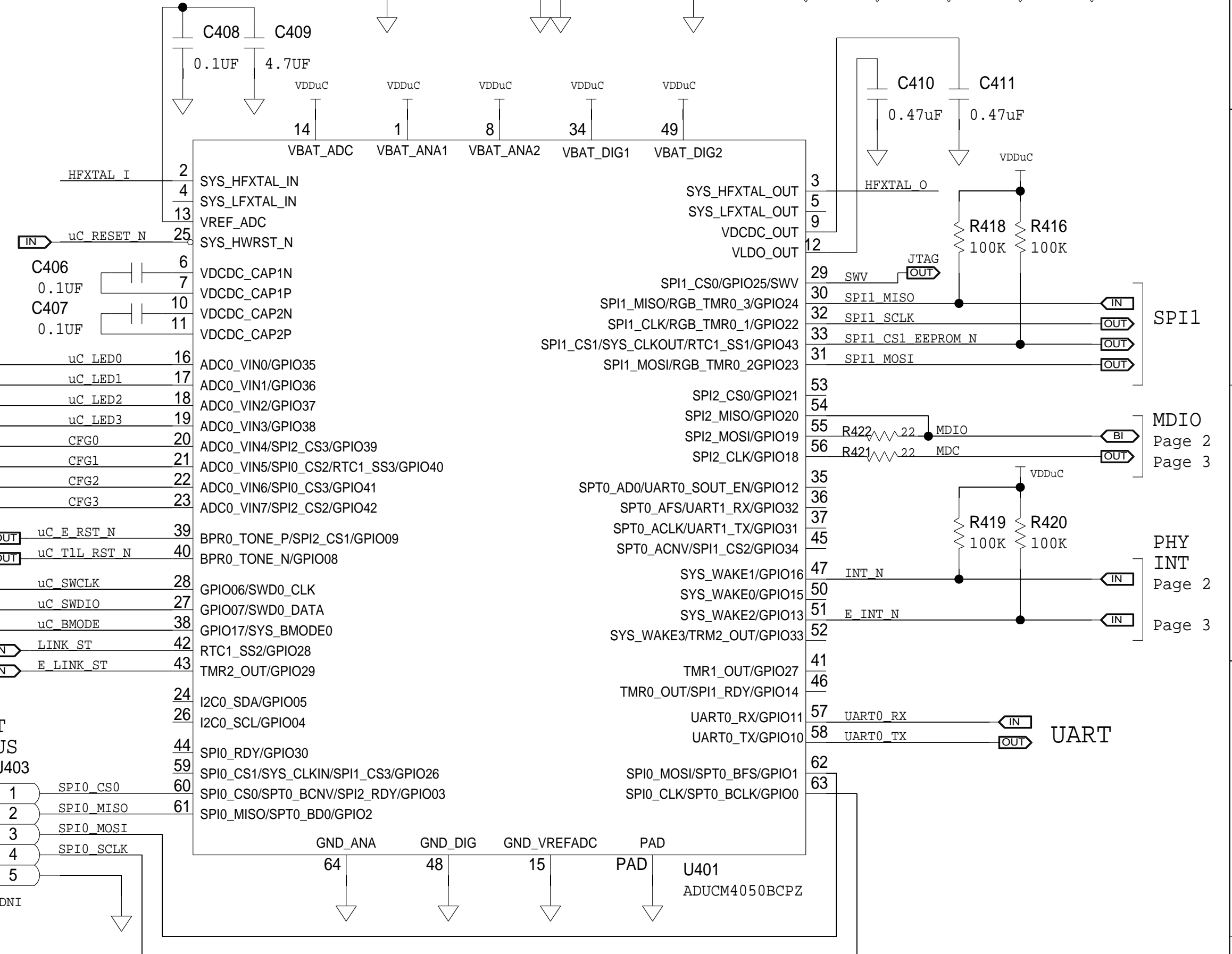
uC CFG



JTAG



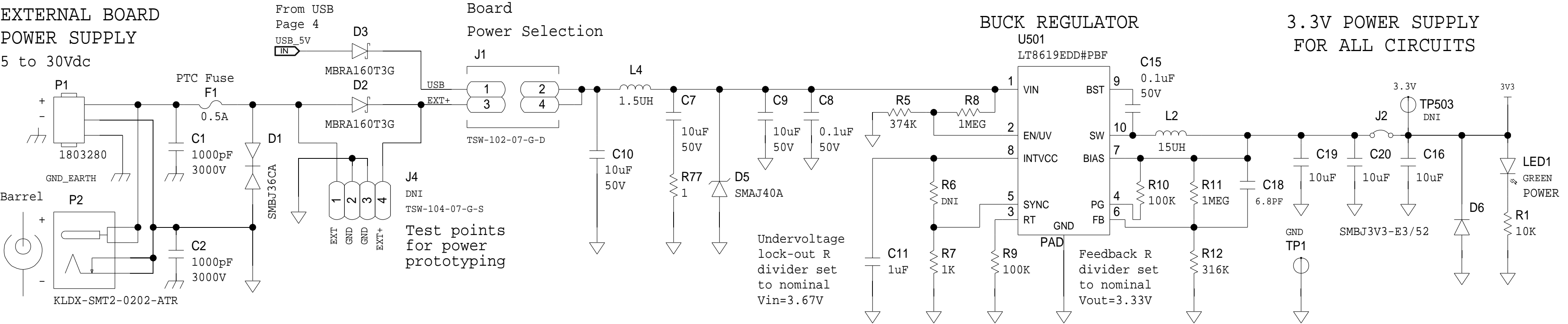
PHY RESET
PHY STATUS



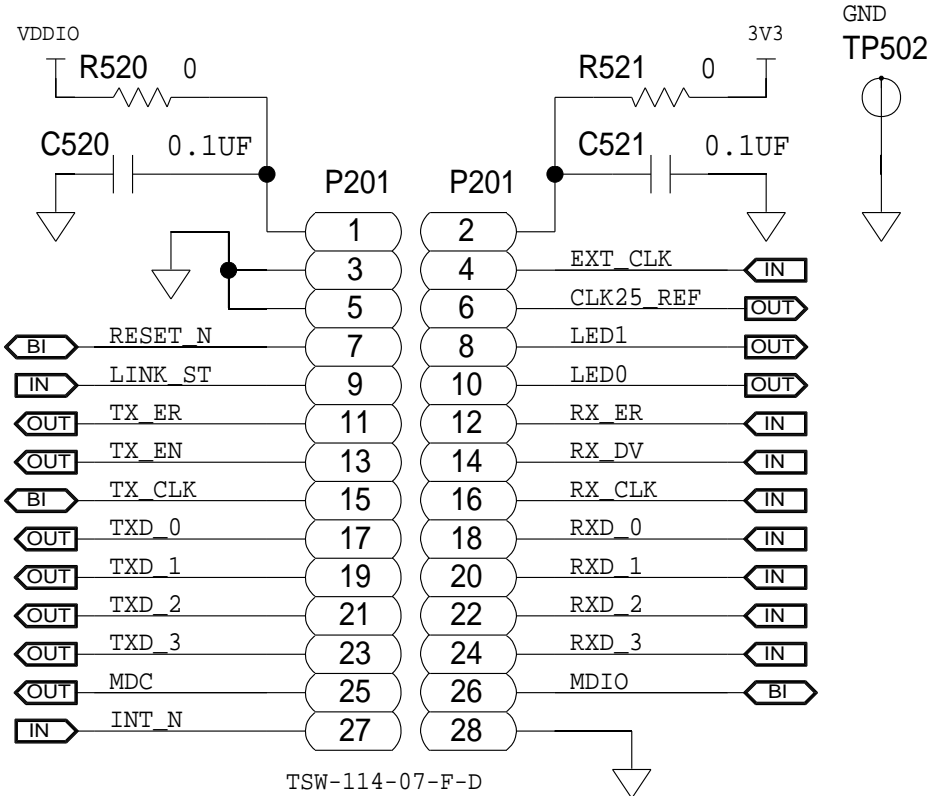
SCHEMATIC			
EVAL-ADIN1100EBZ ADIN1100, ADIN1200 LT8619, LTC3547, ADuCM4050			
DESIGN VIEW Michal Brychta	DRAWING NO. 02_067422	REV C	
PTD ENGINEER Patrick Duignan	SIZE C	SCALE 1:1	SHEET 4 OF 5

Power and other circuits

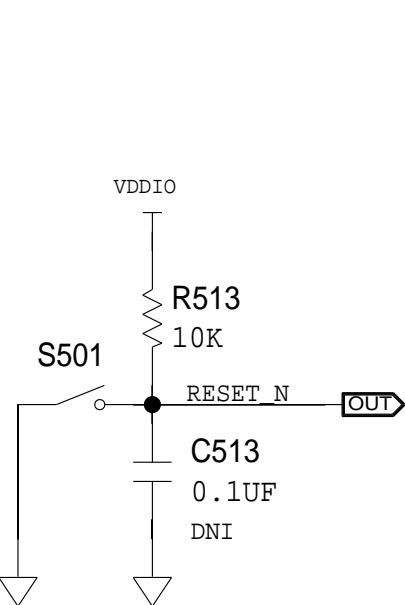
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



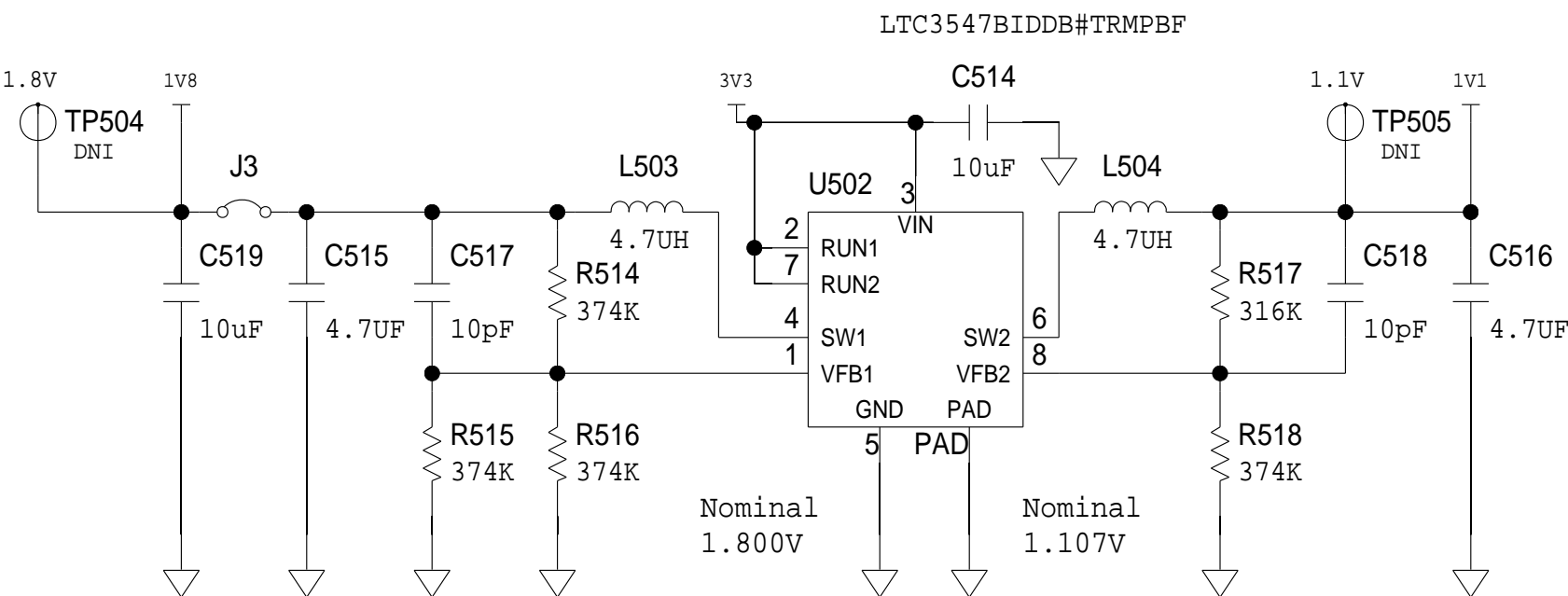
EXTERNAL MII/RMII/RGMII HOST (Including MDIO, clocks, reset, LEDs, ...)



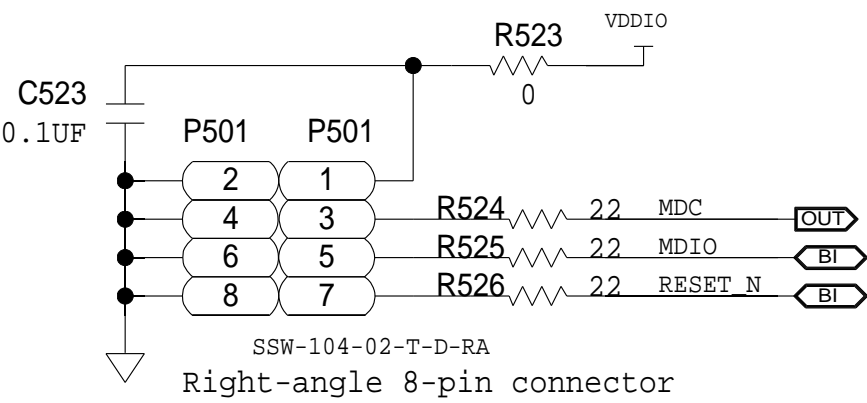
BOARD RESET ("Global")



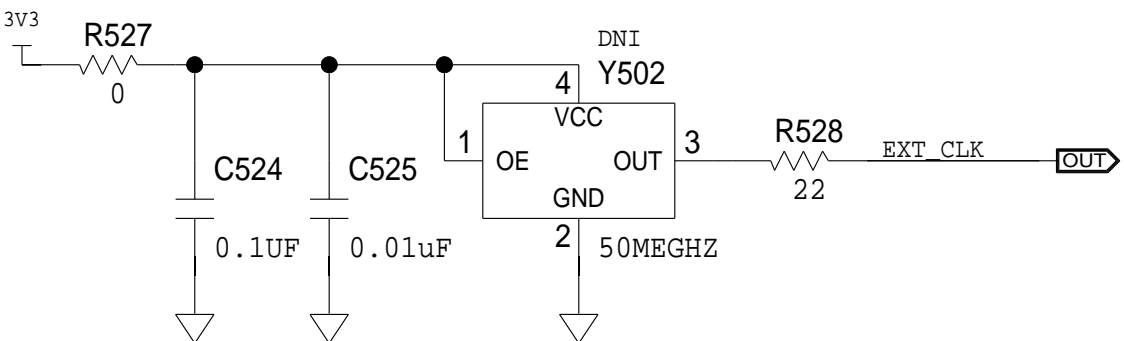
DUAL STEPDOWN from 3.3V to 1.8V and 1.1V



EXTERNAL MDIO HOST



OPTIONAL: 50MHZ CLOCK (Can be added for use with RMII)



SCHEMATIC			
EVAL-ADIN1100EBZ ADIN1100, ADIN1200 LT8619, LTC3547, ADuCM4050			
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PTD ENGINEER Patrick Duignan	SIZE C	SCALE 1:1	SHEET 5 OF 5