

## Auto-Zero In Amps

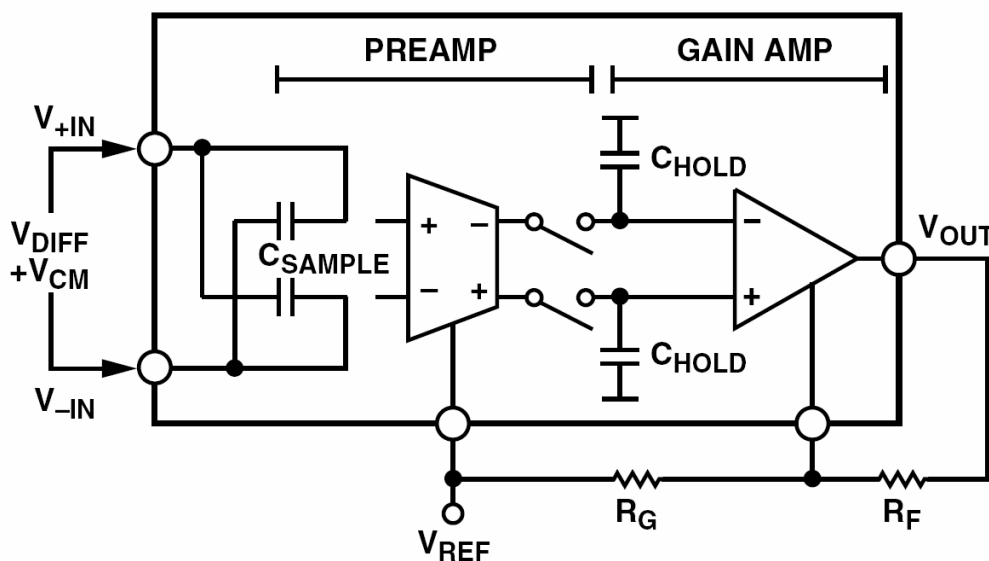
Auto-zeroing is a dynamic offset and drift cancellation technique that reduces input referred voltage offset to the  $\mu\text{V}$  level, and voltage offset drift to the  $\text{nV}/^\circ\text{C}$  level. The operation of standard auto-zero op amps is discussed in [Tutorial MT-055](#). This tutorial discusses the application of the auto-zero technique to instrumentation amplifiers.

### THE [AD8230](#) AUTO-ZERO INSTRUMENTATION AMPLIFIER

The [AD8230](#) is an instrumentation amplifier that utilizes an auto-zeroing topology and combines it with high common-mode signal rejection.

The internal signal path consists of an active differential sample-and-hold stage (preamp), followed by a differential amplifier (gain amp). Both amplifiers implement auto-zeroing to minimize offset and drift. A fully differential topology increases the immunity of the signals to parasitic noise and temperature effects. Amplifier gain is set by two external resistors for convenient TC matching. The AD8230 can accept input common-mode voltages within and including the supply voltages ( $\pm 5\text{ V}$ ). The signal sampling rate is controlled by an on-chip, 6 kHz oscillator and logic to derive the required nonoverlapping clock phases.

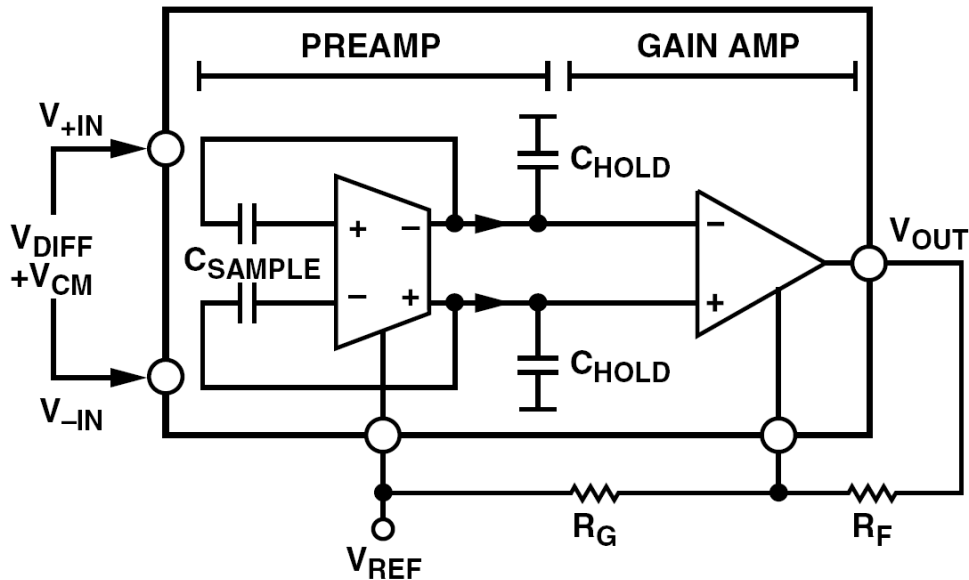
For simplification of the functional description, two sequential clock phases, A and B, will be used to distinguish the order of internal operation as depicted in Figures 1 and 2, respectively. Phase A (sampling phase) operation is shown in Figure 1.



**Figure 1: The [AD8230](#) Auto-Zero In-Amp in the Sampling Phase (Phase A)**

During Phase A, the sampling capacitors are connected to the input signals at the common-mode potential. The input signal's difference voltage,  $V_{DIFF}$ , is stored across the sampling capacitors,  $C_{SAMPLE}$ . The common-mode potential of the input affects  $C_{SAMPLE}$  insofar as the sampling capacitors are at a different common-mode potential than the preamp. During this period, the gain amp is disconnected from the preamp so that its output remains at the level set by the previously sampled input signal, held on  $C_{HOLD}$  in Figure 1.

In Phase B, upon sampling the analog input signals, the input common-mode component is removed. The Phase B state is shown in Figure 2.



**Figure 2: The AD8230 Auto-Zero In-Amp in the Transfer Phase (Phase B)**

The common-mode output of the preamp is held at the reference potential,  $V_{REF}$ . When the bottom plates of the sampling capacitors connect to the output of the preamp, the input signal common-mode voltage is pulled to the amplifier's common-mode voltage,  $V_{REF}$ . In this manner, the sampling capacitors are brought to the same common-mode voltage as the preamp. The remaining differential signal is presented to the gain amp, refreshing the hold capacitors' signal potentials, as shown in Figure 2. The gain amplifier conditions the updated signal stored on the hold capacitors,  $C_{HOLD}$ .

Both the preamp and the gain amp auto-zero. The preamp auto-zeros during Phase A while the sampling capacitors are connected to the signal source. By connecting the preamp differential inputs together, the resulting output-referred offset is connected to an auxiliary port to the preamp. Negative feedback forces a canceling voltage at the auxiliary port. During Phase B, the inputs of the preamp are no longer shorted, and the sampling capacitors are connected to the input and output of the preamp. The preamp, having been auto-zeroed in Phase A, has minimal offset. A separate nulling amplifier (not shown in the diagram) is used to accomplish the auto-

zero function. Further details regarding the operations of the AD8230 auto-zero in-amp can be found in Reference 3.

Although the AD8230 has only 3  $\mu\text{V}$  peak-to-peak RTI noise in the 0.1 Hz to 10 Hz bandwidth, the voltage noise spectral density @ 1 kHz is 240  $\text{nV}/\sqrt{\text{Hz}}$ . The AD8230 therefore requires an appropriate output RC filter to reduce the noise in the measurement bandwidth to an acceptable level.

Key specifications of the AD8230 auto-zero in-amp are given in Figure 3.

- ◆ Resistor programmable gain range: 101 to 1000
- ◆ Supply voltage range:  $\pm 4\text{ V}$  to  $\pm 8\text{ V}$
- ◆ Rail-to-rail input and output
- ◆ Maintains performance over  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- ◆ 110 dB minimum CMR @ 60 Hz,  $G = 10$  to 1000
- ◆ 10  $\mu\text{V}$  maximum offset voltage (RTI,  $\pm 5\text{ V}$  operation)
- ◆ 50  $\text{nV}/^\circ\text{C}$  maximum offset drift
- ◆ 20 ppm maximum gain nonlinearity
- ◆ 0.1 Hz to 10 Hz voltage noise RTI: 3  $\mu\text{V}$  peak-to-peak
- ◆ Voltage noise spectral density @ 1 kHz RTI: 240  $\text{nV}/\sqrt{\text{Hz}}$

**Figure 3: [AD8230](#) Auto-Zero In-Amp Key Specifications**

Auto-zero in amps from Analog Devices which are optimized for single-supply operation are the [AD8553](#), [AD8555](#), [AD8556](#), and [AD8557](#).

## REFERENCES

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as [Linear Circuit Design Handbook](#), Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 2.
2. Walter G. Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN 0-916550-26-5, Also available as [Op Amp Applications Handbook](#), Elsevier/Newnes, 2005, ISBN 0-7506-7844-5. Chapter 2.
3. Charles Kitchin and Lew Counts, [A Designer's Guide to Instrumentation Amplifiers, 3<sup>rd</sup> Edition](#), Analog Devices, 2006.

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