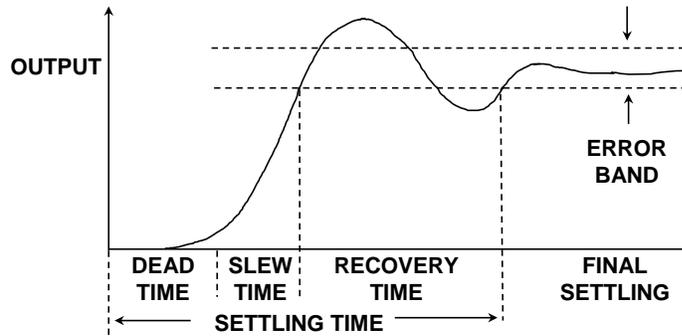


## Op Amp Settling Time

### SETTLING TIME

The *settling time* of an amplifier is defined as the time it takes the output to respond to a step change of input and *come into, and remain within a defined error band*, as measured relative to the 50% point of the input pulse, as shown in Figure 1 below.



- ◆ Error band is usually defined to be a percentage of the step 0.1%, 0.05%, 0.01%, etc.
- ◆ Settling time is non-linear; it may take 30 times as long to settle to 0.01% as to 0.1%.
- ◆ Manufacturers often choose an error band which makes the op amp look good.

**Figure 1: Settling Time**

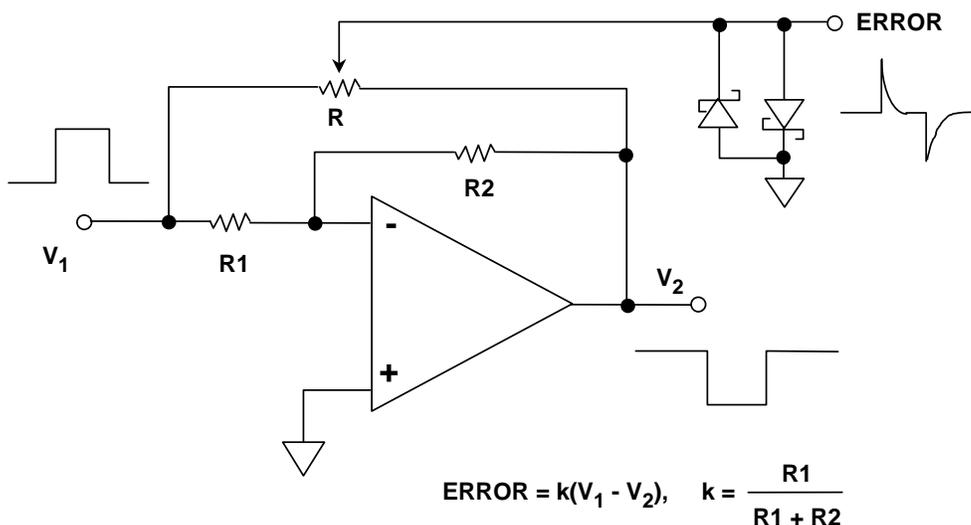
Unlike a DAC device, there is no natural error band for an op amp (a DAC naturally has an error band of 1 LSB, or perhaps  $\pm 1$  LSB). So, one must be chosen and defined, along with other definitions, such as the step size (1 V, 5 V, 10 V, etc.). What is chosen will depend on the performance of the op amp, but since the value chosen will vary from device to device, comparisons are often difficult. This is true because settling is not linear, and many different time constants may be involved. Examples are early op amps using dielectrically isolated (DI) processes. These had very fast settling to 1% of full-scale, but they took almost forever to settle to 10-bits (0.1 %). Similarly, some very high precision op amps have thermal effects that cause settling to 0.001% or better to take tens of ms, although they will settle to 0.025% in a few  $\mu$ s.

It should also be noted that thermal effects can cause significant differences between short-term settling time (generally measured in nanoseconds) and long-term settling time (generally measured in microseconds or milliseconds). In many ac applications, long-term settling time is not important; but if it is, it must be measured on a much different time scale than short-term settling time.

## MEASURING SETTTLING TIME

Measuring fast settling time to high accuracy is very difficult. Great care is required in order to generate fast, highly accurate, low noise, flat top pulses. Large amplitude step voltages will overdrive many oscilloscope front ends, when the input scaling is set for high sensitivity.

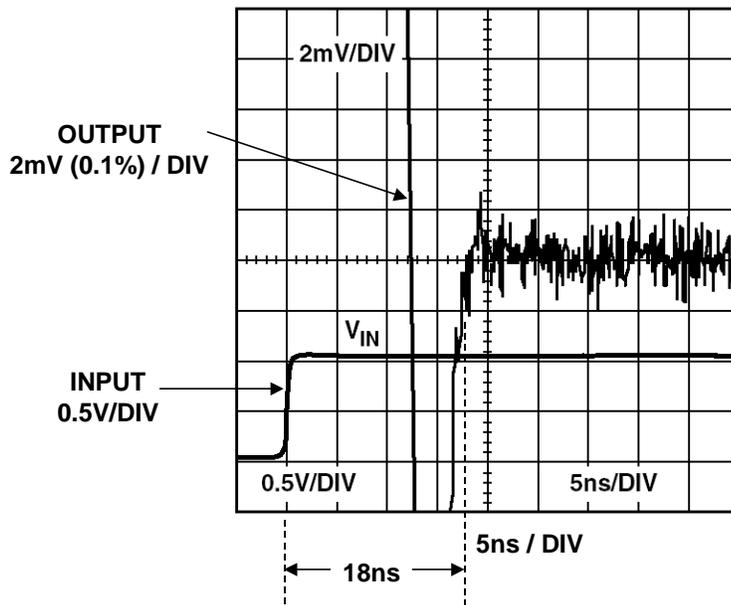
The example test setup shown in Figure 2 below is useful in making settling time measurements on op amps operating in the inverting mode. The signal at the "false summing node" represents the difference between the output and the input signal, multiplied by the constant  $k$ , i.e. the ERROR signal.



**Figure 2: Measuring Settling Time Using a "False Summing Node"**

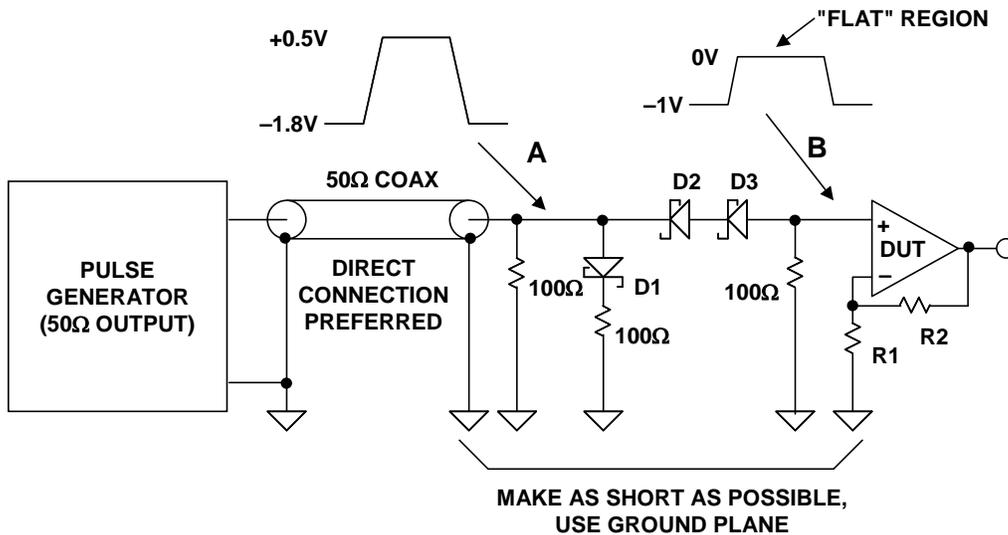
There are many subtleties involved towards making this setup work reliably. The resistances should be low in value, to minimize parasitic time constants. The back-back Schottky diode clamps help prevent scope overdrive, and allow high sensitivity. If  $R_1 = R_2$ , then  $k = 0.5$ . Thus the error band at the ERROR output will be 5 mV for 0.1% settling with a 10V input step.

In some cases, a second (very fast) amplifier stage may be used after the false summing node, to increase the signal level. In any case, testing of settling time must be done with a test setup identical to that used by the op amp manufacturer, to ensure validity. Many modern digitizing oscilloscopes are insensitive to input overdrive and can be used to measure the ERROR waveform directly—this must be verified for each oscilloscope by examining the operating manual carefully. Note that a direct measurement allows measurements of settling time in both the inverting and non-inverting modes. An example of the output step response to a flat pulse input for the [AD8039](#) op amp is shown in Figure 3 below. Notice that the settling time to 0.1% is approximately 18 ns.



**Figure 3: AD8039  $G = +2$  Settling Time Measured Directly**

In making settling time measurements of this type, it is also imperative to use a pulse generator source capable of generating a pulse of sufficient flatness. In other words, if the op amp under test has a settling time of 20 ns to 0.1%, the applied pulse should settle to better than 0.05% in less than 5 ns.



**Figure 4: A Simple Flat Pulse Generator**

This type of generator can be expensive, but a simple circuit as shown in Figure 4 can be used with a reasonably flat generator to ensure a flat pulse output.

The circuit of Fig. 4 works best if low capacitance Schottky diodes are used for D1-D2-D3, and the lead lengths on all the connections are minimized. A short length of 50  $\Omega$  coax can be used to connect the pulse generator to the circuit, however best results are obtained if the test fixture is connected directly to the output of the generator. The pulse generator is adjusted to output a positive-going pulse at "A" which rises from approximately  $-1.8$  V to  $+0.5$  V in less than 5 ns (assuming the settling time of the DUT is in the order of 20 ns). Shorter rise times may generate ringing, and longer rise times can degrade the DUT settling time; therefore some optimization is required in the actual circuit to get best performance. When the pulse generator output "A" goes above 0 V, D1 begins to conduct, and D2/D3 are reversed biased. The "0V" region of the signal "B" at the input of the DUT is flat "by definition"—neglecting the leakage current and stray capacitance of the D2-D3 series combination. The D1 diode and its 100  $\Omega$  resistor help maintain an approximate 50  $\Omega$  termination during the time the pulse at "A" is positive.

## REFERENCES

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as [Linear Circuit Design Handbook](#), Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 1.
2. Walter G. Jung, [Op Amp Applications](#), Analog Devices, 2002, ISBN 0-916550-26-5, Also available as [Op Amp Applications Handbook](#), Elsevier/Newnes, 2005, ISBN 0-7506-7844-5. Chapter 1.

Copyright 2009, Analog Devices, Inc. All rights reserved. Analog Devices assumes no responsibility for customer product design or the use or application of customers' products or for any infringements of patents or rights of others which may result from Analog Devices assistance. All trademarks and logos are property of their respective holders. Information furnished by Analog Devices applications and development tools engineers is believed to be accurate and reliable, however no responsibility is assumed by Analog Devices regarding technical accuracy and topicality of the content provided in Analog Devices Tutorials.