

Using the Test DAC on the ADF702x to Implement Functions Such as Analog FM DEMOD, SNR Measurement, FEC Decoding, and PSK/4FSK Demodulation

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INTRODUCTION

The ADF7020 and ADF7020-1 provide access to the FSK demodulator output to facilitate external measurement of functions such as demodulator output SNR, receiver eye-diagram analysis, and analog FM demodulation. For these measurements, access to the digital FSK demodulator output is achieved by using an on-chip $\Sigma\Delta$ (SD) modulator in conjunction with an external, passive RC network. This network provides an analog output signal (test DAC output) to replicate the output of the on-chip digital FSK demodulator.

In addition, the 1-bit oversampled SD output can be connected directly to an external DSP, such as the Blackfin® BF53x family from Analog Devices, Inc., or a high performance MCU. This connection facilitates additional signal processing of the received signal where such functions as Viterbi detection or PSK/QPSK/4FSK demodulation can be implemented.

FSK DEMODULATOR

Generating an Analog Output Signal

Figure 1 shows a block diagram of how to reconstruct the analog output of the digital FSK demodulator using an external RC filter.

The primary purpose of the RC filter is to remove the $\Sigma\Delta$ quantization noise. To achieve this goal, the effective 3dB bandwidth of the filter should be set at approximately $1.5\times$ to $2\times$ the data rate. There is a land pattern for a 3-stage RC or LC filter on the EVAL-ADF70XXMB board. When designing the filter, note that the effective 3dB bandwidth of a three-pole RC filter is equal to $0.51\times$ the bandwidth of a single-pole RC filter. For example, if the data rate (DR) = 9.6 kbps, aim for a cut-off frequency (f_c) of 15 kHz. Using standard realizable components, this yields R12, R13, R14 = 1 k Ω and C5, C6, C7 = 4.7 nF.

The $\Sigma\Delta$ DAC is clocked by the on-chip CDR_CLK. Although the test DAC functions in regular user mode, that is, when CDR_CLK is programmed to be $32\times$ the data rate, the best performance is achieved when CDR_CLK is increased to the frequency of DEMOD_CLK. This provides a sufficient oversampling rate for the $\Sigma\Delta$ converter. The CDR block does not function when this condition exists.

FUNCTIONAL BLOCK DIAGRAM

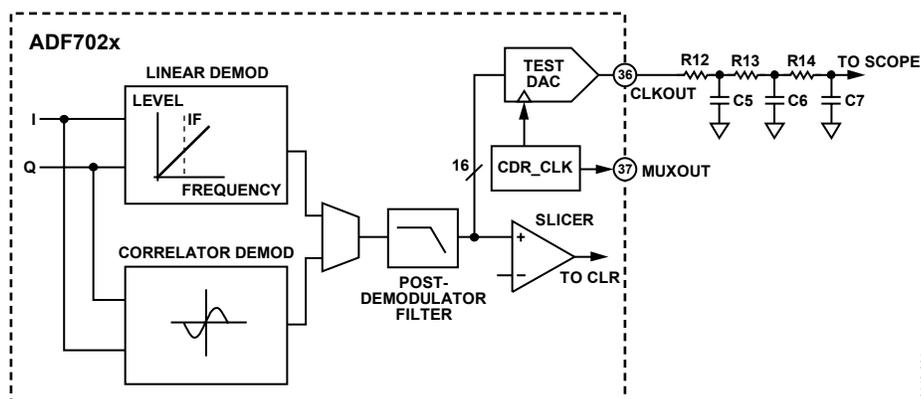


Figure 1. Test DAC Position In Rx Signal Chain

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Programming

Users can enable the test DAC to view the output of either the correlator or linear demodulator by programming the test register, Register 12.

If using the linear demodulator, some DC offset needs to be removed by programming Register 13. In this case, the output is proportional to frequency. As a result, the output consists of a DC offset equal to the IF frequency and the relatively low information signal whose output level is proportional to the frequency deviation. The offset can be removed and gained to use the full dynamic range of the DAC.

The user can determine the offset to be removed by using the frequency error readback to calculate the actual IF. Then, half of this value should be programmed into the offset removal field. Register 13 also has a signal gain term to allow the usage of the maximum DAC dynamic range. This setting should be incremented until the signal range at the output of the DAC spans from $V_{DD}/4$ to $3 \times V_{DD}/4$ at maximum RF input power. See Table 1 for the register writes needed to accomplish this.

VIEWING EYE DIAGRAMS

To view the eye diagram of the demodulated Rx signal, users should input an RF signal into the front-end that is modulated by PRBS data. Depending on the oscilloscope, users can then overlay multiple bit transitions to obtain an eye diagram (see Figure 2 and Figure 3 for two example outputs).

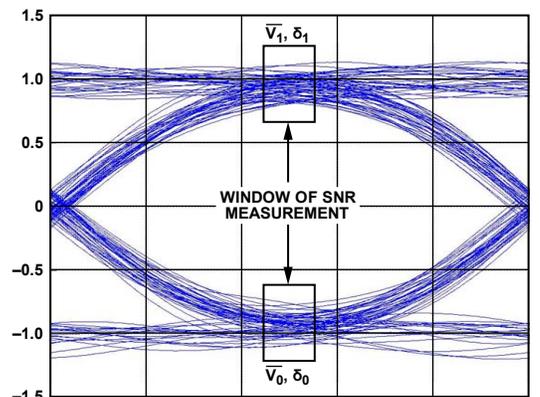


Figure 2. Eye Diagram for a 2-Level FSK Signal at the Test DAC Output

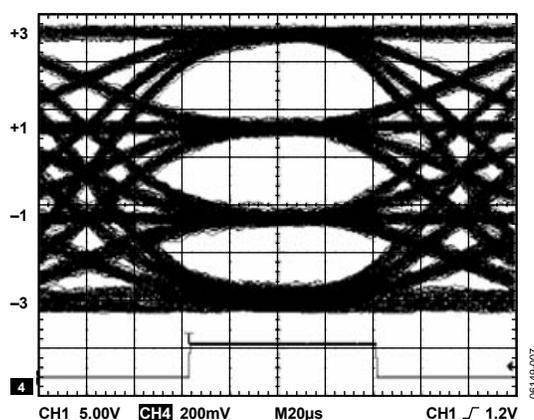


Figure 3. Eye Diagram for a 4-Level FSK Signal at the Test DAC Output

Table 1. Register Values for Programming the Test DAC Output in Linear and Correlator Demodulator Modes

Demodulator Mode	Register Programming	Description
Correlator	0x0001 C00C	Digital Test Mode 7: Enable TEST-DAC.
Linear	0x0001 C00C	Digital Test Mode 7: Enable TEST-DAC.
	0x02 800C	Digital Test Mode 10: Enable TEST-DAC offset removal.
	0x8026 000D	Register13—Offset Removal: Depends on actual IF frequency.

SNR Measurement of the Demodulator Output

The SNR is calculated by first measuring the average signal levels for Level 0 and Level 1, and then by measuring the standard deviation of the noise power for both levels. These measurements should be made at the middle of the eye. The following formula gives an SNR number in dB:

$$SNR(dB) = 20 \log \frac{(\overline{V_1} - \overline{V_0})}{\sqrt{\sigma_0^2 + \sigma_1^2}}$$

where:

\overline{V} = average signal level

σ = standard deviation of the noise power

Figure 4 shows SNR vs. RF input level and bit-error rate (BER) vs. RF input level on the secondary axis. The sensitivity level of the Rx is usually taken at the point where the BER = 1E - 3. The minimum SNR required for the demodulator to demodulate correctly can also be be taken from the graph by drawing a straight line across the sensitivity point. This is shown in Figure 4 by two dashed horizontal lines; one equals ~17 dB for the correlator demodulator and the other is 24 dB for the linear demodulator.

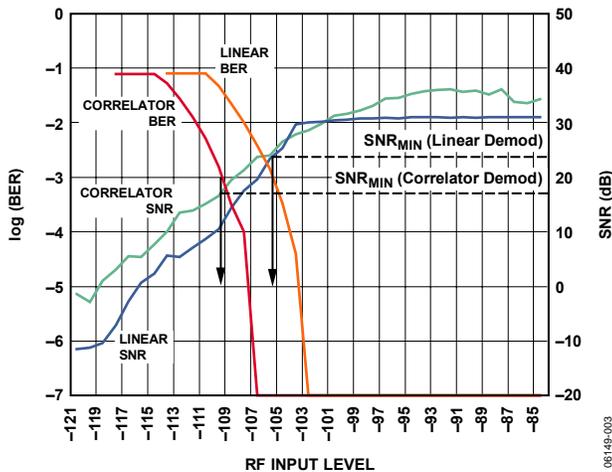


Figure 4. SNR and BER vs. RF Input Level

ANALOG FM ON ADF7020-1

The ADF7020-1 operates from 80 MHz to 650 MHz and, therefore, can be tuned to receive FM bands from 87.5 MHz to 108 MHz. Figure 5 and Figure 6 show a low cost implementation of a mono FM receiver using the ADF7020-1, an external filter, and a PA. The RC filter cutoff and post-demodulator bandwidth should be set at 12 kHz to 15 kHz, and should provide adequate attenuation of the pilot tone at 19 kHz. It is possible to receive stereo FM using an external stereo decoder, such as the LA3430 device from Sanyo, and setting the effective bandwidth of the RC filter and the post-demodulator bandwidth above the RDS channel of 57 kHz.

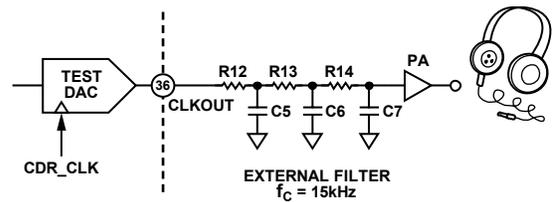


Figure 5. Circuit Connectivity for Mono/Stereo FM Reception

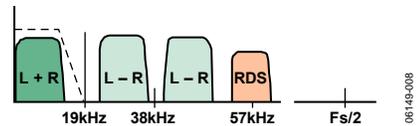


Figure 6. Composite FM Spectrum Available at TEST DAC Output

VITERBI DECODING, PSK DEMODULATION, AND 4-LEVEL FSK DEMODULATION

For communication channels that require additional post-processing of the FSK demodulator output, such as Viterbi detection, PSK/QPSK demodulation, or 4FSK symbol timing recovery, the output of the FSK demodulator can be easily interfaced to a DSP, such as the Blackfin BF53x or a high performance MCU. This can easily be accommodated by connecting the 1-bit oversampled $\Sigma\Delta$ modulator output of the ADF7020 to an input port on the DSP/MCU.

A synchronous clock (CDR_CLK) for the 1-bit $\Sigma\Delta$ modulator output is also provided by the ADF7020. This clock is made available on the MUXOUT pin (Pin 37). Full details of the required test modes to enable both the test DAC and test DAC clock are listed in Table 2.

Table 2. Register Values for Programming the Test DAC Output and Test DAC Clock in Linear and Correlator Demodulator Modes

Demodulator Mode	Register Programming	Description
Correlator	0xDxxx xxx0	Enable PLL Test Modes in Register 0.
	0x0001 C1EC	Digital Test Mode 7 and PLL Test Mode 30: Enable TEST-DAC and TEST-DAC clock.
Linear	0xDxxx xxx0	Enable PLL Test Modes in Register 0.
	0x0001 C1EC	Digital Test Mode 7 and PLL Test Mode 30: Enable TEST-DAC and TEST-DAC clock.
	0x02 800C	Digital Test Mode 10: Enable TEST-DAC offset removal.
	0x8026 000D	Register13—Offset Removal. Depends on actual IF frequency.

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The following is a sample of post-processing tasks that can be performed in DSP or high performance MCU using this interface:

- Forward error correction (FEC)
- PSK/QPSK demodulation
- 4FSK timing recovery
- Stereo/RDS decoder in DSP
- Satellite receiver for automotive telematics (ADF7020-1 in the 138 MHz band)

Forward Error Correction (FEC)

For applications requiring improved channel robustness, improved receiver sensitivity, and/or reduced output power, FEC techniques, such as convolutional coding, can be implemented on an external DSP/MCU in conjunction with the ADF7020 transceiver. In general, the complexity of the convolutional encoder is relatively straightforward, and is performed on the transmit bit stream applied to the ADF7020. The complexity of the convolutional decoder is exponentially dependant on the number of states in the trellis and is usually implemented as a Viterbi decoder. However, this complexity is easily handled by a high performance DSP, such as the BF53x or a high performance MCU.

Figure 7 shows a block diagram of the overall system. In this case, both the convolutional encoder and Viterbi detector are implemented in the DSP. Access to the ADF7020 FSK demodulator output is provided by connecting the oversampled 1-bit $\Sigma\Delta$ modulator output (Pin 36) and clock (Pin 37) to the DSP general-purpose flags or SPORT interface. The first stage of the DSP performs low-pass filtering and decimation of the 1-bit $\Sigma\Delta$ modulator output to reconstruct the multibit FSK demodulator output signal. This provides soft-decision values for Viterbi detection and symbol timing recovery.

Depending on the constraint length of the convolutional code used, significant signal processing gain can be achieved. For example, if a $\frac{1}{2}$ rate convolutional code is used with a constraint length of 7 bits on the radio link, up to 8.9 dB of processing gain can be achieved. Allowing for the $\frac{1}{2}$ rate code loss, this system provides an effective signal processing gain of up to 5.9 dB compared to an uncoded channel.

For more details about FEC implementation on the Blackfin, visit: http://www.analog.com/library/analogDialogue/archives/39-03/smart_modem.html

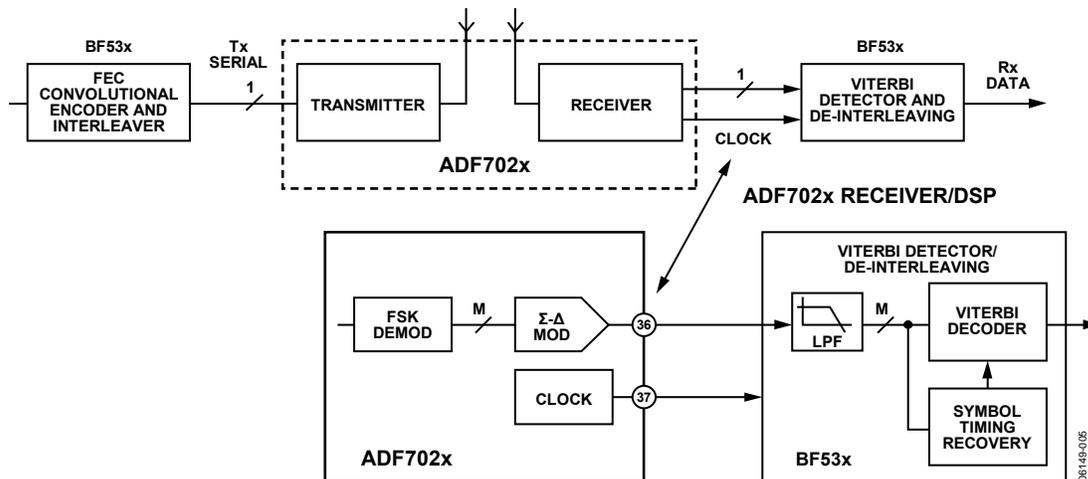


Figure 7. Interface Diagram Showing Connections Required for FEC Decoding

PSK/QPSK Demodulation

For systems that utilize PSK or QPSK modulation, it is possible to perform the appropriate phase demodulation using the ADF7020 in conjunction with a Blackfin DSP. A basic system level diagram is shown in Figure 8. The SD modulator output and clock from the ADF7020 are interfaced as described in the Forward Error Correction (FEC) section. PSK and QPSK modulation can be demodulated by performing an integration operation (integrate and dump) that recovers the phase information from the FSK demodulator output. Note that the ADF7020 is capable of supporting transmit and receive of OQPSK modulation with sinusoidal Tx baseband shaping without the need for an external DSP. This is because the modulation is equivalent to minimum shift keying (MSK).

4FSK Symbol and Timing Recovery

The ADF7020 can also be used to implement 4FSK demodulation with symbol timing recovery in conjunction with a Blackfin DSP

or high performance MCU. In this application, the ADF7020 FSK correlator demodulator is used to provide frequency discrimination of the 4 FSK symbols. Symbol timing recovery is implemented in DSP. The interface between the ADF7020 and BF53x is implemented via the SD modulator output in the same way as described in the Forward Error Correction (FEC) section.

Eye diagrams for the 4 FSK symbols (-3, -1, +1, and +3) can be examined by low-pass filtering the output of the SD modulator (see Figure 3 for an example). For optimum performance of the ADF7020 correlator demodulator in 4 FSK, it is recommended to set the correlator bandwidth to $4 \times$ the deviation frequency used to represent the +1 and -1 symbols at the transmitter. For example, if the transmitter frequencies used to represent the 4FSK symbols (-3, -1, +1, +3) are -2.4 kHz, -800 Hz, +800 Hz, and +2.4 kHz respectively, the ADF7020 FSK correlator's discriminator bandwidth (programmed in Register 6) should be optimized for a bandwidth of $4 \times 800 \text{ Hz} = 3.2 \text{ kHz}$.

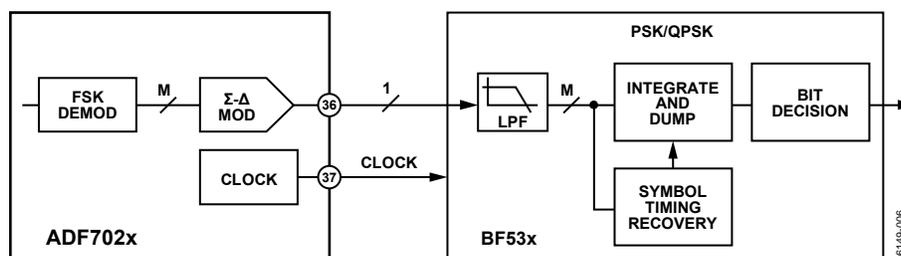


Figure 8. Implementing PSK Demodulation Using the ADF7020 and the Blackfin DSP

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NOTES