

Set-Up and Hold Measurements in High Speed CMOS Input DACs

by Steve Reine

To achieve optimal performance from a high speed DAC, set-up and hold times must be adhered to. At clock rates of 200 MSPS to 250 MSPS, the entire timing budget for the FPGA/ASIC/DAC is not a trivial task. For customers to complete their timing verification, the timing specifications in the data sheet must be clearly laid out and well defined.

When set-up and hold times are met, the data at the DAC internal latch is stable when the clock edge gets to the latch. If the data is in transition when the latching clock edge arrives, the data that gets latched will be non-deterministic, and thus, will increase the noise floor of the DAC analog output. A violation of a few tenths of ns on DACs, such as the AD9777 or AD9786, can make a dramatic impact on the DAC noise floor. Figure 1, Figure 2, and Figure 3 show oscilloscope measurements on the AD9786 clock input/output and data signals when the set-up time is just being met, when it has been violated by 0.1 ns, and when it has been violated by 0.5 ns. In this situation, the AD9786 is in Master Mode with 1x interpolation, so the input sample rate is the same as the DAC output sample rate. Note that Figure 1 implies that the set-up time for this DAC under these conditions is -0.7 ns. The negative set-up time is due to the keep out window shifting entirely to the right of the clock latching (in this case, falling) edge. The dotted line in all three plots indicates the middle of the clock edge, and the solid lines indicate the middle of the data transition.

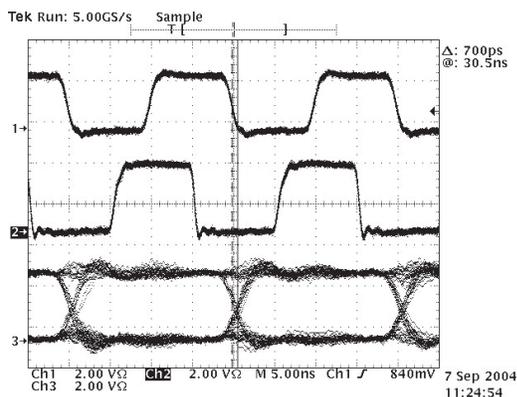


Figure 1. DAC Timing Just Meeting Set-Up Time

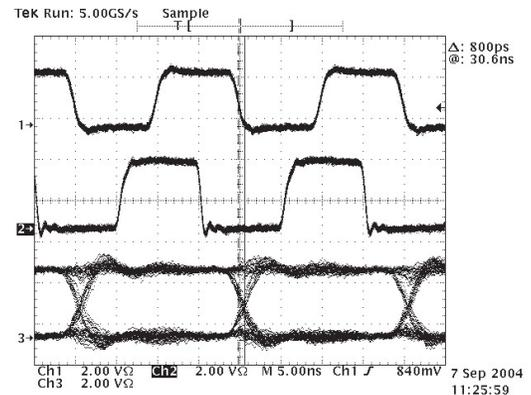


Figure 2. DAC Timing Violating Set-Up Time by 0.1 ns

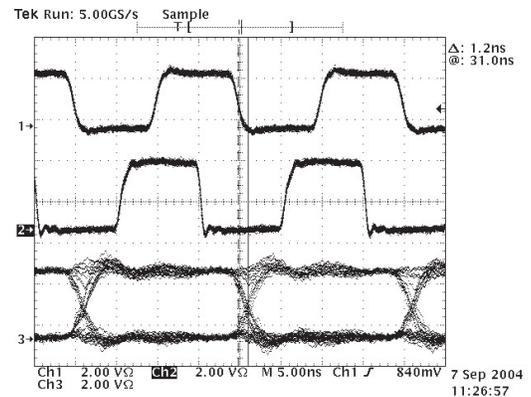


Figure 3. DAC Timing Violating Set-Up Time by 0.5 ns

Also note that the defined set-up (or hold time) indicates the time at which the data is valid, not the time at which the timing is broken. The user has to meet the defined set-up/hold time and no more to achieve optimal performance.

Traditionally, the set-up time is the amount of time before the clock latching edge at which point the data must be stable. This time is usually defined as a minimum spec. Digital designers define the set-up time as the minimum amount of time before the latching edge that the data must become stable. As an example, a set-up time of 1 ns (min) implies that the data must be stable at least 1 ns before the clock latching edge.

Hold time is the amount of time after the latching edge during which time the data must remain stable for the data to be accurately acquired. Hold time is typically defined as a minimum time. An example is that a hold time of 2 ns (min) implies that the data must be stable at least 2 ns after the latching clock edge.

The keep out window is defined as the total window around the latching clock edge which includes both the set-up and hold times. In the examples given previously, with 1 ns setup and 1 ns hold, the keep out window is from 1 ns before the clock latching edge to 1 ns after.

The traditional definitions for setup and hold are easily understood. However, in high speed DACs, complex clock trees and high sample rates sometimes mean that the delay between the externally applied latching clock edge and the actual time that the data is latched may be a significant part of a clock cycle. A typical DAC clock tree and latch structure is shown in Figure 4.

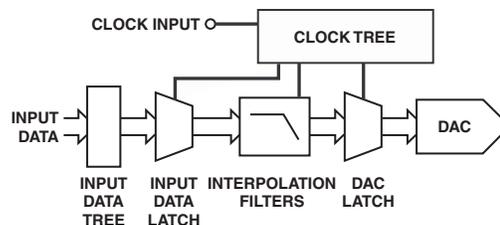


Figure 4. Typical Interpolating DAC Clock

With Analog Devices AD9777 or AD9786 interpolating DACs, in this situation the keep out window may be delayed far enough so that the set-up time may be 0.0, or even a negative number. A particular DAC may have a set-up time of -1.0 ns, and a hold time of 3.0 ns. The keep out window in this case would be from 1 ns after the clock latching edge to 3 ns after the clock latching edge. It's also possible, although less likely, that due to the synchronization inside the DAC, the keep out window has actually moved to the left, or advanced in time. In this case the set-up time would be positive, and the hold time would be a negative number. Figure 5a, Figure 5b, and Figure 5c summarize the situations where the keep out window is symmetrical about the latching clock edge, shifted to the right (set-up time is negative), or shifted to the left (hold time is negative).

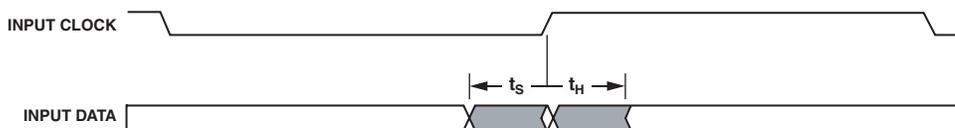


Figure 5a. Set-Up and Hold Times are Symmetric about Latching Clock Edge (t_s and t_H are both positive)

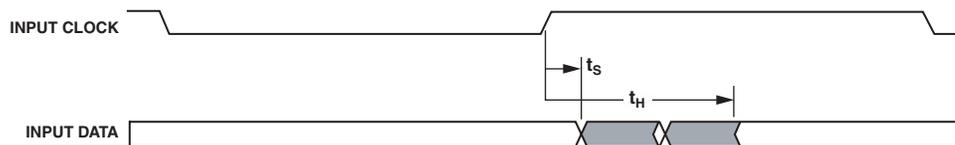


Figure 5b. Set-Up and Hold Times are Delayed from Latching Clock Edge (t_s is negative, t_H is positive)

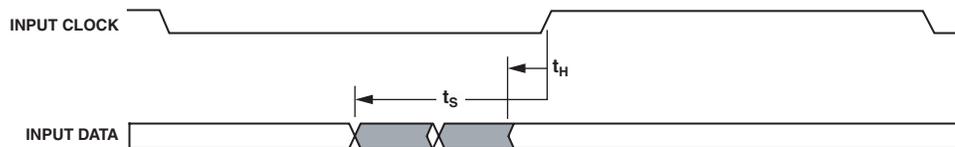


Figure 5c. Set-Up and Hold Times are Advanced in Time from Latching Clock Edge (t_s is positive, t_H is negative)

To a digital designer, the fact that the set-up time or the hold time is negative is not very important. It's much more important that the entire keep out window be as short as possible. The timing specifications on the DAC represent only a portion of the entire timing budget of the FPGA or ASIC digital interface to the DAC. Quite often, the applications engineer is required to test many parts in a lot or multiple lots to see how the set-up, hold times, and keep out window vary, sometimes even over temperature. On the FPGA or ASIC driving the DAC digital inputs, DLLs or other similar synchronization devices may be used which have their own variability. High speed CMOS input DACs may run as high as 250 MSPS, giving a total cycle time of 4 ns. In this case, the keep out window of the DAC itself will probably be on the order of 1 ns to 1.5 ns. This implies that over 25% of the timing budget has already been used by the DAC, so that the digital designer will have to be very careful with the timing in the digital engine driving the DAC.

Measuring Set-Up and Hold Times

High speed DACs are frequently used in wireless transmitter applications. For this reason, many of their specifications are spectral rather than time domain based. Examples of this are spurious free dynamic range (SFDR), spectral noise density, and adjacent channel leakage ratio (ACLR). Set-up and hold times for high speed DACs are therefore measured spectrally. Figure 6 shows a DAC sampling at 50 MSPS, reconstructing a signal at 2.4 MHz. In Figure 6, the set-up and hold times are being met. In Figure 7, the timing for the DAC has just violated the keep out region by 0.1 ns. Whether or not the timing has violated set-up or hold does not matter, as breaking either of these conditions gives the same behavior. Notice in Figure 7 how the noise floor has been noticeably elevated. This is the indication that the timing specs have been violated. In Figure 8, the timing specs have been violated by 0.5 ns, and it becomes very clear that the timing synchronization has been broken, and that the analog output performance of the DAC has been seriously degraded.

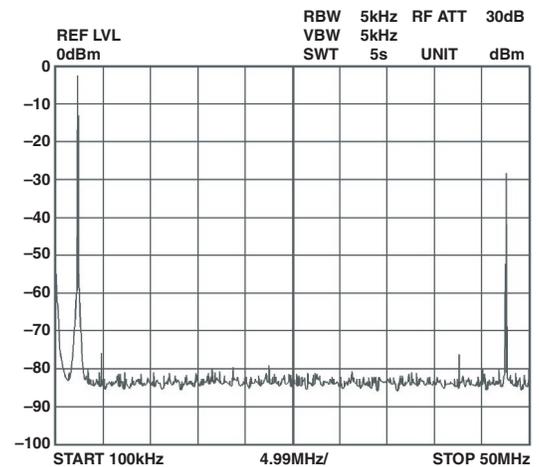


Figure 6. DAC Timing Meeting Set-Up and Hold Requirements

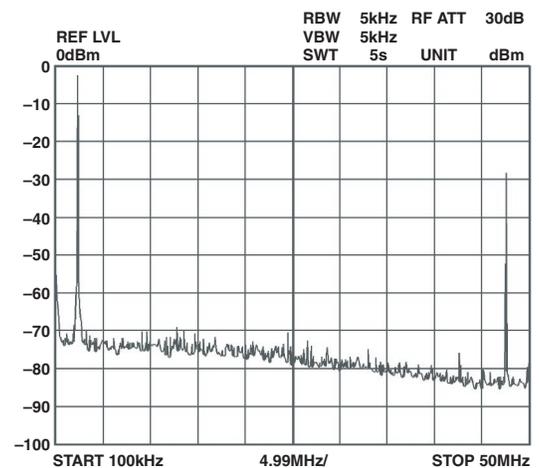


Figure 7. DAC Timing Violating Set-Up and Hold Requirements by 0.1 ns

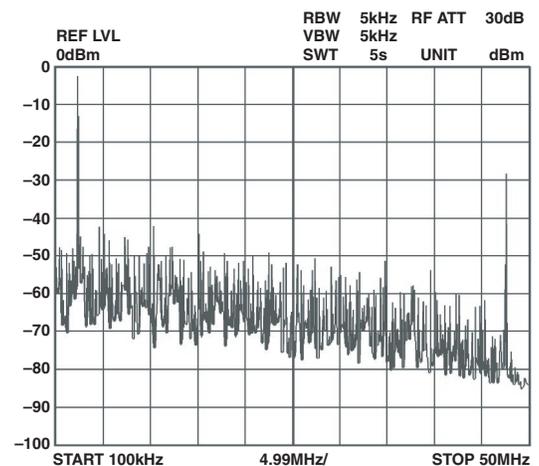


Figure 8. DAC Timing Violating Set-Up and Hold Requirements by 0.5 ns

