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Devices Connected/Referenced	
AD7195	4.8 kHz, Ultralow Noise, 24-Bit Σ - Δ ADC with PGA and AC Excitation
ADP3303	5 V Low Dropout Linear Regulator
ADP3303	3.3 V Low Dropout Linear Regulator

Precision Weigh Scale Design Using a 24-Bit Sigma-Delta ADC with Internal PGA and AC Excitation

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

[AD7195 Evaluation Board \(EVAL-AD7195EBZ\)](#)

Design and Integration Files

[Schematics, Layout Files, Bill of Materials](#)

CIRCUIT FUNCTION AND BENEFITS

This circuit is an ac excited weigh scale system that uses the AD7195, an ultralow noise, low drift, 24-bit Σ - Δ ADC with internal PGA and drivers to implement ac excitation of the load cell.

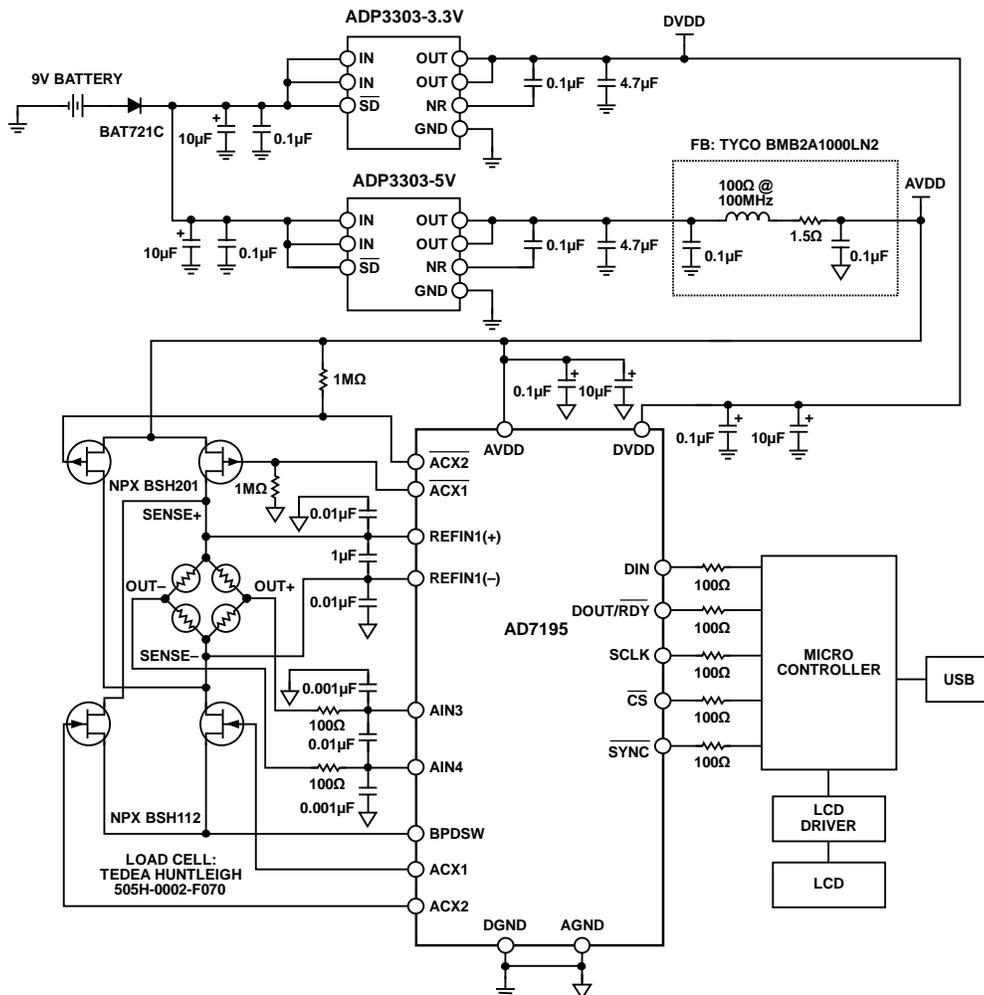


Figure 1. Weigh Scale System Using the AD7195 with AC Excitation (Simplified Schematic: All Connections Not Shown)

Rev. A

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The AD7195 simplifies the weigh scale design in low offset systems because most of the system building blocks are included on the chip. The AD7195 maintains good performance over the complete output data rate range, from 4.7 Hz to 4.8 kHz, which allows it to be used in weigh scale systems that operate at low speeds along with higher speed weigh scale systems.

CIRCUIT DESCRIPTION

With ac excitation, the polarity of the excitation voltage to the load cell is switched using external MOSFETs. Consecutive values are then averaged, which removes dc induced offsets. The AD7195 contains the internal logic to control the switching of the external MOSFETs. The driver signals from the AD7195 are precisely timed and nonoverlapping, which ensures that no short circuit occurs when switching the polarity of the bridge drive voltage. Pull-up and pull-down 1 M Ω resistors are connected to ACX2 and ACX2 to prevent short-circuiting during power-up.

The AD7195 provides an integrated solution for ac excited load cells. The AD7195 can accept an inverted reference voltage, which is required when the excitation voltage to the load cell is inverted. The AD7195 synchronizes the ac excitation with the conversions and performs the averaging. Only a few external components are required. Along with the MOSFET transistors, the only other external components required are some filters on the analog inputs and capacitors on the reference pins for EMC purposes.

The low level signal from the load cell is amplified by the AD7195 internal PGA. The PGA is programmed to operate with a gain of 128. The conversions from the AD7195 are then sent to the PC via the USB connector. Using LabView™ software, the conversions are converted to weight and displayed.

Figure 2 shows the actual test setup. A 6-wire load cell is used because this gives the optimum system performance. A 6-wire load cell has two sense pins in addition to the excitation, ground, and two output connections. The sense pins are connected to the high side and low side of the Wheatstone bridge. The voltage developed across the bridge can, therefore, be accurately measured regardless of the voltage drop due to the wiring resistance. In addition, the AD7195 has differential analog inputs, and it accepts a differential reference. Connection of the load cell differential SENSE lines to the AD7195 reference inputs creates a ratiometric configuration that is immune to low frequency changes in the power supply excitation voltage. In addition, it eliminates the need for a precision reference. With a 4-wire load cell, the sense pins are not present, and the ADC reference pins are connected to the excitation pins EXC+ and EXC-.



Figure 2. Weigh Scale System Setup Using the AD7195

With this arrangement, the system is not completely ratiometric because there is a voltage drop between the EXC+/EXC- pins and the SENSE+/SENSE- due to wiring resistance.

The AD7195 has separate analog and digital power supply pins. The analog section must be powered from 5 V. The digital power supply is independent of the analog power supply and can be any voltage between 2.7 V and 5.25 V.

The microcontroller uses a 3.3 V power supply. Therefore, DVDD is also powered from 3.3 V. This simplifies the interface between the ADC and microcontroller because no external level shifting is required.

There are several methods to power the weigh scale system. It can be powered from the main power supply bus or battery powered (as shown in Figure 1). A 5 V low noise regulator is used to ensure that the AD7195 and the load cell receive a low noise supply. The ADP3303 (5 V) is used to generate the 5 V supply and is a low noise regulator. The filter network shown inside the dotted box ensures a low noise AVDD for the system. In addition, noise reduction capacitors are placed on the regulator output as recommended in the ADP3303 (5 V) data sheet. To optimize the EMC performance, the regulator output is filtered ahead of the AD7195 and the load cell. The 3.3 V digital supply is generated using the ADP3303 (3.3 V). It is essential that low noise regulators be used to generate all the power supply voltages to the AD7195 and the load cell because any noise on the power supply or ground planes introduces noise into the system and degrades the circuit performance.

If a 2 kg load cell with a sensitivity of 2 mV/V is used, the full-scale signal from the load cell is 10 mV when the excitation voltage is 5 V. A load cell has an offset, or TARE, associated with it. The noise of the system is calculated by the software to be 10 nV rms and 51 nV peak-to-peak. This equates to 196,000

noise-free counts, or 17.5 bits of noise-free code resolution (calculated from the measured peak-to-peak noise). The TARE can have a magnitude that is up to 50% of the load cell full-scale output signal. The load cell also has a gain error that can be up to $\pm 20\%$ of full scale. Some customers use a DAC to remove or null the TARE. When the AD7195 uses a 5 V reference, its analog input range is equal to ± 40 mV when the gain is set to 128 and the part is configured for bipolar operation. The wide analog input range of the AD7195 relative to the load cell full-scale signal (10 mV) is beneficial because it ensures that the offset and gain error of the load cell do not overload the ADC's front end.

The AD7195 has an rms noise of 6 nV and a peak-to-peak noise of 40 nV when the first filter notch is programmed to 4.7 Hz. This corresponds to an output data rate of 1.17 Hz when ac excitation is used (sinc⁴ filter selected). The number of noise-free counts is equal to

$$\frac{10 \text{ mV}}{40 \text{ nV}} = 250,000 \quad (1)$$

The resolution in grams is, therefore, equal to

$$\frac{2 \text{ kg}}{250,000} = 0.008 \text{ g} \quad (2)$$

The noise free resolution is equal to

$$\log_2(250,000) = \frac{\log_{10}(250,000)}{\log_{10}(2)} = 17.9 \text{ bits} \quad (3)$$

In practice, the load cell itself introduces some noise. Figure 3 shows the measured output performance when a 1 kg weight is placed on the load cell and 500 conversions are gathered.

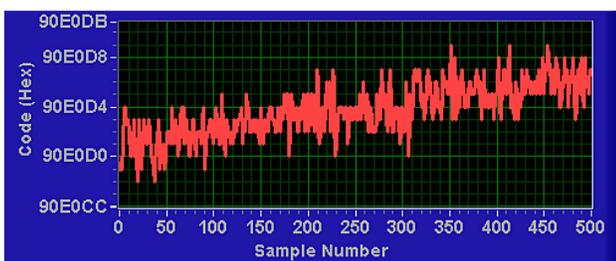


Figure 3. Measured Output Code for 500 Samples Showing the Effects of Noise

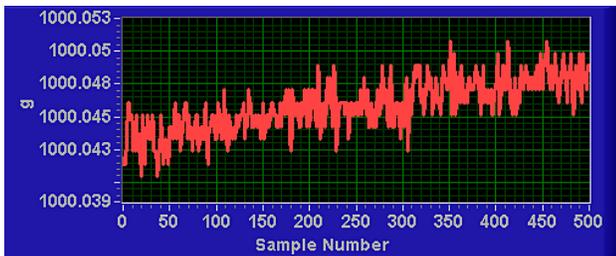


Figure 4. Measured Output in Grams for 500 Samples Showing the Effects of Noise

Figure 4 shows the performance in terms of weight. The peak-to-peak variation in output is 0.01 grams over the 500 codes. Therefore, the weigh scale system achieves an accuracy of 0.01 grams.

The plots show the actual (raw) conversions read back from the AD7195 when the load cell is attached. In practice, a digital post filter is used in a weigh scale system. The additional averaging that is performed in the post filter further improves the number of noise-free counts at the expense of a reduced output data rate.

As with any high accuracy circuit, proper layout, grounding, and decoupling techniques must be employed. See [Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND*](#), and [Tutorial MT-101, *Decoupling Techniques*](#), for more details.

A complete design support package for this circuit note can be found at <http://www.analog.com/CN0155-DesignSupport>.

COMMON VARIATIONS

Other weigh scale circuits, which do not require ac excitation, are described in the following Circuit Notes: [CN-0102](#), [CN-0107](#), [CN-0108](#), [CN-0118](#), and [CN-0119](#).

CIRCUIT EVALUATION AND TEST

With the exception of the external load cell and the PC, the circuit shown in Figure 1 is contained on the AD7195 evaluation board (EVAL-AD7195-EBZ).

Interface to the evaluation board is via a standard USB connector, J1. J1 is used to connect the evaluation board to the USB port of a PC. A standard USB connector cable is included with the AD7195 evaluation board to allow the evaluation board to interface with the USB port of the PC. The AD7195 evaluation board can be powered using a 9 V battery, B1, or using an external 9 V dc source connected at J31. The 9 V is regulated down to 5 V using the on-board [ADP3303-5](#), a high precision, low power 5 V output regulator. Using link J1, this regulated 5 V can be used as the supply to the AD7195. To use this option, link J1 should be placed in the 5 VBAT position.

Equipment Needed

The EVAL-AD7195-EBZ evaluation board and a PC running Windows® 2000, Windows XP, or Windows Vista (32-bit) are the only items required other than the external load cell. A Tedea Huntleigh 505H-0002-F070 load cell was used to obtain the results presented in this circuit note. The load cell is not shipped with the evaluation board and must be purchased from the manufacturer by the customer.

Getting Starting

The EVAL-AD7195-EBZ evaluation board is shipped with a CD containing software that can be installed onto a standard PC to control the AD7195. The software communicates with the AD7195 through the USB cable, which accompanies the board. The software allows conversion data to be read from the AD7195 and displayed or stored for later analysis.

The AD7195 evaluation board software should be installed using the supplied AD7195 evaluation board CD before connecting the board to the PC. Complete details can be found in the AD7195 evaluation board user guide (see the CN0155 Design Support Package: <http://www.analog.com/CN0155-DesignSupport>).

Functional Block

The evaluation board user guide shows the basic functional block diagram of the test setup (see the CN0155 Design Support Package: <http://www.analog.com/CN0155-DesignSupport>).

Setup and Test

Complete instructions for setup and testing of the AD7195 evaluation board can be found in AD7195 evaluation board user guide (see the CN0155 Design Support Package: <http://www.analog.com/CN0155-DesignSupport>).

After the software is installed, the AD7195 evaluation board should be configured for use with the external load cell by setting the appropriate links (jumpers) as described in the AD7195 evaluation board user guide (see the CN0155 Design Support Package: <http://www.analog.com/CN0155-DesignSupport>). Make sure the links are set before applying power to the evaluation board.

The load cell connects to the evaluation board header J4. Operation of the Weighscale Demo is described in the AD7195 evaluation board user guide (see the CN0155 Design Support Package: <http://www.analog.com/CN0155-DesignSupport>).

LEARN MORE

CN0155 Design Support Package:

<http://www.analog.com/CN0155-DesignSupport>

Kester, Walt. 1999. *Sensor Signal Conditioning*. Sections 2, 3, 4. Analog Devices.

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial, *ADC Architectures III: Sigma-Delta ADC Basics*, Analog Devices.

MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

[AD7195 Data Sheet](#)

[AD7195 Evaluation Board](#)

[ADP3303 Data Sheet](#)

REVISION HISTORY**11/10—Rev. 0 to Rev. A**

Changes to Circuit Note Title	1
Added Evaluation and Design Support Section	1
Changes to Circuit Function and Benefits Section	1
Changes to Circuit Description Section	2
Added Circuit Evaluation and Test Section	3
Changes to Learn More Section	4

7/10—Revision 0: Initial Version

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