Minimize Radio Unit (RU) Size, Weight, Power, and Cost (SWaP-C)

- Low power 13 W, supports highest junction temperature (TJ), and simplifies thermal solutions.
- Save up to 20% RU weight through simplified filters. ZIF architecture is robust to interferes in colocated radios.
- Expanded DFE capabilities (DPD, CFR, CDUC, and CDDC) eliminate or reduce external FPGA need.

Maximize RU Flexibility, Accelerate Time to Market

- Common platform supports all sub-6 GHz bands and form factors (M-MIMO, small cell, macrocell) for worldwide 3G/4G/5G deployment.
- SoC is fully qualified, evaluated, and regression tested per use case, simplifying RU system qualification.
- Reduces RU cost and development time for band and power variant designs, while enabling complex multiband combinations in a single chip.

Enhance System Efficiency, Simplify PA/DPD Implementation

- Fully integrated novel charge trapping correction IP enables high efficiency wide bandwidth GaN power amplifiers (PAs).
- >50 pretested PAs in partnership with leading PA vendors to maximize system efficiency.
- User-programmable DPD solution, including functions that maintain PA stability in real-world operating conditions.

Common SoC Platform for:
- TDD and FDD applications
- 3G/4G/5G
- Small cell, macro, and massive MIMO designs

ADRV904x
ADI RadioVerse® SoC Series Drives 5G Radio Efficiency and Performance
Advanced 8T8R Radio System with 400 MHz iBW, Integrated Digital Front End (DFE)

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ADRV904x Platform Functionality and Features

Simplifying System Thermal Solution

- 13 W power consumption for all blocks enabled¹
- 110°C device junction temperature, with excursions to 125°C²

Fully Integrated DFE (DPD, CDUC, CDDC, CFR)³ Engine

- Dedicated DPD adaptation engine (DFE Arm Cortex-A55 quad core processor, LT-DPD block, enhanced algorithm) for PA linearization
- GaN PA support via h/ware accelerated, charge trapping correction algorithm
- CDUC/CDCC: Max 8 component carriers (CCs) per each transmit/receive channel
- Multistage CFR engine
- Supports JESD204B/JESD204C digital interface

Industry-Leading Radio Solution

- Eight differential transmitters (Tx) and receivers (Rx)
- Two observation receivers (ORx)
- Tunable range: 650 MHz to 6000 MHz
- 400 MHz iBW DPD performance
- Single-band and multiband (N × 2T2R/4T4R) capability
- Multichip phase synchronization for all LOs and baseband clocks
- Fully integrated fractional-N RF synthesizers
- Fully integrated clock synthesizer

ADRV9040 SoC Product Page

- For more information, visit analog.com/ADRV9040

¹ 200 MHz OBW/IBW use case with all blocks enabled.
² 110°C TJ based on continuous operation, 125°C TJ based on conditional operation.
³ See “Co-location in C-BAND - Strategies for reducing risk” article for more details.
⁴ Digital predistortion (DPD), crest factor reduction (CFR), carrier digital upconverters (CDUCs), and carrier digital downconverters (CDDCs).
⁵ Allows four individual band profiles within the 650 MHz to 6000 MHz tunable range, where the band profile defines the bandwidth of a channel. Particularly valuable in small cell platforms.