

**FEATURES**

- Eight differential transmitters (Tx)**
- Eight differential receivers (Rx)**
- Two observation receivers (ORx)**
- Single band and multiband (N x 2T2R/4T4R) capability**
  - 4 individual band profiles within tunable range<sup>1</sup>**
- Tunable range: 650 MHz to 6000 MHz**
- 400 MHz iBW DPD support**
  - GaN PA support via hardware accelerated, charge trapping correction algorithm**
- Simplifying system thermal solution**
  - 13 W power consumption for all blocks enabled<sup>2</sup>**
  - 110°C maximum junction temperature, with operation up to 125°C<sup>3</sup>**
- Fully integrated DFE (DPD, CDUC, CDDC, CFR) engine that eliminates FPGAs and halves SERDES lane rate**
  - DPD adaptation engine for power amplifier linearization**
  - CDUC/CDDC—maximum 8 component carriers (CCs) per each Tx/Rx channel**
  - Multistage CFR engine**
- Supports JESD204B/JESD204C digital interface**
- Multichip phase synchronization for all LOs and baseband clocks**
- Fully integrated fractional-N RF synthesizers**
- Fully integrated clock synthesizer**

**APPLICATIONS**

- 3G/4G/5G TDD/FDD small cell, massive MIMO and macro base stations**

**GENERAL DESCRIPTION**

The ADRV9040 is a highly integrated, system on chip (SoC) radio frequency (RF) agile transceiver with integrated digital front end (DFE). The SoC contains eight transmitters, two observation receivers for monitoring transmitter channels, eight receivers, integrated LO and clock synthesizers, and digital signal processing functions. The SoC meets the high radio performance and low power consumption demanded by cellular infrastructure applications including small cell basestation radios, macro 3G/4G/5G systems, and massive MIMO base stations.

The Rx and Tx signal paths use a zero-IF (ZIF) architecture that provides wide bandwidth with dynamic range suitable for contiguous and noncontiguous multicarrier base station applications. The ZIF architecture has the benefits of low power plus RF frequency and bandwidth agility. The lack of aliases and out-of-band images eliminates anti-aliasing and image filters.

This reduces both system size and cost, also making band independent solutions possible.

The device also includes two wide-bandwidth observation path receiver sub-systems for monitoring transmitter outputs. This SoC subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering. GPIOs that provide an array of digital control options are also integrated.

Multi-band capability is enabled by dual LO functionality, additional LO dividers and wideband operation. This allows 4 individual band profiles<sup>1</sup> within the tuneable range, thereby maximizing use case flexibility.

The SoC has fully integrated digital front end (DFE) functionality which includes carrier digital up/down conversion (CDUC and CDDC), crest factor reduction (CFR), digital pre-distortion (DPD), closed loop gain control (CLGC) and voltage standing wave ratio (VSWR) monitor.

The CDUC feature of the ADRV9040 filters and places individual component carriers within the band of interest. The CDDC feature, with its 8 parallel paths, processes each carrier individually before sending over the serial data interface.

The CDUC and CDDC reduce SERDES interface data rates in non-contiguous carrier configurations. This integration also reduces power compared to an equivalent FPGA based implementation.

The CFR engine of the ADRV9040 reduces the peak-to-average ratio of the input signal, enabling higher efficiency transmit line ups while reducing the processing load on baseband processors.

The SoC also contains a fully integrated DPD engine for use in power amplifier (PA) linearization. DPD enables high efficiency PAs, reducing the power consumption of base station radios and the number of SERDES lanes interfacing with baseband processors. The DPD engine incorporates a dedicated long-term DPD (LT-DPD) block which provides support for GaN PAs. The ADRV9040 tackles the charge trapping property of GaN PAs with its LT-DPD block; therefore, improving emissions and EVM. The SoC includes an ARM Cortex-A55 quad core processor to independently serve DPD, CLGC, and VSWR monitor features. The dedicated processor, together with the DPD engine, provides industry leading DPD performance.

**Rev. PrA**

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The serial data interface consists of eight serializer lanes and eight deserializer lanes. The interface supports both the JESD204B and JESD204C standards and both fixed and floating-point data formats are supported. The floating-point format allows internal automatic gain control (AGC) to be transparent to the baseband processor.

The ADRV9040 is powered directly from 0.8 V, 1.0 V, and 1.8 V regulators and is controlled via a standard SPI serial port. Comprehensive power-down modes are included to minimize power consumption in normal use. The device is packaged in a 27 mm × 20 mm, 736-ball grid array.

<sup>1</sup> Band profiles define bandwidth and aggregate sampling rate of a channel.

<sup>2</sup> Use case is TDD 200 MHz instantaneous bandwidth and 200 MHz occupied bandwidth, with all blocks (DPD, CFR, CDUC/CDDC) enabled.

<sup>3</sup> Operating lifetime impact at >110°C can be offset by operation at <110°C based on acceleration factors.

# FUNCTIONAL BLOCK DIAGRAM

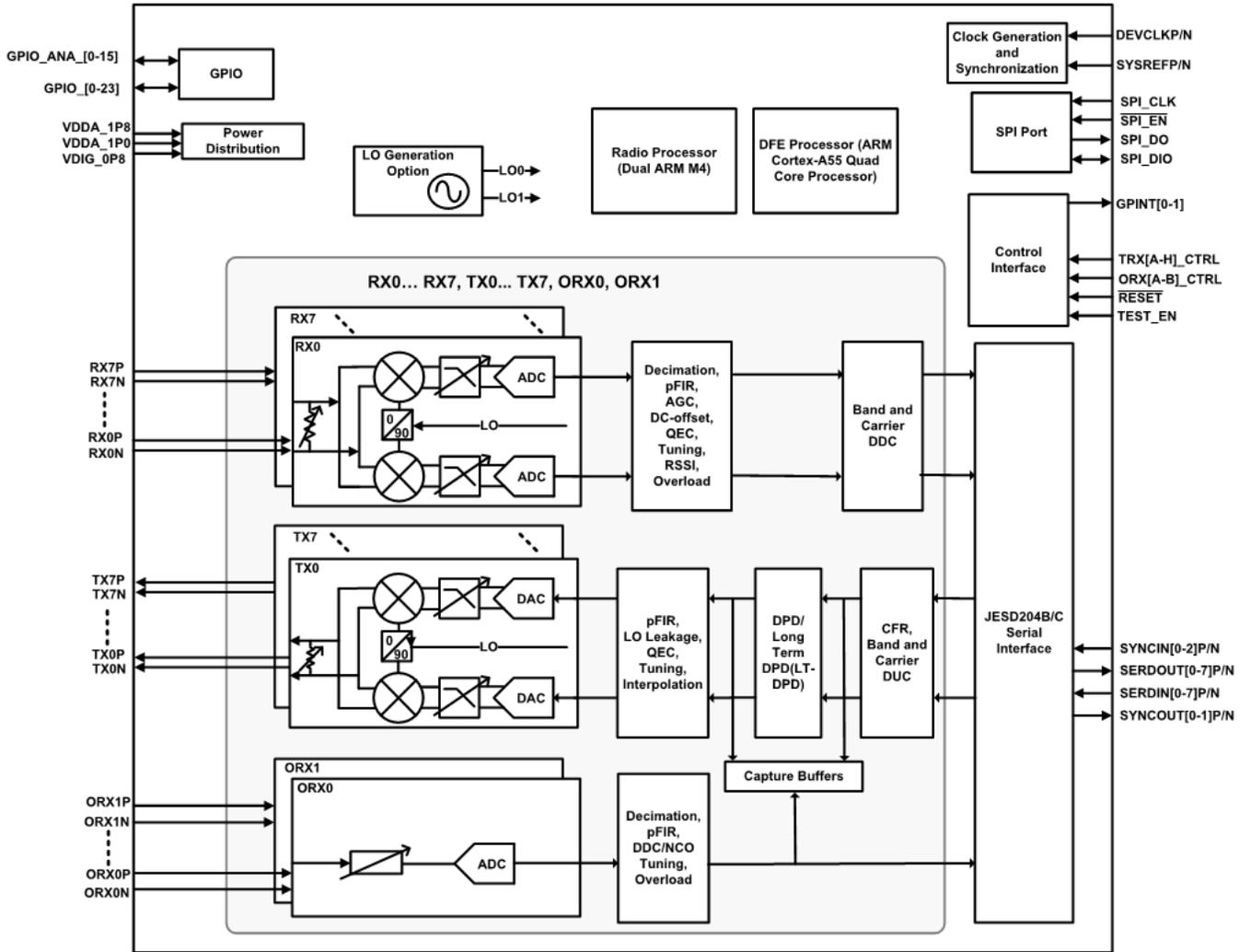


Figure 1.