ADRV9026/29 SOFTWARE RELEASE NOTES SW6.3.0.5

BUILD TYPE: **RELEASE**

RELEASE DATE: **FEBRUARY 28, 2022**

INCLUDED DELIVERABLES:

ARM Firmware Revision: **6.3.0.5**
Gain Tables Revision: **6.3.0.1**
API Revision: **6.3.0.5**
GUI Revision: **6.3.0.5**
(NOTE: Stream files must be generated from the GUI for the selected profile as they are use case dependent.)

PREVIOUS BUILD: **6.2.0.33**
(NOTE: This is the reference baseline for all changes outlined in this document.)

SUPPORTED USE CASES: **UC13-NLS, UC14-LS, UC14-NLS, UC14C-LS, UC26C-LS, UC26C-NLS, UC44-NLS, UC49-NLS, UC50-LS, UC50-NLS, UC51-LS, UC51-NLS, UC51C-LS, UC51C-NLS, UC54-NLS, UC55-NLS, UC59-LS, UC59-NLS, UC61-LS, UC78-NLS, UC83C-LS, UC90-NLS, UC93C-LS, UC93C-NLS, UC95C-LS, UC95C-NLS, UC98-LS, UC98-NLS, UC102-NLS (OTHER INCLUDED USE CASES HAVE NOT BEEN FULLY VERIFIED)**

INIT CALIBRATION:

The following calibrations were enabled during software verification for this release.

Init Calibration	Enabled	Init Calibration	Enabled	Init Calibration	Enabled	Init Calibration	Enabled
RESERVED		HD2 Init		Rx LO Delay		Loopback Rx DC Offset	X
RESERVED		RESERVED		Loopback Rx QEC Init		ORx DC Offset	X
CFR Init	X	Closed Loop Gain Control Init		Loopback Rx LO Delay	X	Rx DC Offset	X
RESERVED		DPD Init	X	Tx QEC Init	X	Loopback Rx TIA Filter	X
Rx Gain Phase	X	Tx DAC Init	X	Tx LO Leakage External Init	X	ORx TIA Filter	X
Rx Gain Delay	X	ORx QEC Init	X	Tx LO Leakage Init	X	Rx TIA Filter	X
Tx Atten Table Linearization	X	ORx LO Delay		Path Delay	X	ADC Tuner	X
Tx Atten Delay	X	Rx QEC Init	X	ADC Flash	X	Tx Baseband Filter	X

OVERVIEW

The SW6.3.0.5 RELEASE build provides updates in the ARM firmware, stream files, API, and GUI software to support ADRV9026/29. Changes outlined in this document are relative to the previous release build listed above. The updates included in this build are:

- Added support for new AGC functionality.
- Resolved several bugs related to DPD operation.

The following sections describe the changes and enhancements provided in this build.

API CHANGES

1. Added support for AGC Hybrid Mode by enabling GPIO configuration for agc_slowloop_freeze_enable on each Rx channel.
2. Added reset Sample PRBS error counter to the API function adi_adrv9025_DfrmPrbsCountReset().
3. Added a new API function adi_adrv9025_RxAgcSyncGpioPinSet to map Rx channels to a GPIO to enable the gain counter sync pulse feature, as such the Gain Update Counter gets synchronized with the rising edge of the pulse. This function should be used if agcEnableSyncPulseForGainCounter is set.
4. adi_adrv9025_OrxGainControlWithTxToOrxMappingGainGet API function is now deprecated.
5. Corrected an issue with the API function adi_adrv9025_GpioOeGet to return the proper argument type in the DLL.

ARM FIRMWARE CHANGES

Channel Setup

1. Resolved an error causing ACLR to degrade due to ORx QEC tracking cal. The FW was modified to prevent tracking on smaller signals and increase ORx QEC averaging when signal is present in both sidebands.
2. Added optimization of ADC coefficients over temperature for robust noise performance.

Applicable to ADRV9029 Only

1. Addressed an issue that caused DPD/QEC/CLGC calibration to not run on all four channels.
2. Resolved an API timeout issue when doing DPD reset command
3. Addressed an error where the DPD update count was incrementing without any DPD actuator updates.
4. Resolved an error that was causing timeout DPD reset command was being issued.

Calibrations

No changes

GUI CHANGES

No Changes

STREAM CHANGES

No changes

KNOWN ISSUES/LIMITATIONS

1. An additional step is required to deactivate the unused framer and deframer (in JESD page) to program certain JESD204C profiles successfully with the GUI.
2. External LO functionality is included in this release for debug quality (not for production systems). ADI only verified UC51 with for External LO operation. ADI will fully verify this operation in a future release.
3. UC13 and UC44 cannot support DPD
4. AUX LO operation is not supported for 2T4R profiles.
5. When a large tone appears near the RX/ORX band edge, ADI has occasionally observed reduced RX/ORX QEC performance.
6. RX/ORX QEC tracking convergence time may be impacted when a large tone is present near DC.
7. TX LOL can degrade with signals close to DC when using a 100 µs subframe duration.
8. TX LOL can degrade slightly when testing with CW signals at specific frequencies – no issue observed with modulated signals.
9. DPD Timeout issues have been observed when a DPD reset is asserted via adi_adrv9025_DpdReset() cmd with the DPD tracking calibration enabled. It is recommended to disable the DPD tracking calibration via TrackingCalsEnableSet() cmd and wait for 1 second to ensure that DPD has stopped tracking before proceeding to issue a DPD reset command.

ADDITIONAL INFORMATION

1. Profile generator is now supported with this build.
2. The API command ***adi_adrv9025_DpdModelConfigSet()*** supports programming a DPD model with a maximum of 190 coefficients primarily targeting 200MHz channel bandwidth DPD applications.
3. A user defined macro **ADI_ADRV9025_MAX_DPD_FEATURES** has been included in adi_adrv9025_user.h, which specifies the maximum no. of DPD coefficients supported. By default, **ADI_ADRV9025_MAX_DPD_FEATURES** is set to 190. This macro needs to be modified by the user.
4. The user should integrate ARM-D (ADRV9025_DPDCORE_FW.bin) along with the default ARM-C (ADRV9025_FW.bin) to ensure successful boot up. This is required even if not using ADI internal DPD.

5. The user is advised to optimize the LEMC/LMFC offset for the deframer to get the correct data and deterministic latency. The user can refer to SELECTING THE OPTIMAL LMFC/LEMC OFFSET FOR A ADRV902X DEFRAMER section in the user guide for detailed information on sweeping the LEMC/LMFC offset for ADRV902X.
6. ADI recommends setting ORx Attenuation to 10dB at higher LO frequencies, to take advantage of the LO leakage algorithm's rejection of coupling.
7. Tracking cals should be disabled prior to changing LO frequency.
8. Customers should add adi_adrv9025_PllLoopFilterSet in their startup sequence immediately before adi_adrv9025_PostMcsInit to set the loop filter bandwidth to 600 kHz.
9. It is recommended that customers run the external TX LOL init calibration. When running init calibrations, be sure to disable all tracking calibrations.

SUPPORTED USE CASES

This following use cases are included in this GUI revision but have not been verified. For a list of verified use cases, see the Supported Use Cases list on page 1 of this document.

Use Case	Np Value		Tx Channels			ORx Channels			Rx Channels			JESD Lane Rate (Gpbs)
	Tx	Rx/ Orx	BW (MHz)	Data Rate (MSPS)	Channels	BW (MHz)	Data Rate (MSPS)	Channels	BW (MHz)	Data Rate (MSPS)	Channels	
13-NLS	16	16	100/225	245.76	4	225	245.76	2	100	122.88	4	9.8304
14-LS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	14.7
14-NLS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	14.7
14C-LS[5]	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	24.3302
20-NLS	16	16	125/250	307.2	4	281.2	307.2	2	125	153.6	4	12.288
23C-LS[5]	16	16	150/300	368.64	4	300	368.64	2	150	184.32	4	24.3302
26C-LS[5]	16	16	200/450	491.52	4	450	491.52	2	200	245.76	4	16.2202
26C-NLS[5]	16	16	200/450	491.52	4	450	491.52	2	200	245.76	4	16.2202
44-NLS[1,3,4]	16	16	40/225	61.44	4	225	245.76	1	20	61.44	4	9.8304
49-NLS[1,2]	16	16	200/450	245.76	4	450	491.52	2	100	122.88	4	9.8304
50-LS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	100	122.88	4	9.8304
50-NLS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	100	122.88	4	9.8304
51-LS[1,3,4]	16	16	200/450	245.76	4	450	245.76	2	200	245.76	4	9.8304
51C-LS[1,3,4,5]	16	16	200/450	245.76	4	450	245.76	2	200	245.76	4	16.2202
51C-LS-Np12[1,3,4]	12	12	200/450	245.76	4	450	245.76	2	200	245.76	4	12.165
51-NLS[1,3,4]	16	16	200/450	245.76	4	450	245.76	2	200	245.76	4	9.8304
51C-NLS[1,3,4,5]	16	16	200/450	245.76	4	450	245.76	2	200	245.76	4	16.2202
51C-NLS-Np12[1,3,4]	12	12	200/450	245.76	4	450	245.76	2	200	245.76	4	12.165
54-NLS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	200	122.88	4	9.8304
55-NLS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	160	122.88	4	9.8304
59-NLS[1,2]	16	16	200/450	250	4	450	250	2	200	250	4	10
59-LS[1,2]	16	16	200/450	250	4	450	250	2	200	250	4	10
61-LS	12	12	200/300	368.64	4	300	368.64	2	200	368.64	4	11.0592
78-LS[1,3,4]	16	16	100/281	153.6	4	281	307.2	2	125	153.6	4	6.144
78-NLS[1,3,4]	16	16	100/281	153.6	4	281	307.2	2	125	153.6	4	6.144
82C-LS[5]	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	24.3302
83C-LS[5]	16	16	200/337	368.64	4	337	368.64	2	200	368.64	4	24.3302
90-LS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	100	122.88	4	4.9152
90-NLS[1,2,4]	16	16	200/450	122.88	4	450	245.76	2	100	122.88	4	4.9152
93C-LS*[5]	12	24	200/450	491.52	4	450	491.52	2	300	245.76	4	24.3302
93C-NLS*[5]	12	24	200/450	491.52	4	450	491.52	2	300	245.76	4	24.3302
95C-LS*[5]	16	16	200/450	491.52	4	450	491.52	2	300	245.76	4	16.2202
95C-NLS*[5]	16	16	200/450	491.52	4	450	491.52	2	300	245.76	4	16.2202
98-LS*	12	12	200/450	491.52	4	450	491.52	2	300	245.76	4	14.7
98-NLS*	12	12	200/450	491.52	4	450	491.52	2	300	245.76	4	14.7
102-NLS[1,2,4S]	16	16	200/330	245.76	4	450	245.76	2	200	245.76	4	9.8304

Notes: LS = Link Sharing; NLS = Non-Link Sharing

[1] DPD specific profile

[2] Internal DPD actuator rate is 491.52 MSPS (DPD HB enabled)

[3] Internal DPD actuator rate is 983.04 MSPS (DPD HB enabled)

[4] DPD x4 HB enabled

[5] Only supported on B silicon

Additional Note: Other use cases not included in the above table may be present in the build package – these use cases have not been verified by ADI and there is no guarantee of operation/performance.

* These profiles exceed the datasheet maximum bandwidth specification and therefore may not meet all datasheet performance specs.