ADRV9026 SOFTWARE RELEASE NOTES SW5.0.0.47

BUILD TYPE: **DEBUG**

(NOTE: This release is not a Production Release and shall not be used in field trials, demonstrations, or in commercially released applications.)

RELEASE DATE: **AUGUST 10, 2020**

INCLUDED DELIVERABLES:

ARM Firmware Revision: **5.0.0.22**
Gain Tables Revision: **5.0.0.1**
API Revision: **5.0.0.40**
GUI Revision: **5.0.0.51**
(NOTE: Stream files must be generated from the GUI for the selected profile as they are use case dependent.)

PREVIOUS BUILD: **4.2.0.11**
(NOTE: This is the reference baseline for all changes outlined in this document.)

SUPPORTED USE CASES: **UC14C-LS, UC26C-LS, UC26C-NLS, UC93C-LS, UC93C-NLS, UC95C-LS, UC95C-NLS, UC83C-LS (OTHER INCLUDED USE CASES HAVE NOT BEEN FULLY VERIFIED)**

INIT CALIBRATION:

The following calibrations were enabled during software verification for this release.

Init Calibration	Enabled	Init Calibration	Enabled	Init Calibration	Enabled	Init Calibration	Enabled
RESERVED		HD2 Init		Rx LO Delay		Loopback Rx DC Offset	X
RESERVED		VSWR Init		Loopback Rx QEC Init		ORx DC Offset	X
CFR Init		Closed Loop Gain Control Init		Loopback Rx LO Delay	X	Rx DC Offset	X
RESERVED		DPD Init		Tx QEC Init	X	Loopback Rx TIA Filter	X
Rx Gain Phase	X	Tx DAC Init	X	Tx LO Leakage External Init	X	ORx TIA Filter	X
Rx Gain Delay	X	ORx QEC Init	X	Tx LO Leakage Init	X	Rx TIA Filter	X
Tx Atten Table Linearization	X	ORx LO Delay		Path Delay	X	ADC Tuner	X
Tx Atten Delay	X	Rx QEC Init	X	ADC Flash	X	Tx Baseband Filter	X

OVERVIEW

The SW5.0.0.47 DEBUG build provides updates in the ARM firmware, stream files, API, and GUI software to support ADRV9025. Changes outlined in this document are relative to the previous release build listed above. The updates included in this build are:

- Adding ADRV9026 support for additional use cases with SERDES lane rates at 25G and 16G.

The following sections describe the changes and enhancements provided in this build.

API CHANGES

1. Added new API to enable sysref timing debug. The API uses both clock and 9025 device which is contained in adi_device_share.c. adi_device_share_setupHoldMonitorTimingBlock returns two arrays of hold and setup words which can be used to tell if sysref is meeting timing requirements with respect to device clock for a given coarse or fine clock adjustment.
2. Added new API adi_adrv9025_GenerateEyeDiagramQRMode which can be used to generate multi-level eye diagram on ADRV9025 for profiles that have lane rate greater than 16 Gbps (i.e. quarter rate profiles).
3. Added support for 2T2R. Use cases: UC51-NLS, UC90-NLS and UC59-LS now support 2T2R configurations.
4. Implemented new main.c for ADRV9025. The new main.c will program the platform directly, not using any board level APIs. After the main is executed, a command line menu will be presented to the user, which will give the following options –
    a. Initialization
    b. Get Rx & Tx Channels
    c. Set Rx & Tx Channels
    d. Exit

    This is aimed at giving the customer the knowledge of how the programming sequence works and how to use our API functions.

ARM FIRMWARE CHANGES

Channel Setup

1. Added ARM FW support for changing the Rx LO during runtime.
2. Disabled the ARM watchdog before MCS and enable it again when MCS done to prevent spurious watchdog timeouts.
3. Resolved a bug to prevent ARM-C from locking up if ARM-D becomes unresponsive.

Calibrations

1. Modified the FW so that the RF ORx DC offset cal is always enabled.

GUI CHANGES

1. Fixed a bug with ORx3 Select Pin assignment for Madura. This was enabling incorrect Stream Options.

STREAM CHANGES

1. Modified the stream so that the RF ORx DC offset cal is always enabled.

KNOWN ISSUES/LIMITATIONS

1. Slightly degraded Tx QEC calibration performance was seen for Tx3 channel. This is currently being investigated.
2. When a large tone appears near the RX/ORX band edge, ADI has occasionally observed reduced RX/ORX QEC performance.
3. RX/ORX QEC tracking convergence time may be impacted when a large tone is present near DC.
4. TX LOL can degrade with signals close to DC when using a 100 µs subframe duration.
5. TX LOL can degrade slightly when testing with CW signals at specific frequencies – no issue observed with modulated signals.

ADDITIONAL INFORMATION

1. The user should integrate ARM-D (ADRV9025_DPDCORE_FW.bin) along with the default ARM-C (ADRV9025_FW.bin) to ensure successful boot up. This is required even if not using ADI internal DPD.
2. The user might is advised to optimize the LEMC/LMFC offset for the deframer to get the correct data and deterministic latency. The user can refer to SELECTING THE OPTIMAL LMFC/LEMC OFFSET FOR A ADRV902X DEFRAMER section in the user guide for detailed information on sweeping the LEMC/LMFC offset for ADRV902X.
3. ADI recommends setting ORx Attenuation to 10dB at higher LO frequencies, to take advantage of the LO leakage algorithm's rejection of coupling.
4. Tracking cals should be disabled prior to changing LO frequency.
5. Customers should add adi_adrv9025_PllLoopFilterSet in their startup sequence immediately before adi_adrv9025_PostMcsInit to set the loop filter bandwidth to 600 kHz.
6. It is recommended that customers run the external TX LOL init calibration. When running init calibrations, be sure to disable all tracking calibrations.

SUPPORTED USE CASES

This following use cases are included in this GUI revision but have not been verified. For a list of verified use cases, see the Supported Use Cases list on page 1 of this document.

Use Case	Np Value		Tx Channels			ORx Channels			Rx Channels			JESD Lane Rate (Gpbs)
	Tx	Rx/ Orx	BW (MHz)	Data Rate (MSPS)	Channels	BW (MHz)	Data Rate (MSPS)	Channels	BW (MHz)	Data Rate (MSPS)	Channels	
13-NLS	16	16	100/225	245.76	4	225	245.76	2	100	122.88	4	9.8304
14-LS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	14.7
14-NLS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	14.7
14C-LS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	24.3302
14C-NLS	12	12	200/450	491.52	4	450	491.52	2	200	245.76	4	24.3302
26C-LS	16	16	200/450	491.52	4	450	491.52	2	200	245.76	4	16.2202
26C-NLS	16	16	200/450	491.52	4	450	491.52	2	200	245.76	4	16.2202
61-LS	12	12	200/300	368.64	4	300	368.64	2	200	368.64	4	11.0592
83C-LS	16	16	200/337	368.64	4	337	368.64	2	200	368.64	4	24.3302
93C-LS	12	24	200/450	491.52	4	450	491.52	2	300	245.76	4	24.3302
93C-NLS	12	24	200/450	491.52	4	450	491.52	2	300	245.76	4	24.3302
95C-LS	16	16	200/450	491.52	4	450	491.52	2	300	245.76	4	16.2202
95C-NLS	16	16	200/450	491.52	4	450	491.52	2	300	245.76	4	16.2202

Notes: LS = Link Sharing; NLS = Non Link Sharing