# ADRV9026/29 SOFTWARE RELEASE NOTES SW6.2.0.33

**BUILD TYPE:** **RELEASE**

**RELEASE DATE:** **OCTOBER 27, 2021**

**INCLUDED DELIVERABLES:**

**ARM Firmware Revision:** **6.2.0.13**
**Gain Tables Revision:** **6.2.0.1**
**API Revision:** **6.2.0.19**
**GUI Revision:** **6.2.0.36**
**(NOTE: Stream files must be generated from the GUI for the selected profile as they are use case dependent.)**

**PREVIOUS BUILD:** **5.1.0.27**
**(NOTE: This is the reference baseline for all changes outlined in this document.)**

**SUPPORTED USE CASES:** **UC13-NLS, UC14-LS, UC14-NLS, UC14C-LS, UC26C-LS, UC26C-NLS, UC44-NLS, UC49-NLS, UC50-LS, UC50-NLS, UC51-LS, UC51-NLS, UC51C-LS, UC51C-NLS, UC54-NLS, UC55-NLS, UC59-LS, UC59-NLS, UC61-LS, UC78-NLS, UC83C-LS, UC90-NLS, UC93C-LS, UC93C-NLS, UC95C-LS, UC95C-NLS, UC98-LS, UC98-NLS (OTHER INCLUDED USE CASES HAVE NOT BEEN FULLY VERIFIED)**

**INIT CALIBRATION:**

The following calibrations were enabled during software verification for this release.

| Init Calibration | Enabled | Init Calibration | Enabled | Init Calibration | Enabled | Init Calibration | Enabled |
|---|---|---|---|---|---|---|---|
| RESERVED | | RESERVED | | RESERVED | | Loopback Rx DC Offset | X |
| RESERVED | | RESERVED | | RESERVED | | ORx DC Offset | X |
| CFR Init | X | RESERVED | | Loopback Rx LO Delay | X | Rx DC Offset | X |
| RESERVED | | DPD Init | X | Tx QEC Init | X | Loopback Rx TIA Filter | X |
| Rx Gain Phase | X | Tx DAC Init | X | Tx LO Leakage External Init | X | ORx TIA Filter | X |
| Rx Gain Delay | X | ORx QEC Init | X | Tx LO Leakage Init | X | Rx TIA Filter | X |
| Tx Atten Table Linearization | X | RESERVED | | Path Delay | X | ADC Tuner | X |
| Tx Atten Delay | X | Rx QEC Init | X | ADC Flash | X | Tx Baseband Filter | X |

## OVERVIEW

The SW6.2.0.33 RELEASE build provides updates in the ARM firmware, stream files, API, and GUI software to support ADRV9026/29. Changes outlined in this document are relative to the previous release build listed above. The updates included in this build are:

- Added profile generator support to support generation of different user defined use cases.
- Added enhanced features for DPD support for ADRV9029.

The following sections describe the changes and enhancements provided in this build.

## API CHANGES

1. ADI_ADRV9025_TRACKINGCAL_SYNC_BASE_CAL_ABORT enum was added to adi_adrv9025_TrackingCalSyncStatus_e data structure to report if the base cal is aborted.
2. Updated the API to correct minimum and maximum Tx, Rx and ORx bandwidths that can be supported by ADRV9025.
3. Updated the initdata.c file to add an offset to resolve any mismatch with API.
4. Added check to identify if any CPU exception has occurred.
5. Modified the adi_adrv9025_SerializerReset API function to readback the bitfield after call BfSet to ensure the reset bit was set correctly. It also verifies that the bit clears after the BfSet to clear is called.
6. Added a new macro ADI_ADRV9025_HW_RMW_ENABLE in adi_adrv9025_user.h through which the hardware based read-modify-write on the ADRV9025 device can optionally be disabled. By default it is enabled (same as earlier software versions) and the users are recommended NOT to modify this macro.
7. Optimized all the ADC profiles specific for use cases having ADC rates in between 2-3GHz.
8. Update for adi_adrv9025_CpuCmdStatusOpcodeGet to check the correct bits for Stream opcode.
9. Added code to generate RxAdc profiles with the given Sampling frequency and bandwidth.
10. Corrected the GpioOeGet function in the DLL side to include the correct data type.

### *Applicable to ADRV9029 Only*

11. Added a change to CLGC operation to stop CLGC updates during the occurrence of PA protection/Tx Ramp down events.
12. Updated documentation for several DPD related enums and their corresponding values to reflect intended usage more accurately. This impacted Enums as follows –
    a. adi_adrv9025_DpdTrackingUpdateMode_e
    b. adi_adrv9025_DpdModelTableSel_e
    c. adi_adrv9025_DpdRecoveryAction_e
    d. adi_adrv9025_DpdMetric_e
    e. adi_adrv9025_DpdErrorState_e
    f. adi_adrv9025_CfrModeSel_e
    g. adi_adrv9025_ClgcRunState_e
    h. adi_adrv9025_dpdSamplesPerCapture_e
    i. adi_adrv9025_DpdStatistics_t
    j. adi_adrv9025_DpdStatus_t
    k. adi_adrv9025_DpdTrackingConfig_t
    l. adi_adrv9025_EnhancedDpdTrackingConfig_t
13. Added changes to adi_adrv9025_dpdModelConfigSet structure to optimize DPD model loading time.
14. Added new API interfaces for DPD Wideband Regularization feature. This includes two new control settings for wideband regularization
    - adi_adrv9025_EnhancedDpdTrackingConfigSet.enableWidebandRegularization for wideband regularization enable/disable control programmable through the API adi_adrv9025_EnhancedDpdTrackingConfigSet( ).
    - adi_adrv9025_EnhancedDpdTrackingConfigGet.widebandRegularizationFactor to configure the weighting factor β for wideband regularization programmable through the API adi_adrv9025_EnhancedDpdTrackingConfigSet( ).
    - A new API adi_adrv9025_EnhancedDpdWidebandRegularizationConfigSet() has been added through which the user can program 1024 sample complex wideband regularization data.
15. Added a new function (adi_adrv9025_EnhancedDpdWidebandRegularizationConfigSet) to pass customer waveform data to FW for eDPD feature, wideband regularization.
16. TDD LUT switch interface changed between FW and API, change API code.
    - Added 2 members to the adi_adrv9025_DpdResetMode_e:
      i. ADI_ADRV9025_DPD_LUT_RESTORE_R_TABLE = 6, /*!< Restores DPD LUT R Table */
      ii. ADI_ADRV9025_DPD_COEFF_SAVE_R_TABLE = 7 /*!< Save off DPD Coefficients R Table */
    - Added 3 new members to adi_adrv9025_EnhancedDpdTrackingConfig_t:
      i. uint16_t tddLutSwitchModelADelay[ADI_ADRV9025_MAX_TDD_LUT_MODELA_DELAY]; /*!< TDD LUT switch Model A delay array, value unit: us */
      ii. uint16_t tddLutSwitchModelBDelay; /*!< TDD LUT switch Model B delay value, unit: us */
      iii. uint8_t enableTddLutSwitch; /*!< TDD LUT switch feature enable, (0: enable, 1: disable) */
17. Added new AP function to enable enhanced DPD (eDPD) feature to ADRV9025 as part of adi_adrv9025_EnhancedDpdTrackingConfig_t –

- adi_adrv9025_EnhancedDpdTrackingConfigSet
- adi_adrv9025_EnhancedDpdTrackingConfigGet

## ARM FIRMWARE CHANGES

### *Channel Setup*

1. The ORxQEC calibration was updated to prevent rapidly occurring overload signals in the Receiver HW from causing timing problems within the processor. This was causing extended ARM response times leading to timeout errors.
2. Added changes to use the current Tx attenuation setting while running the path delay init cal.
3. Added a FW update to include facility for supporting pseudo link sharing profiles.
4. Resolved an issue which was causing the API to report an incorrect build type.
5. Added ability to use the ARM SRL error bit to extend the GP INT until after PA protection Tx recovery ramp is complete.
6. Added changes to avoid any precision loss when calculating Rx NCO Frequency Tuning Word from desired frequency offset.
7. Added FW support to enable broadcast of ADC Profiles to multiple devices.
8. Corrected a boot up issue while using UC61 profile.
9. Resolved an error that was causing the Tx NCO set and get values to not match.
10. Optimized the FW to improve robustness of PLL operation.
11. Resolved an issue that was causing the fractional path delay filters to produce incorrect delays.
12. Added ability to support Rx datapath at 491.52Msps.
13. A more accurate temperature is reported by the FW based on a factory calibrated fused temperature offset.
14. Updated FW to clear and then set the efuse read_start bit before every efuse read.
15. Removed some test FW code to optimize the FW code size.
16. Updated the FW fix to make sure that a cal is properly terminated before exit.

### *Applicable to ADRV9029 Only*

17. Added TDD LUT switching feature in ADRV9025.
18. Resolved a timeout issue when DPD reset command or clgcStatusGet function was being run.
19. Addressed an issue that was causing the R-Table to not be read after full reset.
20. Resolved an error causing CLGC and DPD tracking to report an error when PA protection event is triggered.
21. Added Enhanced DPD (eDPD) algorithm to improve ACLR and EVM requirements for GaN PA.
22. Firmware implementation of DPD wideband regularization algorithm.
23. Expanded the extended peak capture for DPD multi-model. It requires customer to trigger every capture via GPIO within extended peak search window.
24. Added a new command DPD_CTRL_UPDATE_BANK to resolve an issue with swapping Multi-model LUTs in Tx_EN static low mode.
25. In External DP multi-model mode, the ARM updates LUTs while TX is low to avoid any impact of transmitted data. However, after TX goes high it takes a window of time for the ARM to stop updating. This window has been decreased from ~20us to ~2us.
26. Resolved a health monitor timeout error when issuing the DPD reset command.

### *Calibrations*

1. Resolved an issue with calculation of the Tx NCO frequency causing Tx QEC calibration to fail.
2. Updated the Tx LOL algorithm for optimized performance.
3. Modified the Tx LOL tracking calibration to not updated if saturation is detected and avoid adding a bad LOL correction.
4. During the rare situation that the LOL hardware "square" accumulators overflow or saturate, then avoid using the LOL capture data from that track.
5. Due to correlator issues with accumulating auto and cross correlation terms, modified the TxQEC tracking code to handle the accumulations.
6. For TxLOL's capture of narrow band bursts, added logic to process the burst if the cal is paused before the task gets the notification to process the data. For certain TDD timing, this improves the capture time by < 1 ms.
7. Fixed a rare race condition where TxQEC tracking might not detect tracking disable if starting a data capture at the same time.
8. The new pathdelay fractional filter changes was leaving the correlator configured with the wrong number of filter taps when running TxQEC. This was causing TxQEC tracking to sometimes go unstable or fail to converge.
9. Updated the LO delay algorithm to increase the correction range to support the 6.2GHz

***Applicable to ADRV9029 Only***

10. Added a fix to address the issue where the CLGC error status specified by the API data structure parameter adi_adrv9025_ClgcStatus_t.clgcTrackingCalStatus.errorCode was toggling between no error and the error status intermittently.
11. Added ability to disable update of CLGC calibration on occurrence of PA protection/Tx ramp down events.
12. Added logic in CLGC tracking to properly handle correlator registers following a tracking pause.
13. Resolved an issue in the Tx observation path (for profiles using DPD actuator at 983.04Msps) set up causing inaccurate loop gain estimations for CLGC.
14. Resolved an error causing CLGC timeout when ClgcConfigSet function was called.

## GUI CHANGES

1. Added profile generator support to support generation of different user defined use cases.
2. Resolved minor bugs in JESD calculation and set up in the GUI JESD page.
3. Resolved an issue with setting the extLoFreqN field in the GUI initialization page.
4. Addressed minor bugs in generation of init files in demo mode.
5. Resolved an error to disable unused deframer 1 correctly. This was causing UC49 profile to not program while using the GUI.
6. Added ability to integrate user special profile generated functions.
7. Resolved the following GUI issues –
    a. Fixed GUI not appearing on some machines.
    b. Fixed GUI panel collapsing problems.
    c. Fixed ACLR config window's "Flexible" mode not working.

***Applicable to ADRV9029 Only***

8. Implemented enhanced DPD for ADRV9025 in GUI. Added new enhanced DPD tracking configuration parameters.

## STREAM CHANGES

1. The ORx high stream was changed slightly alter the TIA power up sequence - this improves TIA robustness over temperature.
2. Added new stream tag "SwitchXbarOnRxLow" to allow customer to do ADC XBar control using ORx or Rx.
3. Resolved an error where the core stream processor interrupted the ARM when GP INT goes high. This was causing the GP INT to remain at high until any PA protection related recovery ramp is complete. This can be enabled by setting the stream tag “DeframerErrorRampControl”.

***Applicable to ADRV9029 Only***

4. Added an optional feature to disable External Timer stream before starting a DPD capture, to reduce jitter in starting the capture. The external timer stream will be disabled when the Capture GPIO goes low, and GPIO high will trigger a capture and restart the stream. The time between falling edge and rising edge must be within 6 - 10us. This feature must be explicitly enabled when generating the stream binary with {stopExtTimerForDpdCap:true}
5. Added stream changes to support TDD LUT switch features while using GaN power amplifiers.

## KNOWN ISSUES/LIMITATIONS

1. eDPD was found to be unstable while using waveform with sparse signal content (for example – TM2 waveform).
2. UC13 cannot support DPD
3. Slightly degraded Tx QEC calibration performance was seen for Tx3 channel. This is currently being investigated.
4. When a large tone appears near the RX/ORX band edge, ADI has occasionally observed reduced RX/ORX QEC performance.
5. RX/ORX QEC tracking convergence time may be impacted when a large tone is present near DC.
6. TX LOL can degrade with signals close to DC when using a 100 µs subframe duration.
7. TX LOL can degrade slightly when testing with CW signals at specific frequencies – no issue observed with modulated signals.
8. DPD Timeout issues have been observed when a DPD reset is asserted via adi_adrv9025_DpdReset() cmd with the DPD tracking calibration enabled. It is recommended to disable the DPD tracking calibration via TrackingCalsEnableSet() cmd and wait for 1 second to ensure that DPD has stopped tracking before proceeding to issue a DPD reset command.

## ADDITIONAL INFORMATION

1. For the wideband regularization feature, the recommended default value for the weighting factor **adi_adrv9025_EnhancedDpdTrackingConfigGet.widebandRegularizationFactor** is 1e-4. The user can tune this value further depending on the PA characteristics.

2. The 1024 sample calibration signal for wideband regularization programmed via **adi_adrv9025_EnhancedDpdWidebandRegularizationConfigSet()** API should be a copy of the full power wideband Tx waveform to be used in the application. The recommended method to generate this waveform is documented below
    a. Program the device with the required use case
    b. Transmit a full power full bandwidth signal (Eg: NR100, TM3.1a, -14dBFS rms for the 100MHz channel BW case)
    c. Enable CFR, DPD tracking through the usual procedure
    d. Allow ACLR to settle.
    e. Disable DPD tracking
    f. Dump the DPD capture buffers. Please contact ADI for scripts to dump the DPD capture buffers.
    g. Grab the first 1024 samples of the pre-DPD actuator buffer data from step 6 for use with wideband regularization.
    h. While enabling wideband regularization, use the 1024 samples saved from Step 7 as the input to **adi_adrv9025_EnahcedDpdWidebandRegularizationConfigSet()** API.
3. The API command ***adi_adrv9025_DpdModelConfigSet()*** supports programming a DPD model with a maximum of 190 coefficients primarily targeting 200MHz channel bandwidth DPD applications.
4. A user defined macro **ADI_ADRV9025_MAX_DPD_FEATURES** has been included in adi_adrv9025_user.h, which specifies the maximum no. of DPD coefficients supported. By default, **ADI_ADRV9025_MAX_DPD_FEATURES** is set to 190. This macro needs to be modified by the user.
5. The user should integrate ARM-D (ADRV9025_DPDCORE_FW.bin) along with the default ARM-C (ADRV9025_FW.bin) to ensure successful boot up. This is required even if not using ADI internal DPD. Please note that DPD is not supported in this release.
6. The user is advised to optimize the LEMC/LMFC offset for the deframer to get the correct data and deterministic latency. The user can refer to SELECTING THE OPTIMAL LMFC/LEMC OFFSET FOR A ADRV902X DEFRAMER section in the user guide for detailed information on sweeping the LEMC/LMFC offset for ADRV902X.
7. ADI recommends setting ORx Attenuation to 10dB at higher LO frequencies, to take advantage of the LO leakage algorithm's rejection of coupling.
8. Tracking cals should be disabled prior to changing LO frequency.
9. Customers should add adi_adrv9025_PllLoopFilterSet in their startup sequence immediately before adi_adrv9025_PostMcsInit to set the loop filter bandwidth to 600 kHz.
10. It is recommended that customers run the external TX LOL init calibration. When running init calibrations, be sure to disable all tracking calibrations.

## SUPPORTED USE CASES

This following use cases are included in this GUI revision but have not been verified. For a list of verified use cases, see the Supported Use Cases list on page 1 of this document.

| Use Case | Np Value | | Tx Channels | | | ORx Channels | | | Rx Channels | | | JESD Lane Rate (Gpbs) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Tx | Rx/ Orx | BW (MHz) | Data Rate (MSPS) | Channels | BW (MHz) | Data Rate (MSPS) | Channels | BW (MHz) | Data Rate (MSPS) | Channels | |
| 13-NLS | 16 | 16 | 100/225 | 245.76 | 4 | 225 | 245.76 | 2 | 100 | 122.88 | 4 | 9.8304 |
| 14-LS | 12 | 12 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 200 | 245.76 | 4 | 14.7 |
| 14-NLS | 12 | 12 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 200 | 245.76 | 4 | 14.7 |
| 14C-LS[5] | 12 | 12 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 200 | 245.76 | 4 | 24.3302 |
| 26C-LS[5] | 16 | 16 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 200 | 245.76 | 4 | 16.2202 |
| 26C-NLS[5] | 16 | 16 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 200 | 245.76 | 4 | 16.2202 |
| 44-NLS[1,3,4] | 16 | 16 | 40/225 | 61.44 | 4 | 225 | 245.76 | 2 | 20 | 61.44 | 4 | 9.8304 |
| 49-NLS[1,2] | 16 | 16 | 200/450 | 245.76 | 4 | 450 | 491.52 | 2 | 100 | 122.88 | 4 | 9.8304 |
| 50-LS[1,2,4] | 16 | 16 | 200/450 | 122.88 | 4 | 450 | 245.76 | 2 | 100 | 122.88 | 4 | 9.8304 |
| 50-NLS[1,2,4] | 16 | 16 | 200/450 | 122.88 | 4 | 450 | 245.76 | 2 | 100 | 122.88 | 4 | 9.8304 |
| 51-LS[1,3,4] | 16 | 16 | 200/450 | 245.76 | 4 | 450 | 245.76 | 2 | 200 | 245.76 | 4 | 9.8304 |
| 51C-LS[1,3,4,5] | 16 | 16 | 200/450 | 245.76 | 4 | 450 | 245.76 | 2 | 200 | 245.76 | 4 | 16.2202 |
| 51C-LS-Np12[1,3,4] | 12 | 12 | 200/450 | 245.76 | 4 | 450 | 245.76 | 2 | 200 | 245.76 | 4 | 12.165 |
| 51-NLS[1,3,4] | 16 | 16 | 200/450 | 245.76 | 4 | 450 | 245.76 | 2 | 200 | 245.76 | 4 | 9.8304 |
| 51C-NLS[1,3,4,5] | 16 | 16 | 200/450 | 245.76 | 4 | 450 | 245.76 | 2 | 200 | 245.76 | 4 | 16.2202 |
| 51C-NLS-Np12[1,3,4] | 12 | 12 | 200/450 | 245.76 | 4 | 450 | 245.76 | 2 | 200 | 245.76 | 4 | 12.165 |
| 54-NLS[1,2,4] | 16 | 16 | 200/450 | 122.88 | 4 | 450 | 245.76 | 2 | 200 | 122.88 | 4 | 9.8304 |
| 55-NLS[1,2,4] | 16 | 16 | 200/450 | 122.88 | 4 | 450 | 245.76 | 2 | 160 | 122.88 | 4 | 9.8304 |
| 59-NLS[1,2] | 16 | 16 | 200/450 | 250 | 4 | 450 | 250 | 2 | 200 | 250 | 4 | 10 |
| 59-LS[1,2] | 16 | 16 | 200/450 | 250 | 4 | 450 | 250 | 2 | 200 | 250 | 4 | 10 |
| 61-LS | 12 | 12 | 200/300 | 368.64 | 4 | 300 | 368.64 | 2 | 200 | 368.64 | 4 | 11.0592 |
| 78-LS[1,3,4] | 16 | 16 | 100/281 | 153.6 | 4 | 281 | 307.2 | 2 | 125 | 153.6 | 4 | 6.144 |
| 78-NLS[1,3,4] | 16 | 16 | 100/281 | 153.6 | 4 | 281 | 307.2 | 2 | 125 | 153.6 | 4 | 6.144 |
| 82C-LS[5] | 12 | 12 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 200 | 245.76 | 4 | 24.3302 |
| 83C-LS[5] | 16 | 16 | 200/337 | 368.64 | 4 | 337 | 368.64 | 2 | 200 | 368.64 | 4 | 24.3302 |
| 90-NLS[1,2,4] | 16 | 16 | 200/450 | 122.88 | 4 | 450 | 245.76 | 2 | 100 | 122.88 | 4 | 4.9152 |
| 93C-LS*[5] | 12 | 24 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 300 | 245.76 | 4 | 24.3302 |
| 93C-NLS*[5] | 12 | 24 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 300 | 245.76 | 4 | 24.3302 |
| 95C-LS*[5] | 16 | 16 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 300 | 245.76 | 4 | 16.2202 |
| 95C-NLS*[5] | 16 | 16 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 300 | 245.76 | 4 | 16.2202 |
| 98-LS* | 12 | 12 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 300 | 245.76 | 4 | 14.7 |
| 98-NLS* | 12 | 12 | 200/450 | 491.52 | 4 | 450 | 491.52 | 2 | 300 | 245.76 | 4 | 14.7 |
| 102-LS[1,3,4] | 16 | 16 | 200/330 | 245.76 | 4 | 450 | 245.76 | 2 | 200 | 245.76 | 4 | 9.8304 |

**Notes:** LS = Link Sharing; NLS = Non-Link Sharing

[1] DPD specific profile

[2] Internal DPD actuator rate is 491.52 MSPS (DPD HB enabled)

[3] Internal DPD actuator rate is 983.04 MSPS (DPD HB enabled)

[4] DPD x4 HB enabled

[5] Only supported on B silicon

Additional Note: Other use cases not included in the above table may be present in the build package – these use cases have not been verified by ADI and there is no guarantee of operation/performance.

* These profiles exceed the datasheet maximum bandwidth specification and therefore may not meet all datasheet performance specs.