デュアル/クワッド・マイクロパワー 1MHz C-Loadピコアンペア バイアス電流JFET入力オペアンプ

特長

- **入力バイアス電流：20pA最大**
- **電源電流/アンプ：200μA最大**
- **利得バンド幅積：1MHz標準**
- **スルーレート：0.9V/μs標準**
- **入力同相範囲には正レールが含まれる**
- **C-Load™によって10nFまでユニティゲインで安定**
- **±5V、±15V電源でスペックを保証**
- **マッチング特性を保証**
- **標準ピン配置：SO-8、SO-14パッケージ**

アプリケーション

- **バッテリ電源機器**
- **フォトカレント・アンプ**
- **低周波、マイクロパワー・アクティブフィルタ**
- **低垂下トラック&ホールド回路**

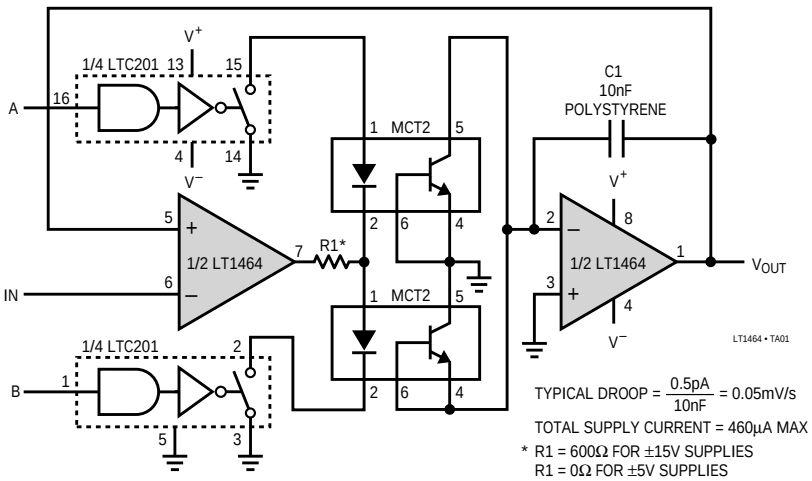
概要

LT®1464(デュアル)およびLT1465(クワッド)は、ピコアンペア入力バイアス電流(500fA標準)と10nFまでの容量性負荷に対してユニティゲイン安定動作を提供する最初のマイクロパワー・オペアンプ(1アンプ当たり最大200μA)です。出力は、1桁以上高い電流を必要とするオペアンプと同様に、10k負荷をいずれかの電源の1.5V以内に振幅させることができます。このユニークな性能を兼ね備えているため、LT1464/LT1465は広範な入力および出力インピーダンスに対し最適なデバイスです。

LT1464/LT1465の設計およびテストでは、特に±15Vおよび±5V電源を使用した低コストのSO-8(デュアル)および14ピンSOパッケージ(クワッド)で最適な性能が得られるよう配慮されています。入力同相範囲には正電源レールが含まれます。また、スルーレート(0.5V/μs最小)と利得・バンド幅積(650kHz最小)は100%テストされています。さらに、完全なマッチング仕様も提供されています。

TYPICAL APPLICATION

Micropower Low Droop Track-and-Hold/Peak Detector



$$\text{TYPICAL DROOP} = \frac{0.5\text{pA}}{10\text{nF}} = 0.05\text{mV/s}$$

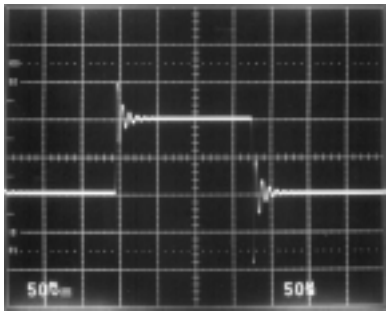
TOTAL SUPPLY CURRENT = 460μA MAX

* R1 = 600Ω FOR ±15V SUPPLIES
R1 = 0Ω FOR ±5V SUPPLIES

FUNCTION	MODE	IN A	IN B	MODE	IN A	IN B
Track-and-Hold	Track	0	0	Hold	1	1
Positive Peak Detector	Reset	0	0	Store	0	1
Negative Peak Detector	Reset	0	0	Store	1	0

LTC201 switch is open for logic "1".

Small-Signal Response, C_{LOAD} = 10nF



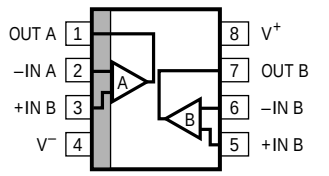
A_V = 1
V_S = ±5V, ±15V
C_L = 10nF

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Current 20mA
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range ..... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S)

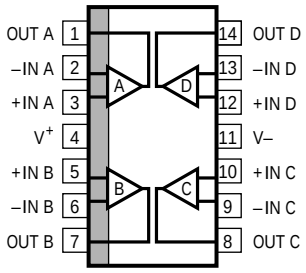
ORDER PART NUMBER

LT1464CN8
LT1464CS8

S8 PART MARKING

1464

TOP VIEW



N PACKAGE
14-LEAD PDIP

S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 110°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER

LT1465CN
LT1465CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = ±5V V_S = ±15V		0.4 0.6	0.8 2.0	mV mV
I_{OS}	Input Offset Current			0.3	15	pA
I_B	Input Bias Current			±0.5	±20	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz		33 24		nV/√Hz nV/√Hz
	Input Noise Current Density	f_O = 10Hz, 1kHz (Note 3)		0.4		fA/√Hz
CMRR	Common Mode Rejection Ratio	V_{CM} = –12.5V to 15V	74	85		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±20V	78	90		dB
R_{IN}	Input Resistance—Differential Common Mode Common Mode	 V_{CM} = –12.5V to 8V V_{CM} = 8V to 15V		10^{12} 10^{12} 10^{11}		Ω Ω Ω
C_{IN}	Input Capacitance			3		pF
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V, R_L = 10k V_O = ±10V, R_L = 2k	300 150	900 450		V/mV V/mV
		V_S = ±5V, V_O = ±2V, R_L = 10k V_S = ±5V, V_O = ±1V, R_L = 2k	100 50	250 170		V/mV V/mV

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage Swing	$R_L = 10k$ $R_L = 2k$ $V_S = \pm 5V$, $R_L = 2k$	±13.5 ±13.3 ±3.5	±13.7 ±13.5 ±3.7		V V V
SR	Slew Rate	$R_L = 10k$ (Note 4)	0.5	0.9		V/µs
GBW	Gain Bandwidth Product	f = 10kHz	650	1000		kHz
I_S	Supply Current per Amplifier	 $V_S = \pm 5V$		145 135	200 200	µA µA
	Channel Separation	f = 10Hz, $V_O = \pm 10V$, $R_L = 10k$		132		dB
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$ $V_S = \pm 15V$		0.5 0.8	1.3 3.3	mV mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)			0.5	30	pA
ΔCMRR	Common Mode Rejection Match	(Notes 5, 7)	71	85		dB
ΔPSRR	Power Supply Rejection Match	(Notes 5, 7)	74	88		dB

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm 5V$ $V_S = \pm 15V$	● ●		0.5 0.9	1.4 2.8	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		7	20	µV/°C
I_{OS}	Input Offset Current		●		25	450	pA
I_B	Input Bias Current		●		150	750	pA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -12V$ to 15V	●	73	85		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 20V$	●	77	89		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10k$ $V_O = \pm 10V$, $R_L = 2k$	● ●	200 100	600 350		V/mV V/mV
		$V_S = \pm 5V$, $V_O = \pm 2V$, $R_L = 10k$ $V_S = \pm 5V$, $V_O = \pm 1V$, $R_L = 2k$	● ●	80 45	200 150		V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$ $R_L = 2k$ $V_S = \pm 5V$, $R_L = 2k$	● ● ●	±13.4 ±13.2 ±3.4	±13.6 ±13.4 ±3.6		V V V
SR	Slew Rate	$R_L = 10k$ (Note 4)	●	0.4	0.8		V/µs
GBW	Gain Bandwidth Product	f = 10kHz	●	540	870		kHz
I_S	Supply Current per Amplifier	 $V_S = \pm 5V$	● ●		160 150	220 220	µA µA
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$ $V_S = \pm 15V$	● ●		0.7 0.9	2.0 3.5	mV mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)		●		35	500	pA
ΔCMRR	Common Mode Rejection Match	(Notes 5, 7)	●	70	84		dB
ΔPSRR	Power Supply Rejection Match	(Notes 5, 7)	●	73	85		dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$ (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm 5V$ $V_S = \pm 15V$	● ●		0.6 1.0	1.5 3.0	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		7	20	µV/°C
I_{OS}	Input Offset Current		●		60	700	pA
I_B	Input Bias Current		●		300	2500	pA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -12V$ to 15V	●	72	84		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 20V$	●	76	88		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10k$ $V_O = \pm 10V$, $R_L = 2k$	● ●	175 80	400 250		V/mV V/mV
		$V_S = \pm 5V$, $V_O = \pm 2V$, $R_L = 10k$ $V_S = \pm 5V$, $V_O = \pm 1V$, $R_L = 2k$	● ●	70 45	180 140		V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$ $R_L = 2k$ $V_S = \pm 5V$, $R_L = 2k$	● ● ●	±13.2 ±13.0 ±3.2	±13.4 ±13.2 ±3.4		V V V
SR	Slew Rate	$R_L = 10k$ (Note 4)	●	0.35	0.7		V/µs
GBW	Gain Bandwidth Product	f = 10kHz	●	510	850		kHz
I_S	Supply Current per Amplifier	 $V_S = \pm 5V$	● ●		165 160	230 230	µA µA
V_{OS}	Offset Voltage Match (Note 7)	$V_S = \pm 5V$ $V_S = \pm 15V$	● ●		0.8 1.0	2.5 4.0	mV mV
ΔI_B^+	Noninverting Bias Current Match (Note 7)		●		70	800	pA
ΔCMRR	Common Mode Rejection Match	(Notes 5, 7)	●	69	83		dB
ΔPSRR	Power Supply Rejection Match	(Notes 5, 7)	●	73	81		dB

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as 60% yield of parameter distributions of individual amplifiers, i.e., out of 100 LT1465s (or 100 LT1464s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: The LT1464 and LT1465 are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. Guaranteed I grade parts are available, consult factory.

Note 3: Current noise is calculated from the formula: $i_n = (2qi_b)^{1/2}$ where $q = (1.6)(10)^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 4: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output is measured at ±2.5V.

Note 5: ΔCMRR and ΔPSRR are defined as follows:

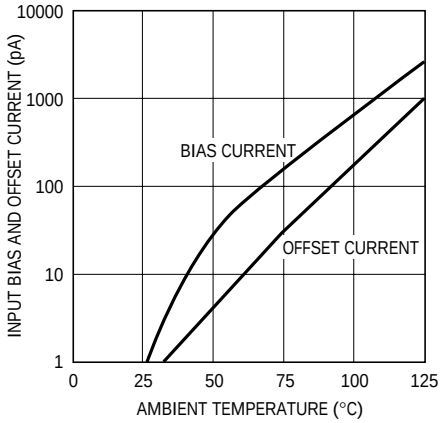
1. CMRR and PSRR are measured in µV/V on the individual amplifiers.
2. The difference is calculated between the matching sides in µV/V.
3. The result is converted to dB.

Note 6: This parameter is not 100% tested.

Note 7: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1465; between the two amplifiers on the LT1464.

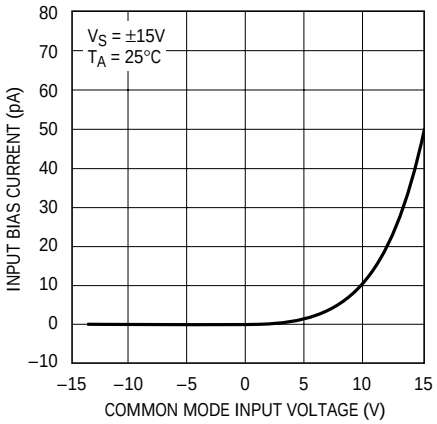
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias and Offset Current vs Temperature



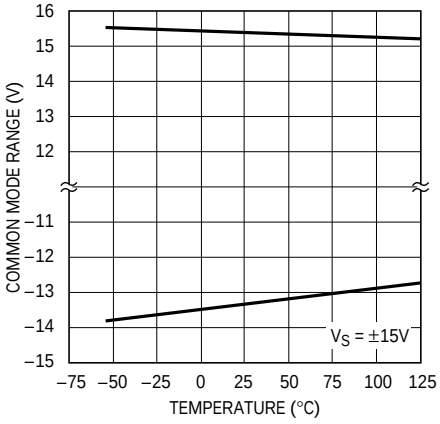
LT1464 • TPC01

Input Bias Current Over the Common Mode Range



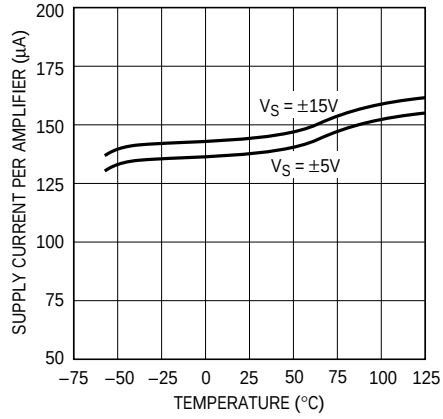
LT1464 • TPC02

Common Mode Range vs Temperature



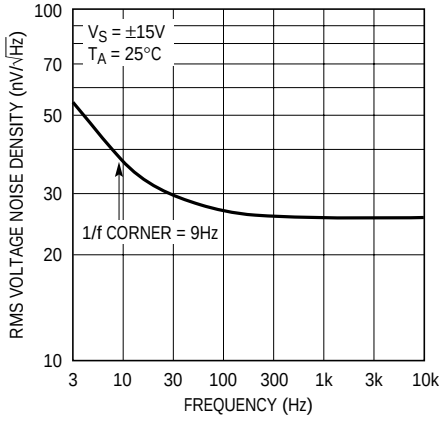
LT1464 • TPC03

Supply Current vs Temperature



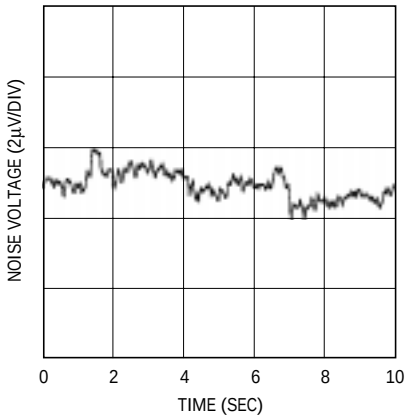
LT1464 • TPC04

Voltage Noise vs Frequency



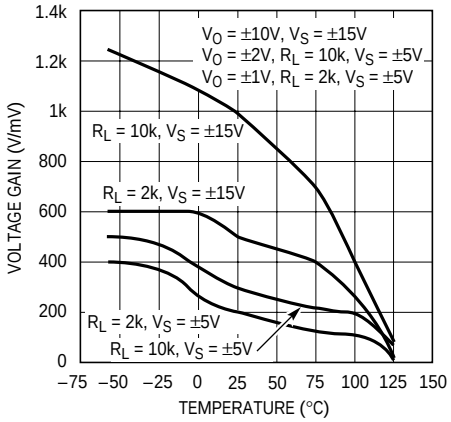
LT1464 • TPC05

0.1Hz to 10Hz Noise



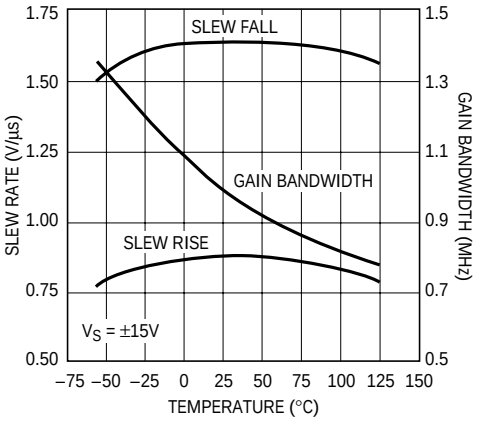
LT1464 • TPC06

Voltage Gain vs Temperature



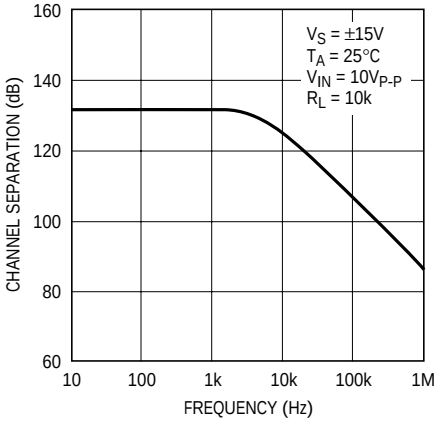
LT1464 • TPC07

Slew Rate, Gain Bandwidth Product vs Temperature



LT1464 • TPC08

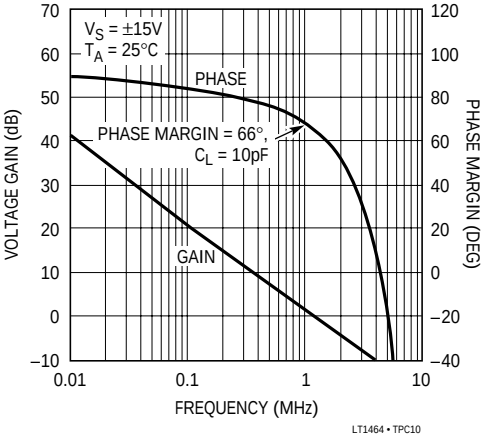
Channel Separation vs Frequency



LT1464 • TPC09

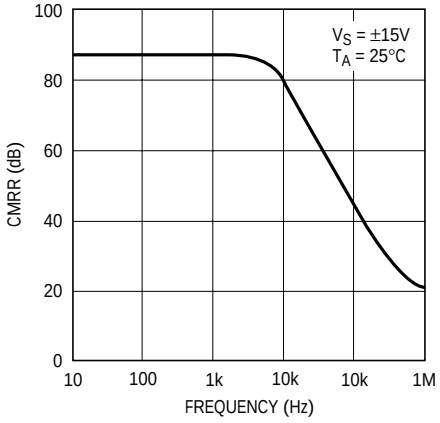
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase vs Frequency



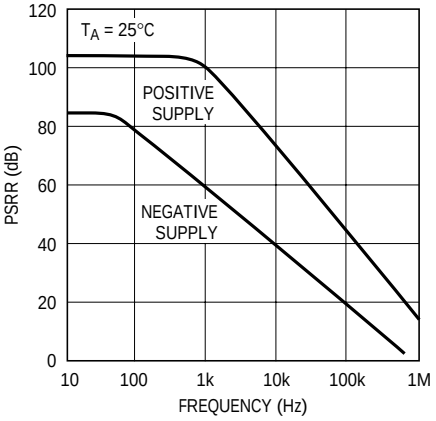
LT1464 • TPC10

Common Mode Rejection Ratio vs Frequency



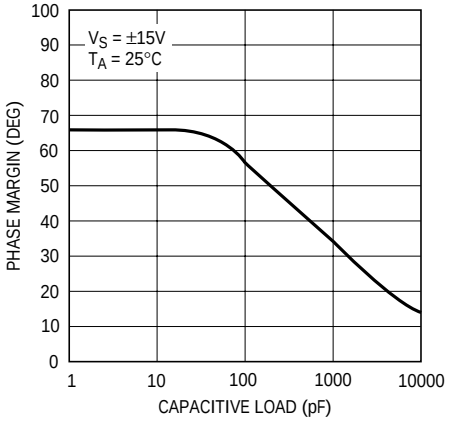
LT1464 • TPC11

Power Supply Rejection Ratio vs Frequency



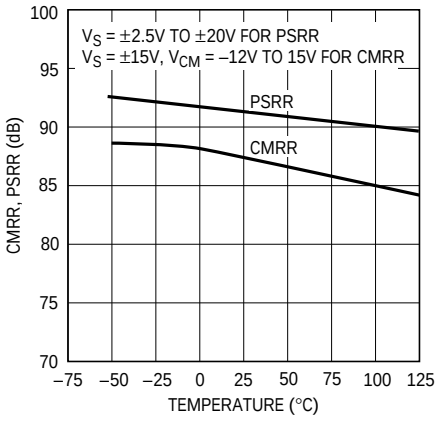
LT1464 • TPC12

Phase Margin vs C_{LOAD}



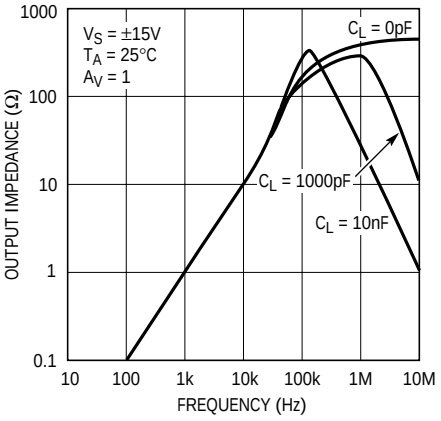
LT1464 • TPC13

Common Mode and Power Supply Rejections vs Temperature



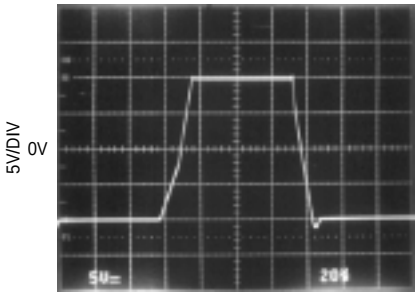
LT1464 • TPC14

Closed-Loop Output Impedance



LT1464 • TPC15

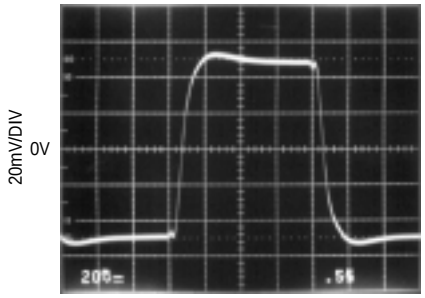
Large-Signal Response, V_S = ±15V



A_V = 1 20µs/DIV
C_L = 10pF

LT1464 • TPC16

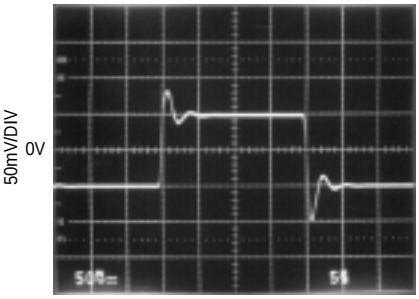
Small-Signal Response, V_S = ±5V, ±15V



A_V = 1 0.5µs/DIV
C_L = 10pF

LT1464 • TPC17

Small-Signal Response, V_S = ±5V, ±15V, C_{LOAD} = 1000pF



A_V = 1 5µs/DIV
C_L = 1000pF

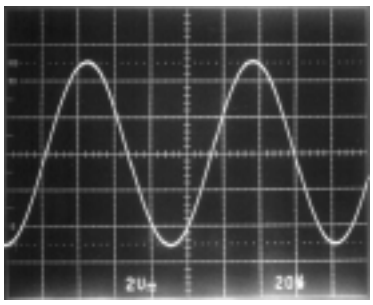
LT1464 • TPC18

アプリケーション情報

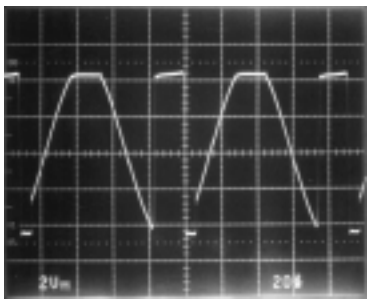
逆位相保護

ほとんどの業界標準JFET入力シングル、デュアル、およびクワッドのオペアンプでは、入力が負の同相制限範囲を超えると、出力で位相反転が起こります。同相範囲は±5V電源では重要です。以下の図に、±5.2Vの正弦波入力(図1a)、ユニティゲイン・フォロワモードでの競合JFET入力オペアンプの応答(図1b)、およびLT1464/LT1465の応答(図1c)を示します。

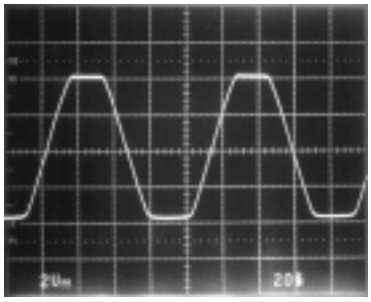
図1bのように位相反転が起こると、サーボ機構がロックアップする可能性があります。LT1464/LT1465は、同相入力が電源電圧内にあるときには位相反転を起こしません。



(1a) ±5.2V Sine Wave



(1b) Typical JFET Input Op Amp with ±5V Supplies

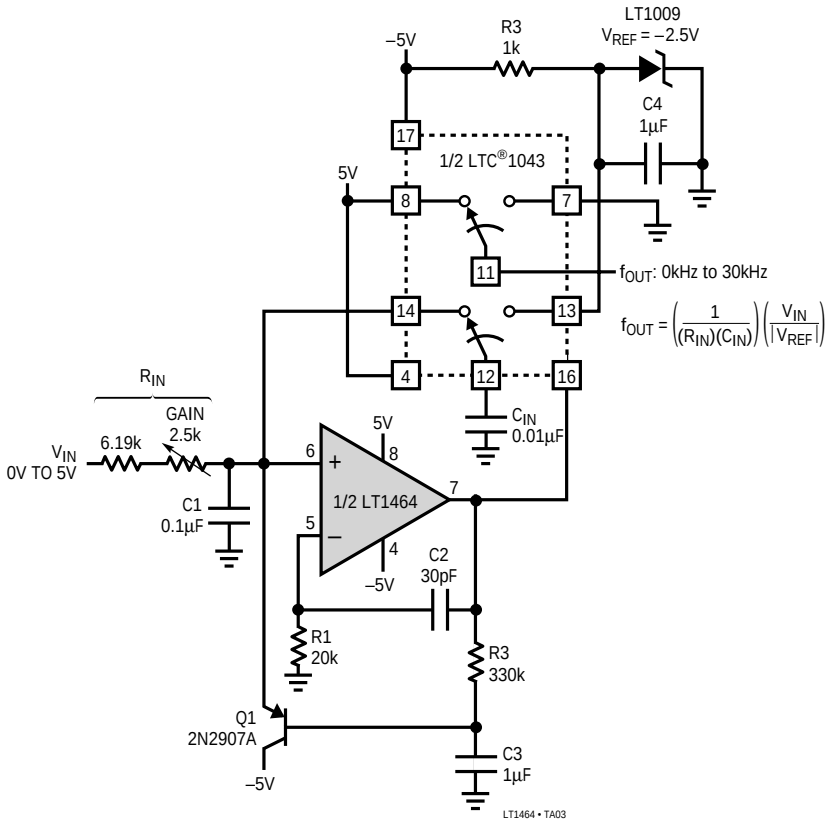


(1c) LT1464/LT1465 Output with ±5V Supplies

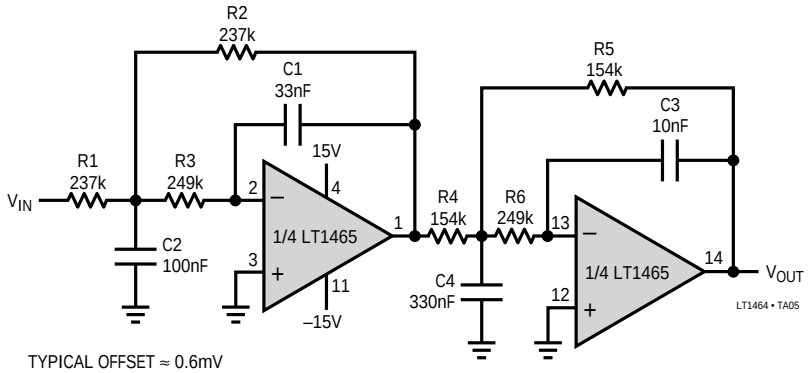
Figure 1. Voltage Follower with Input Exceeding the Common Mode Range (V_S = ±5V)

TYPICAL APPLICATIONS

Low Voltage 0.016% Voltage to Frequency Converter

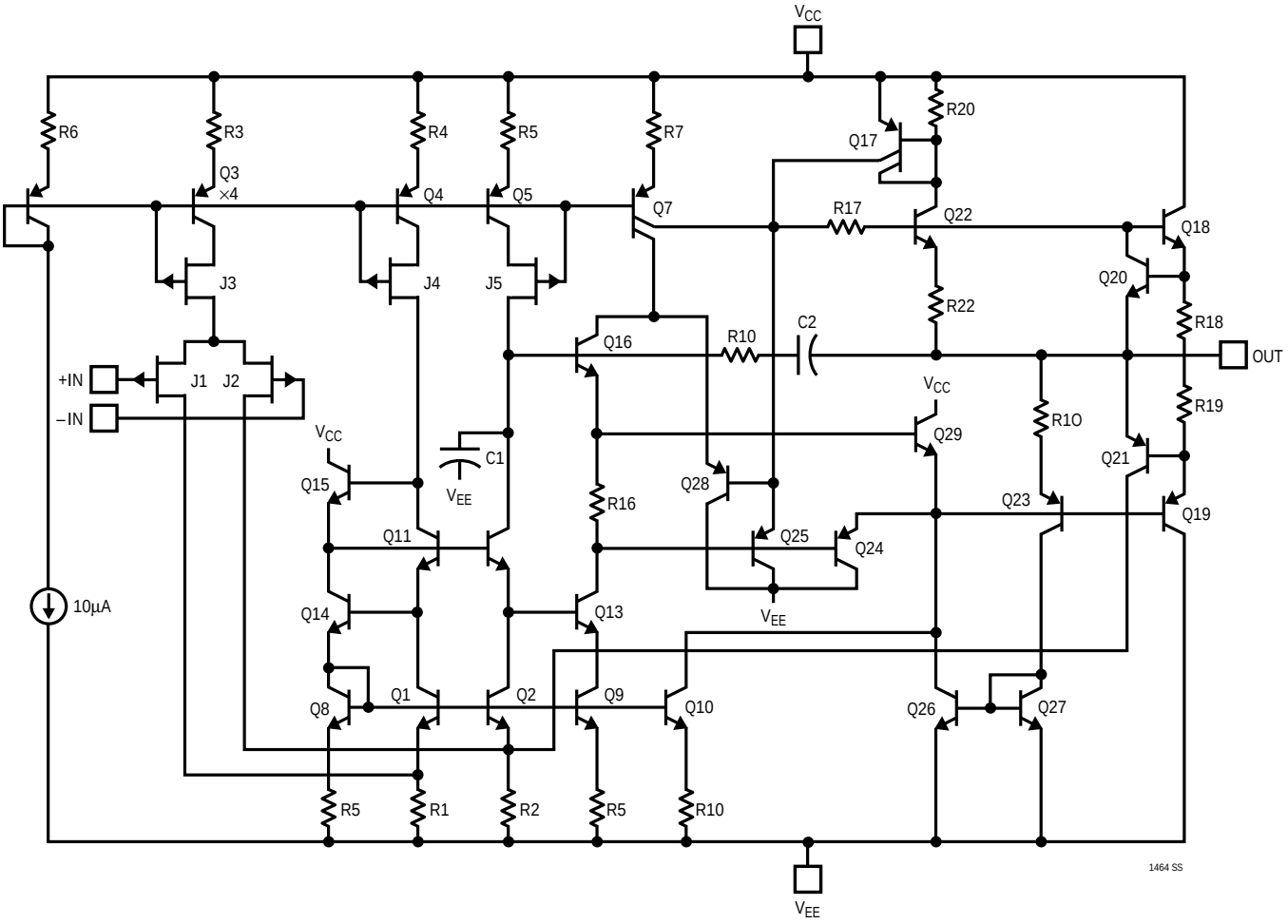


10Hz 4th Order Chebyshev Lowpass Filter (0.01dB Ripple)



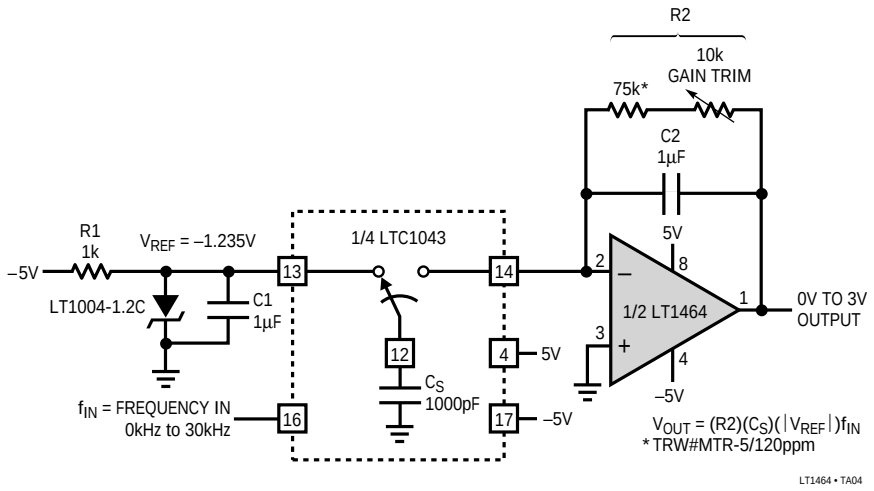
TYPICAL OFFSET ≈ 0.6mV
1% TOLERANCES
FOR V_{IN} = 10V_{P-P}, V_{OUT} = –110dB AT f > 300Hz
V_{OUT} = –6dB AT f = 16Hz
THE LOW INPUT BIAS CURRENTS ALLOW THE USE OF HIGH RESISTOR VALUES

SIMPLIFIED SCHEMATIC



TYPICAL APPLICATION

Low Voltage 0.027% Frequency to Voltage Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1057	Dual JFET Input Precision, High Speed Op Amp	Fast Settling Time, 14V/µs Slew Rate, 5Mhz GBW, 450µV V_{OS} (Max), 50pA I_{OS} (Max)
LT1113	Dual Low Noise, Precision, JFET Input Op Amp	6nV/$\sqrt{Hz}$ Input Noise Voltage Density, 480pA I_B, 6.3MHz GBW
LT1169	Dual Low Noise, Picoampere Bias Current, JFET Input Op Amp	20pA I_B, 8nV/$\sqrt{Hz}$ e_n, 5.3MHz GBW, 1.5pF Input Capacitance
LT1457	Dual Precision JFET Input Op Amp C-Load	Drives 10,000pF Capacitive Load, 450µV V_{OS} (Max), 4µV/°C Drift
LT1462/LT1463	Dual/Quad Micropower, C-Load Picoampere Bias Current JFET Input Op Amps	28µA Supply Current Per Amplifiers Drives 10µF Capacitive Load, 175kHz GBW